

FIG. 1

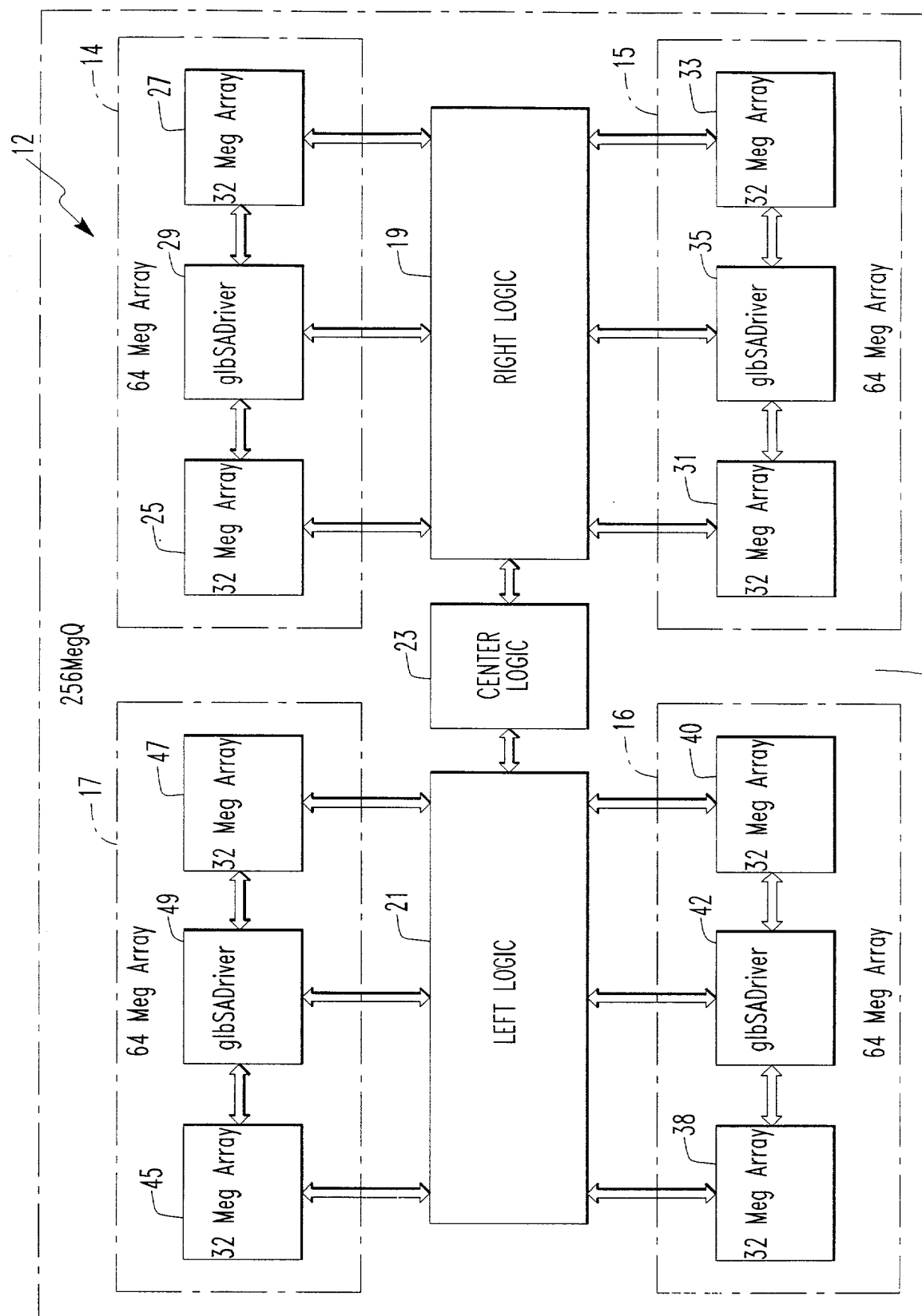


FIG. 2

FIG. 3A

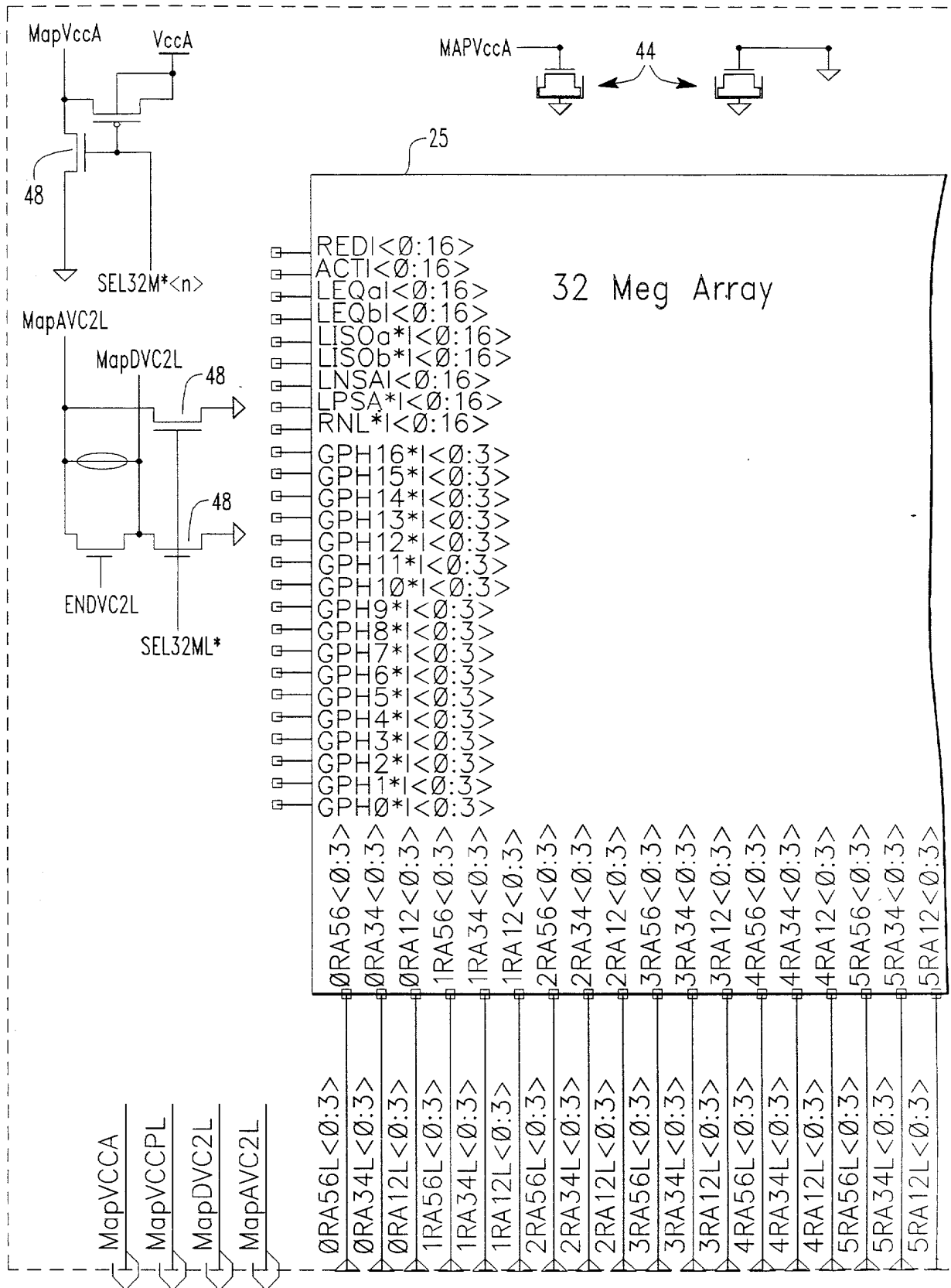


FIG. 3B

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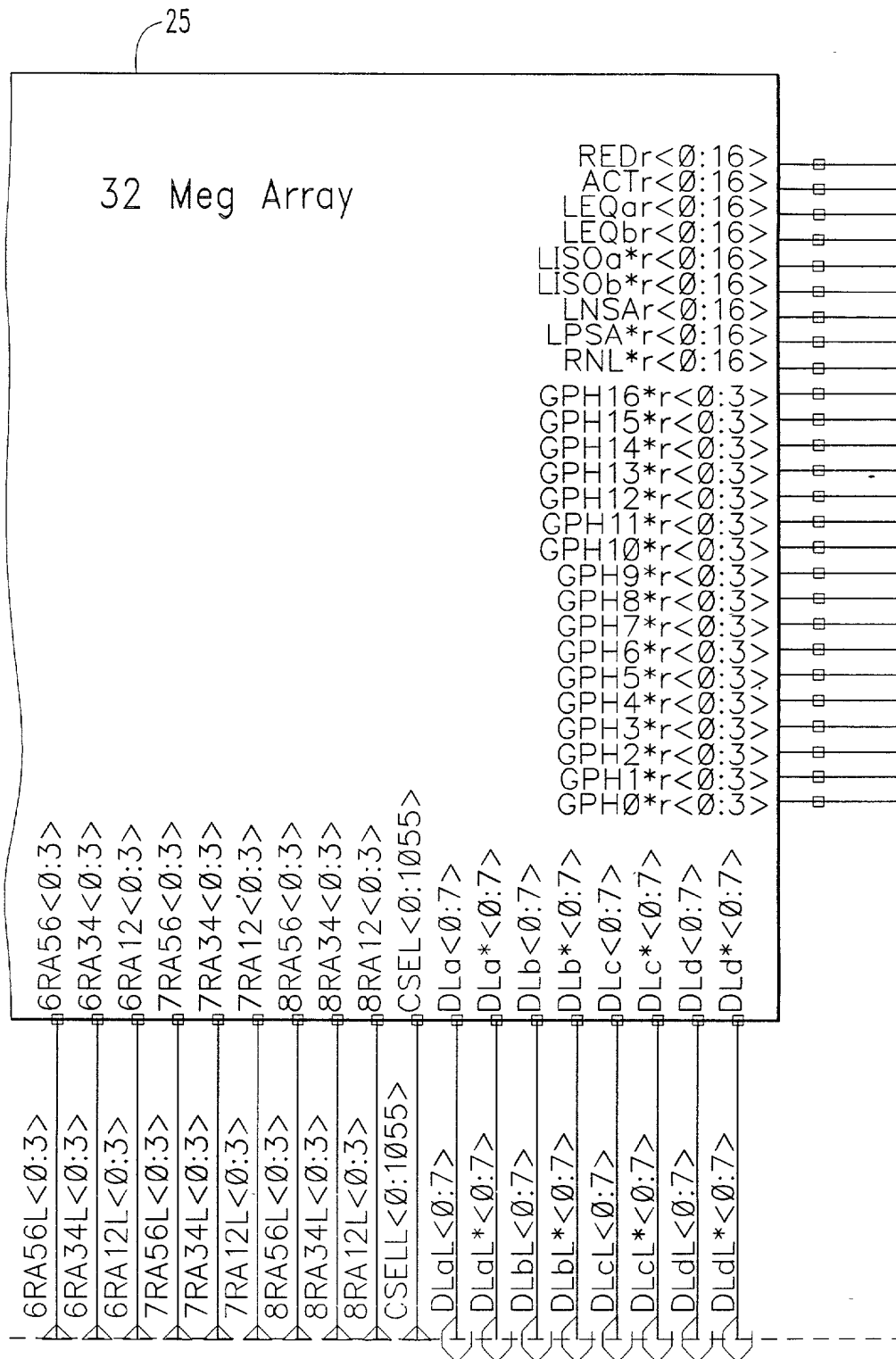
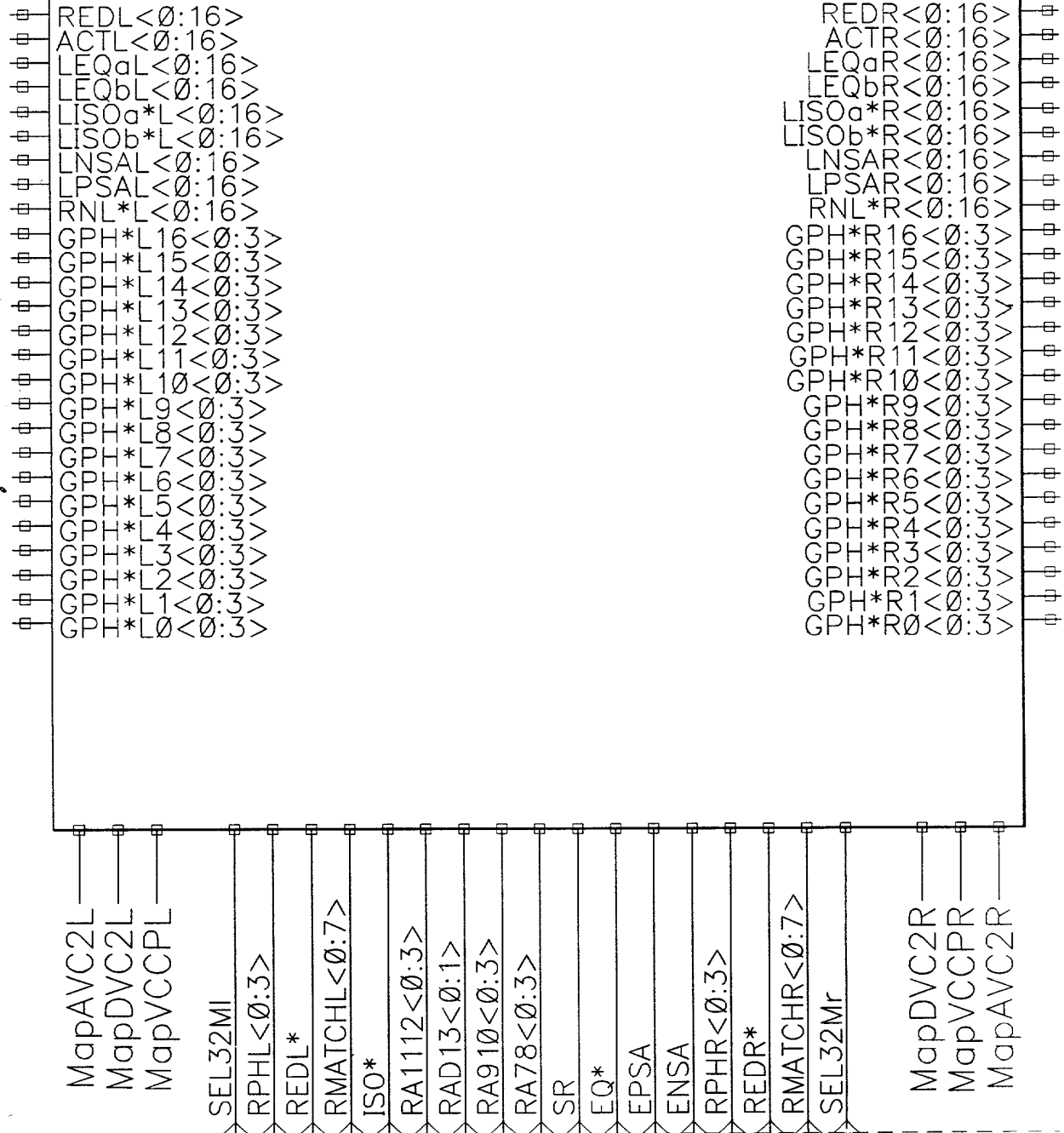


FIG. 3C

64 Meg Array

29

glbSADriver



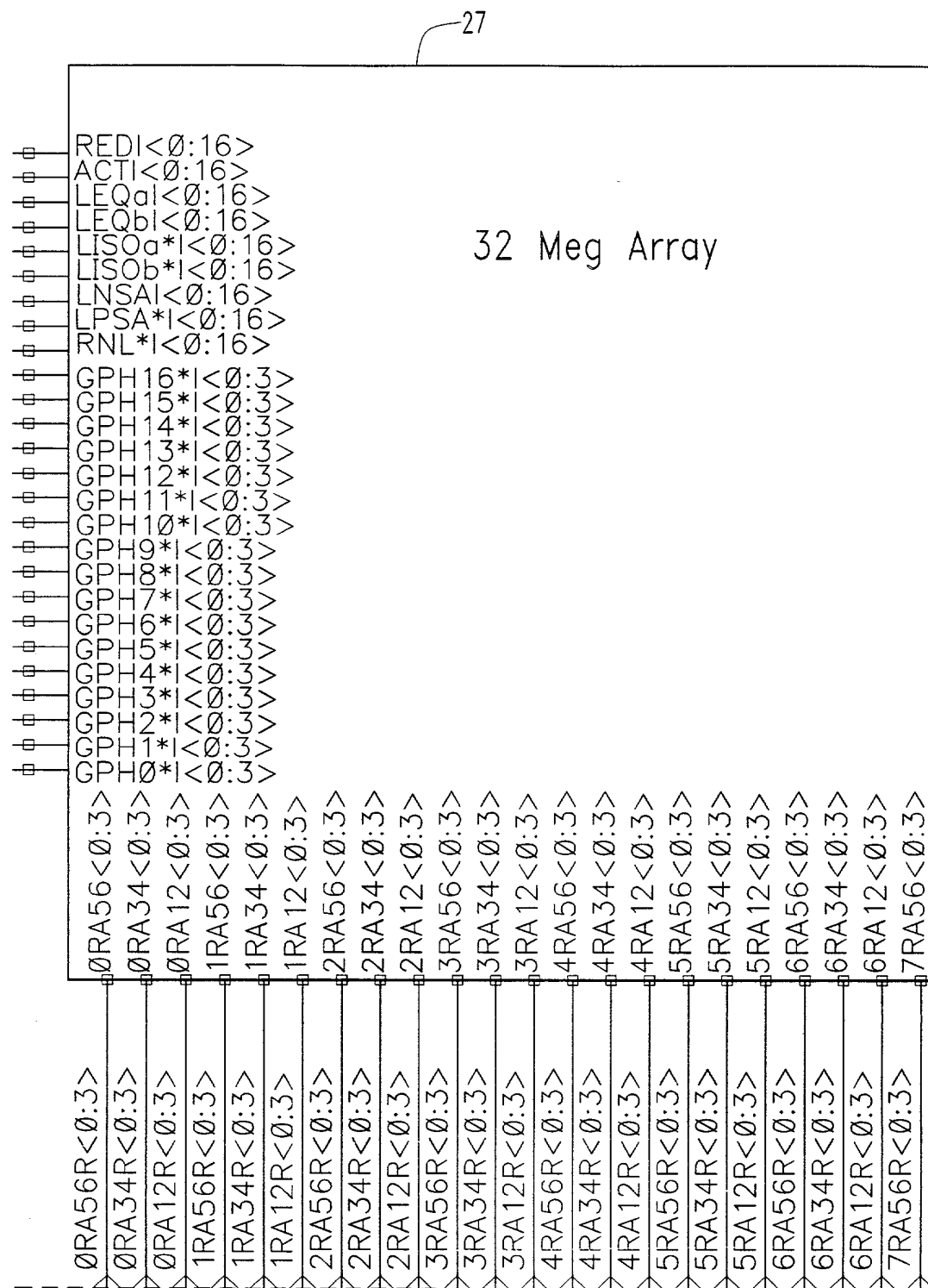
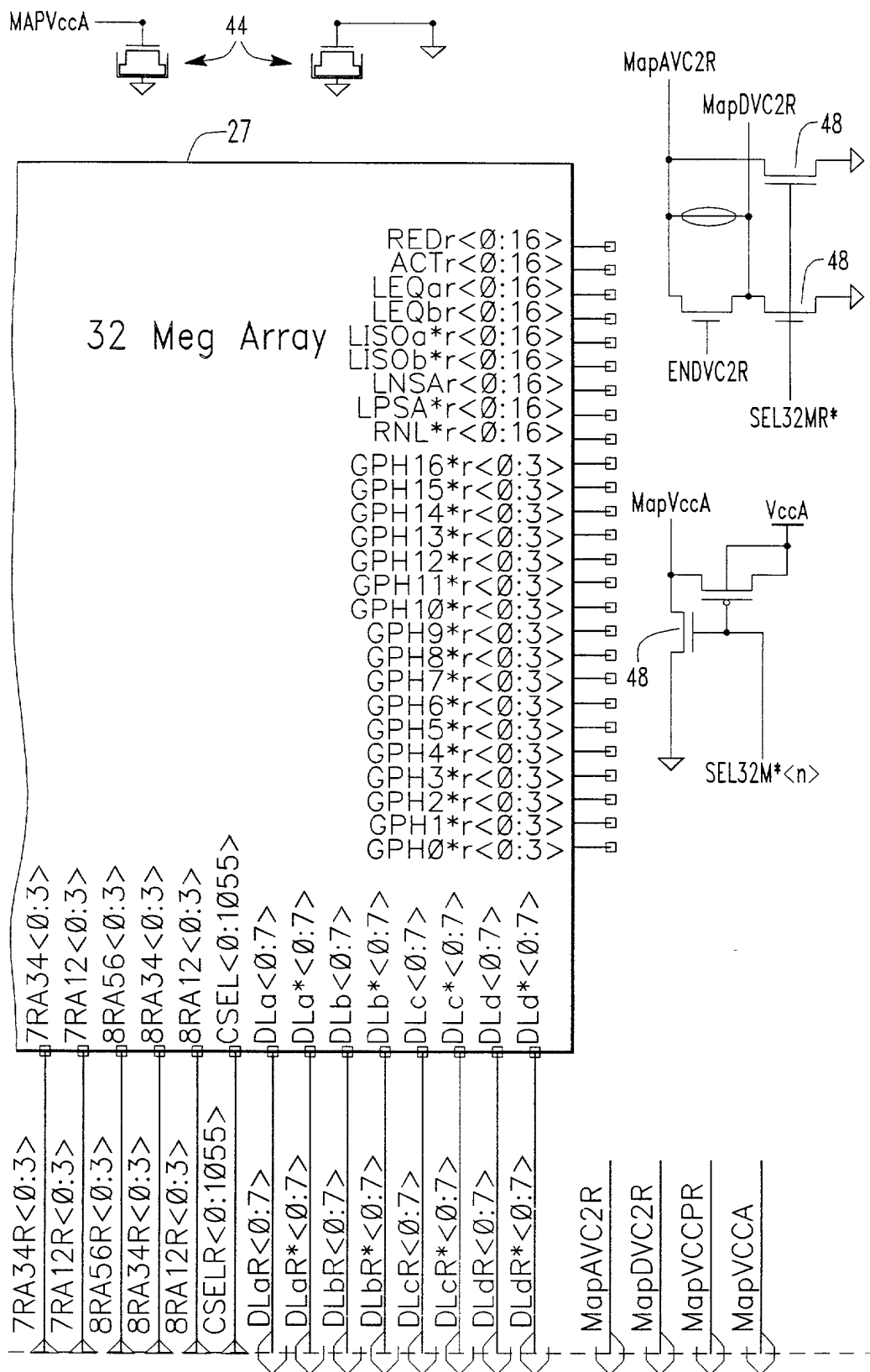


FIG. 3E

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32MEG ARRAY

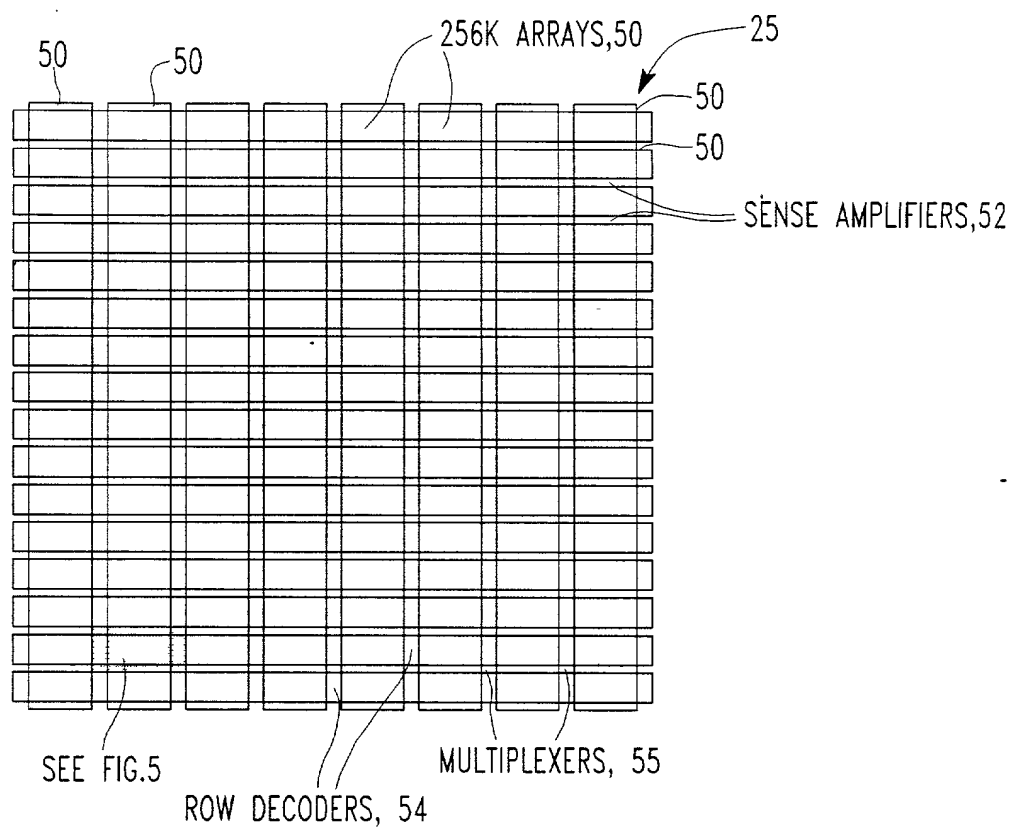


FIG. 4

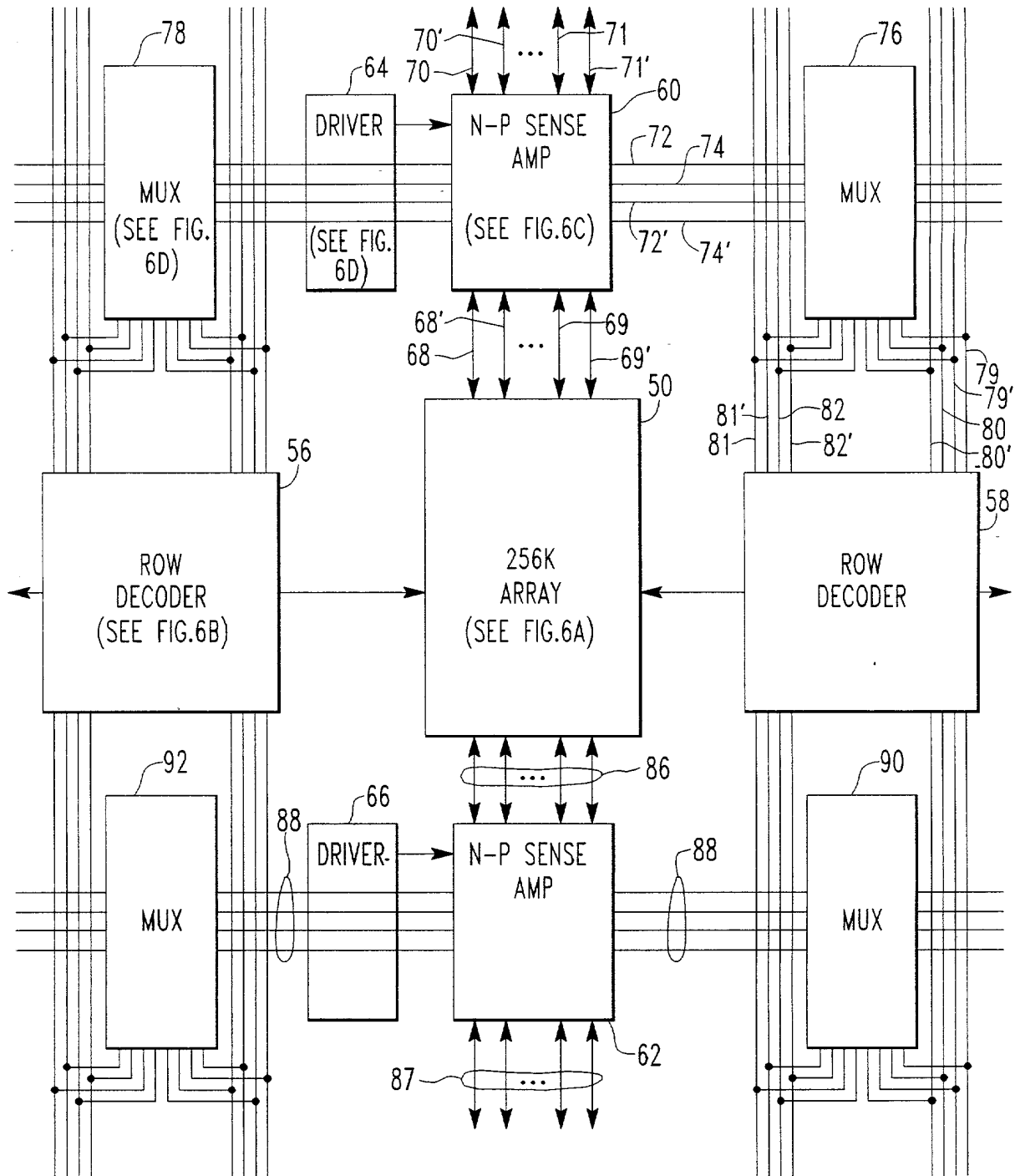


FIG. 5

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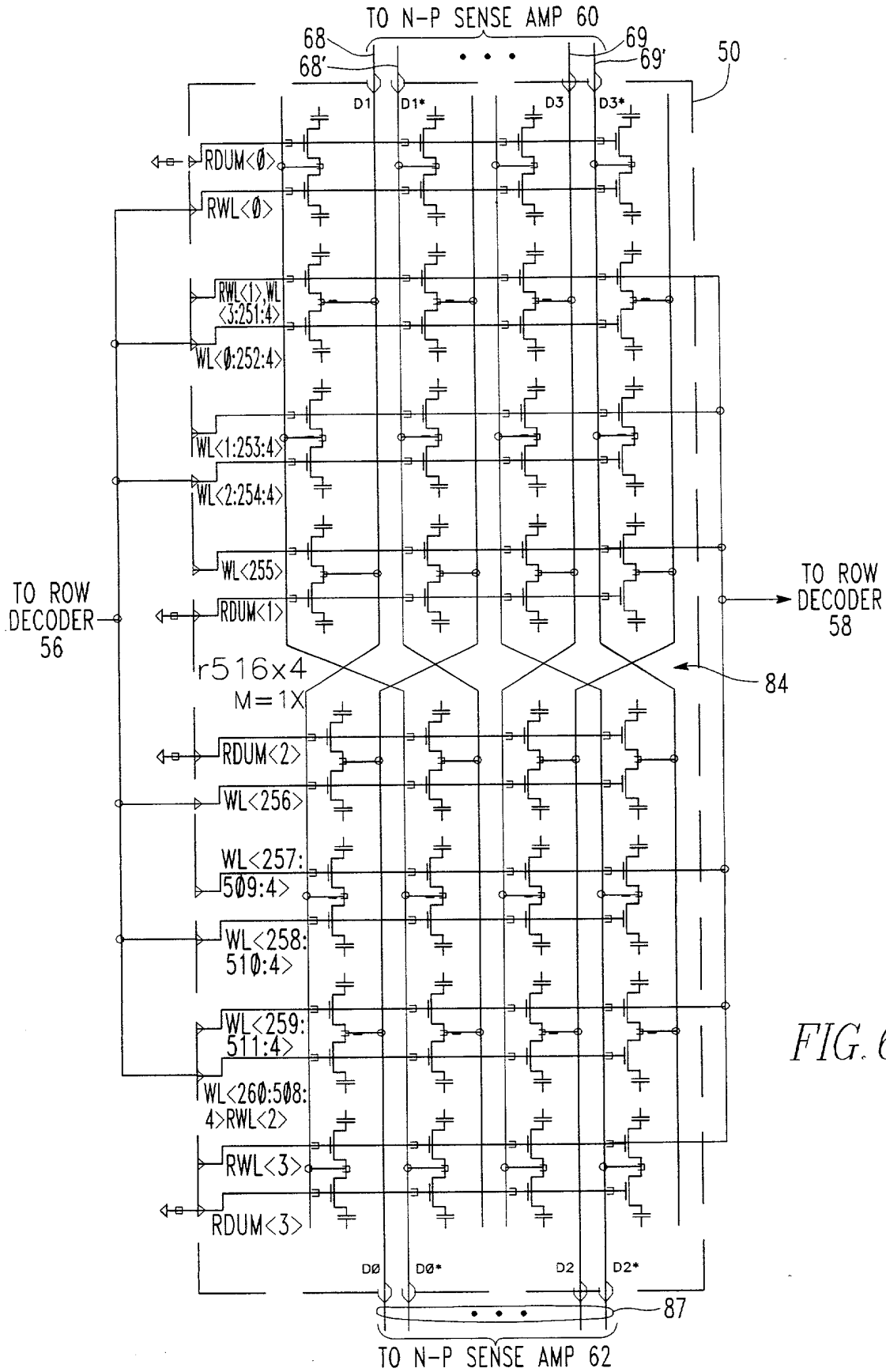
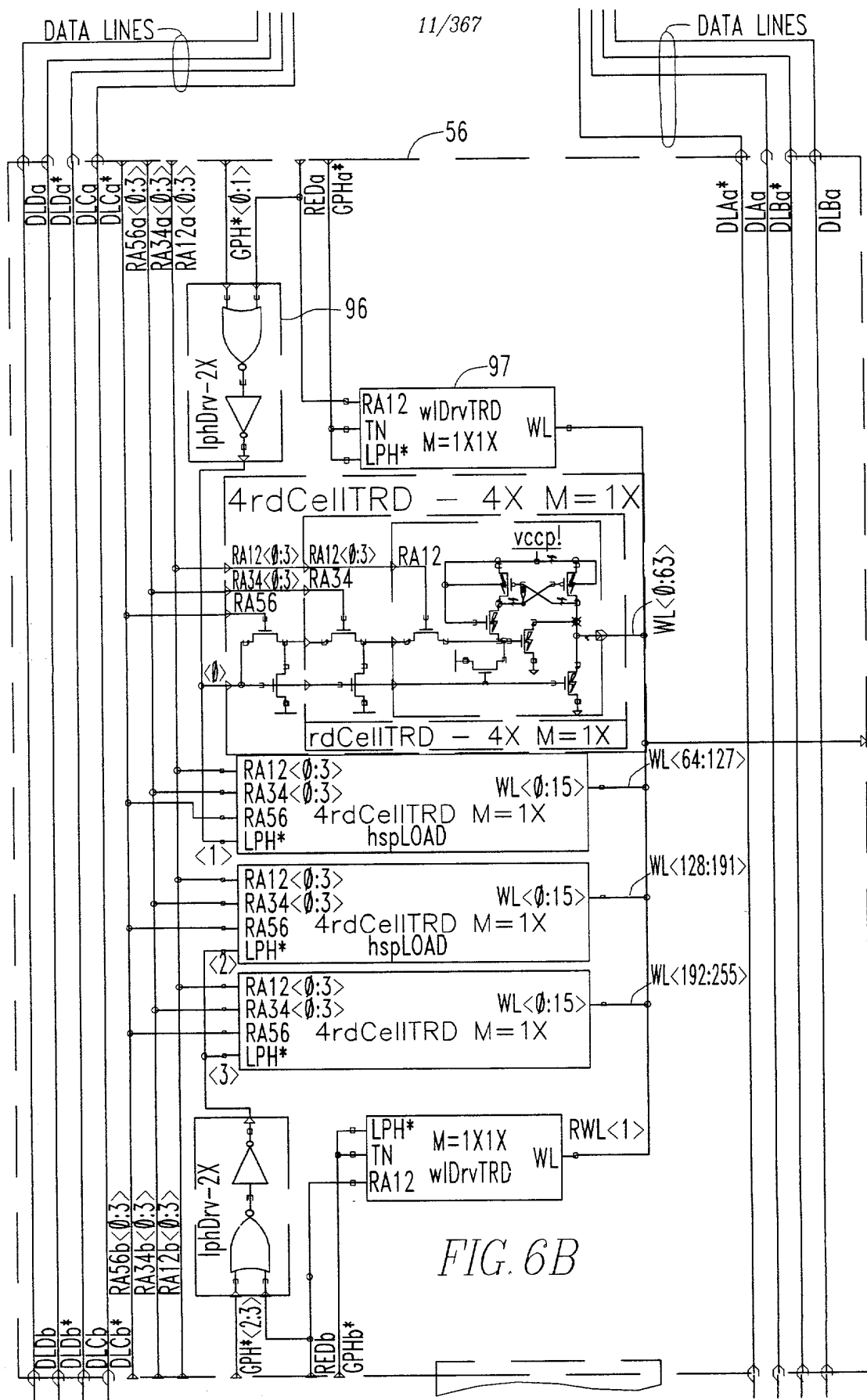
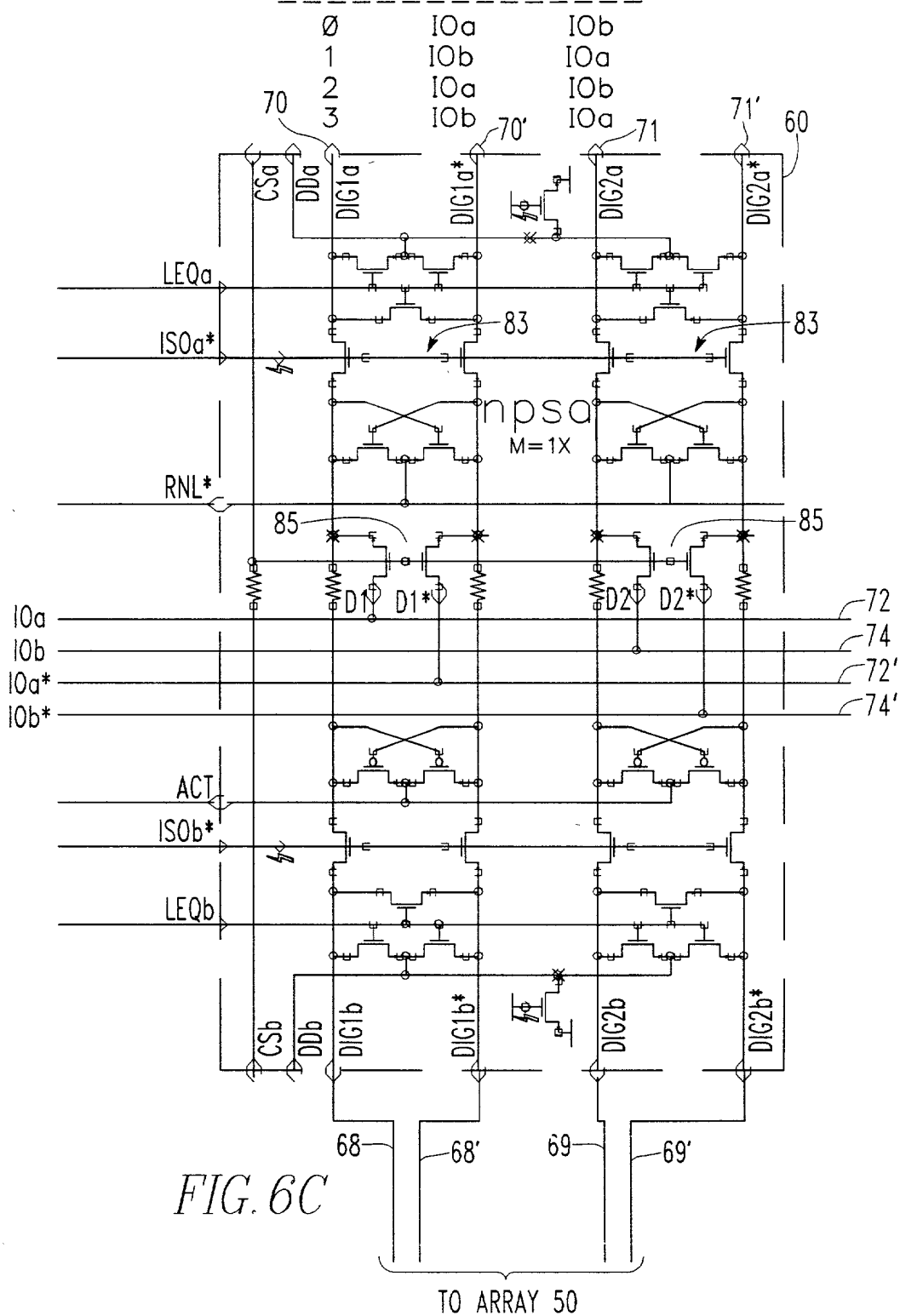


FIG. 6A



Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:
CA01* D1(even) D2(odd)



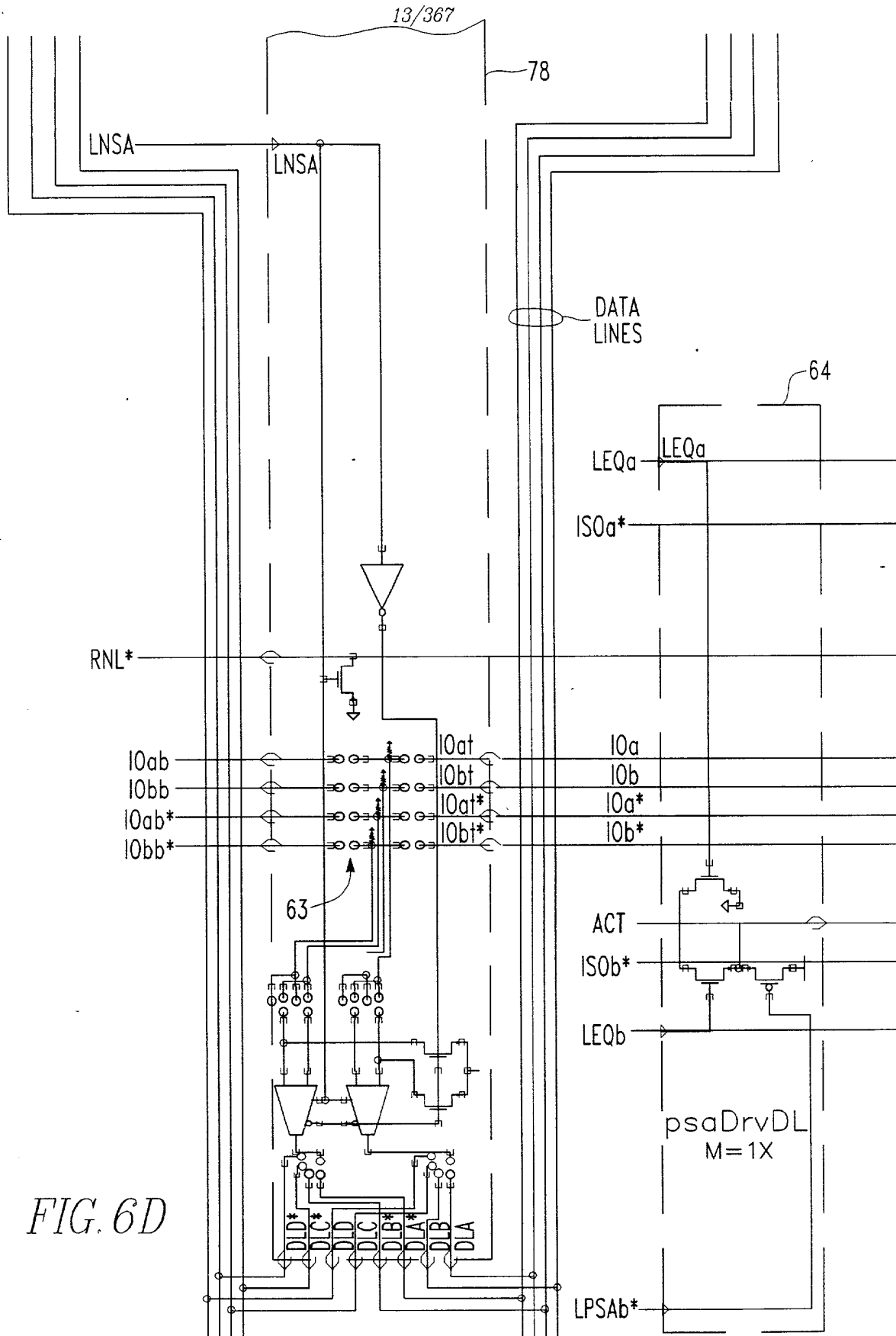


FIG. 6D



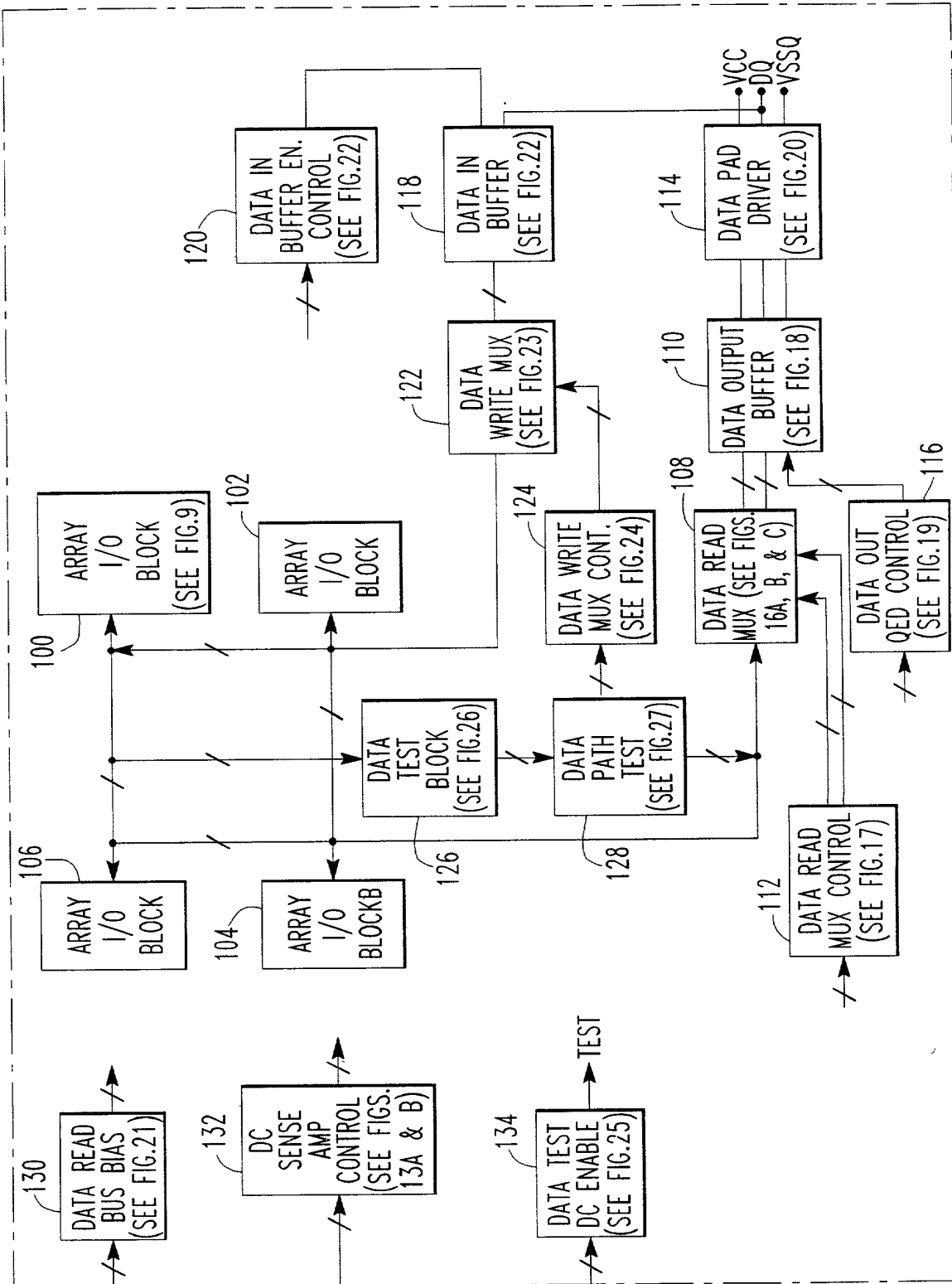


FIG. 8

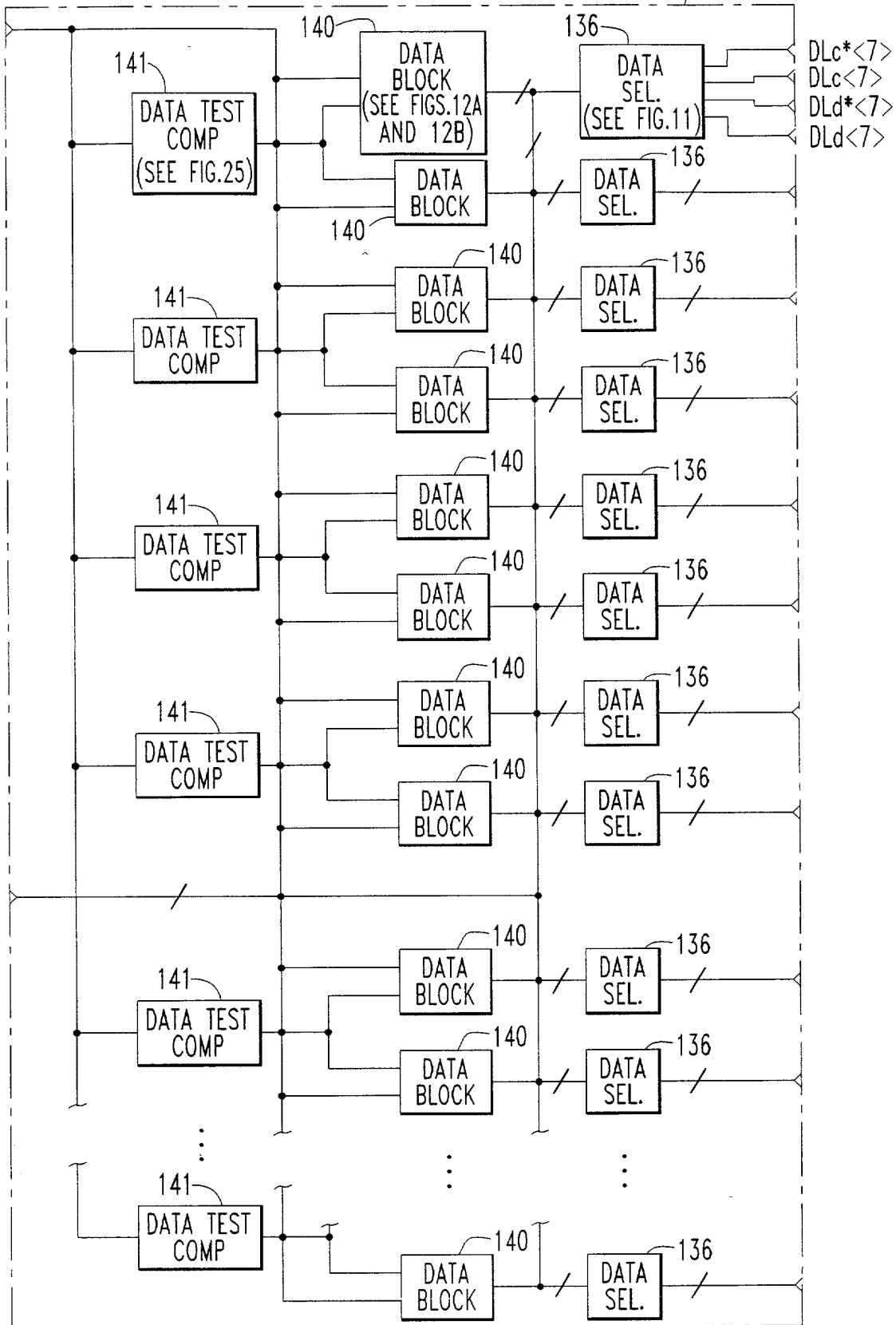
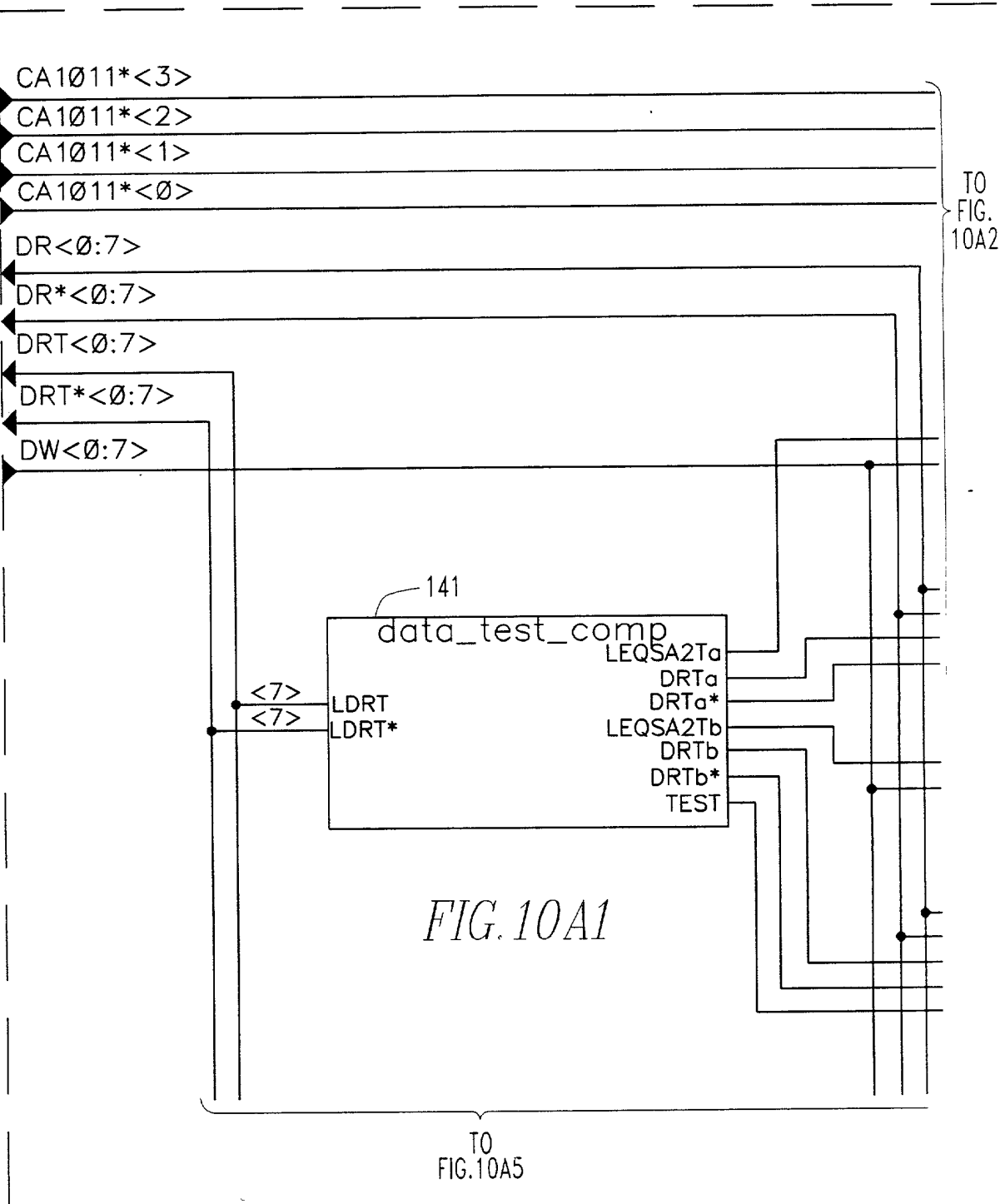


FIG. 9



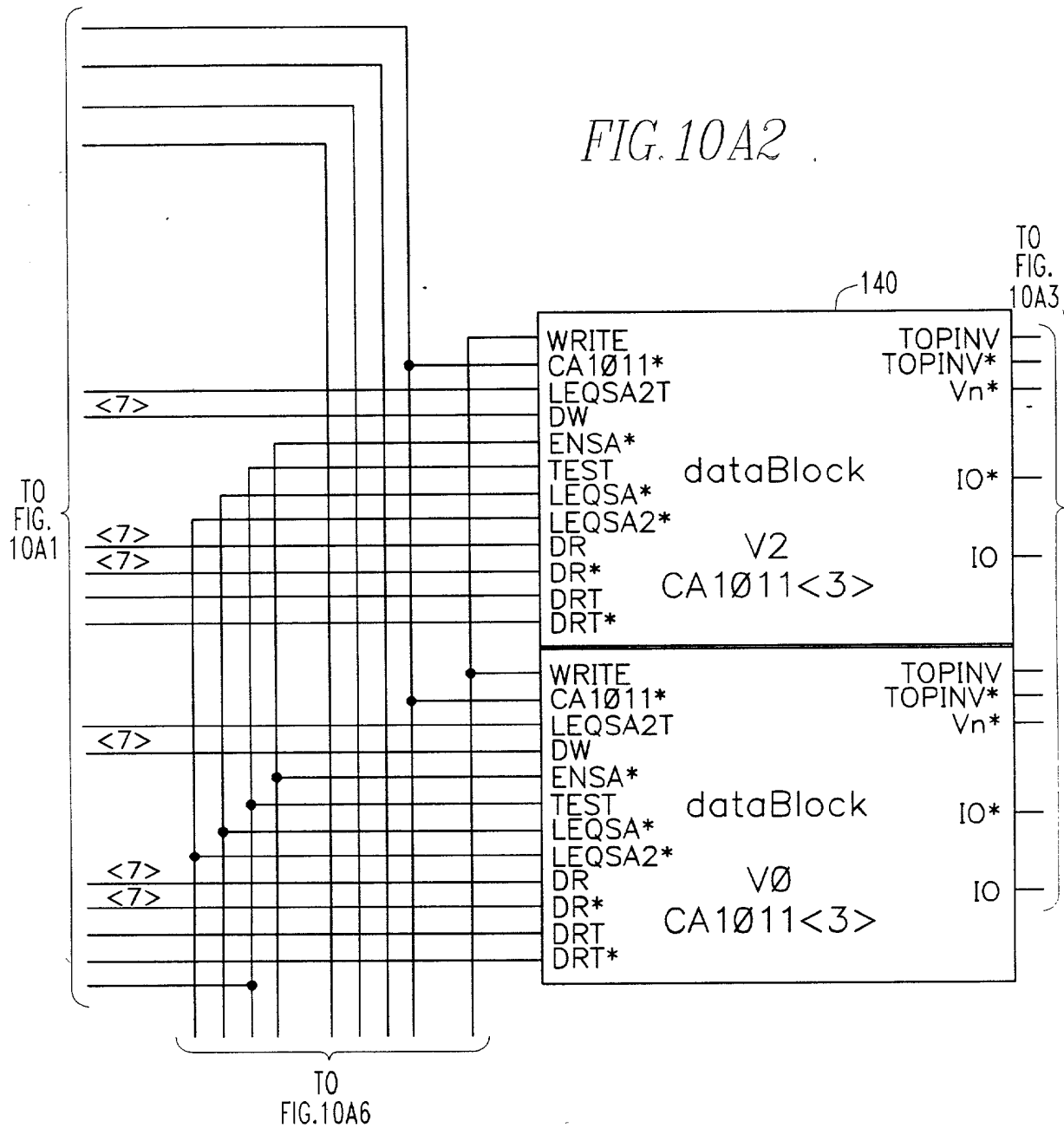
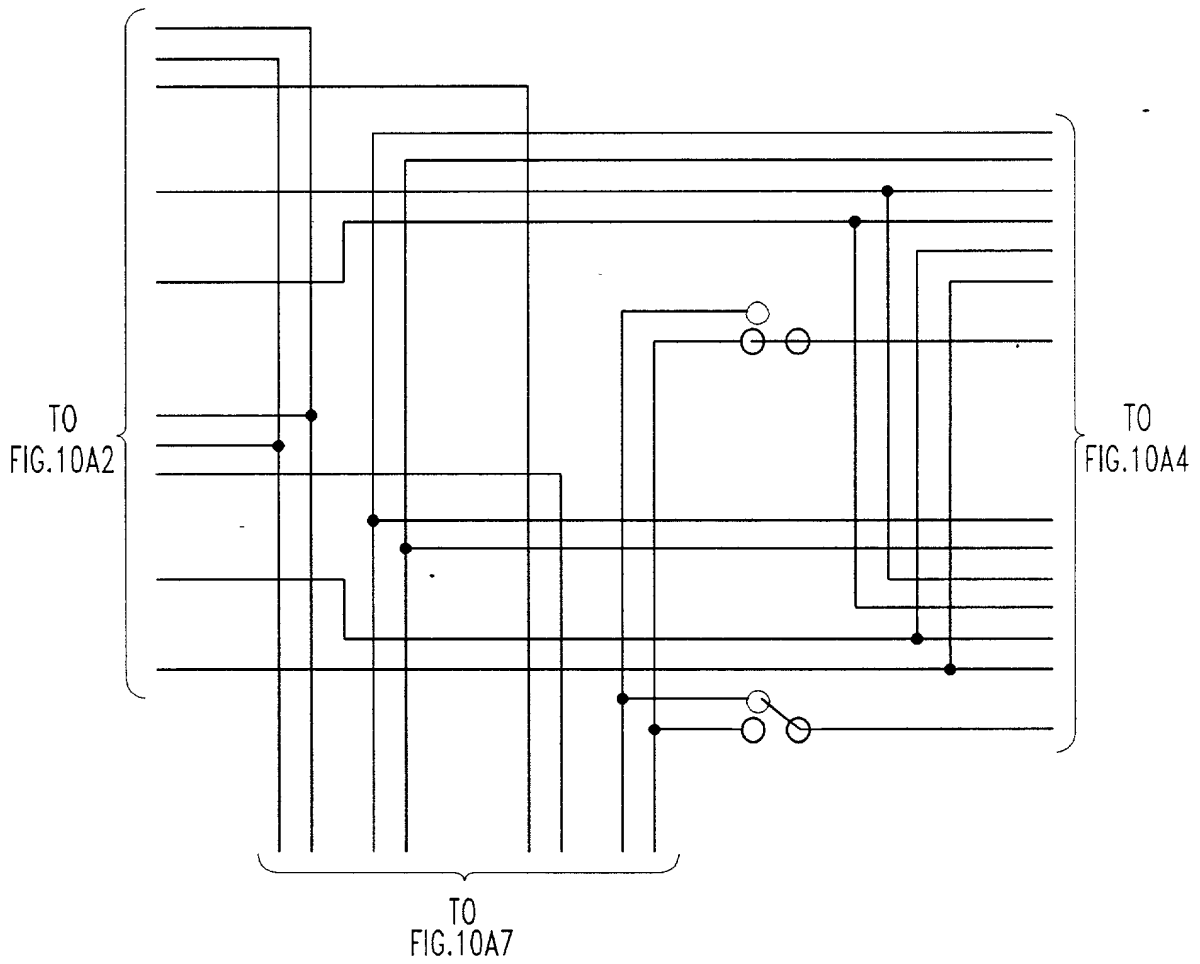


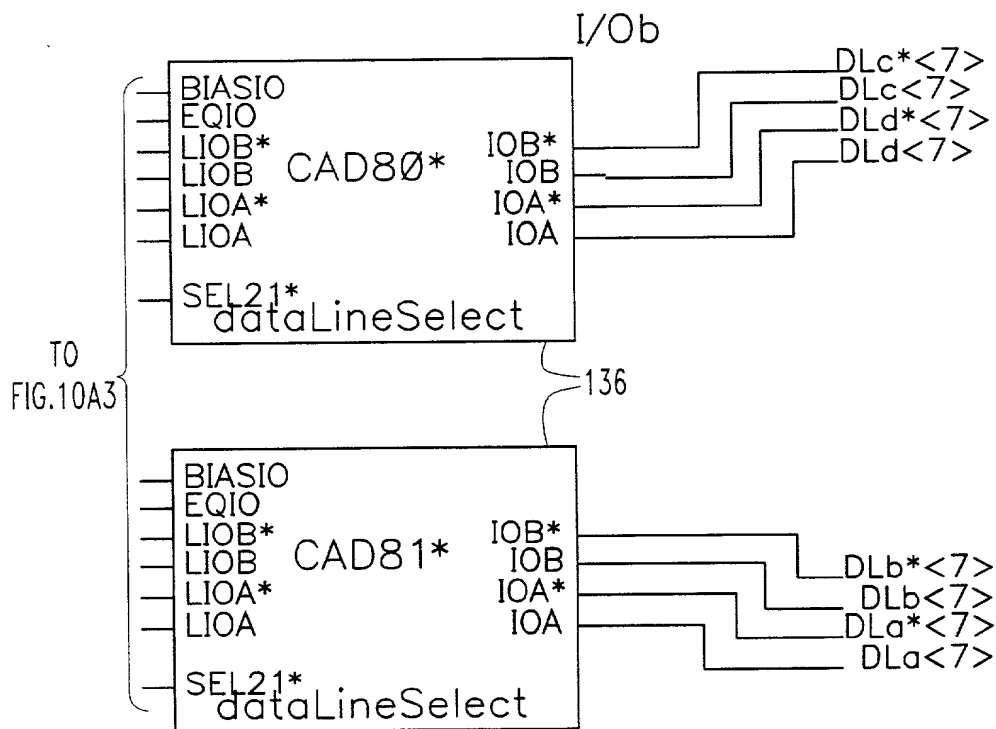
FIG. 10A3



arrayIOBlock

100

FIG. 10A4



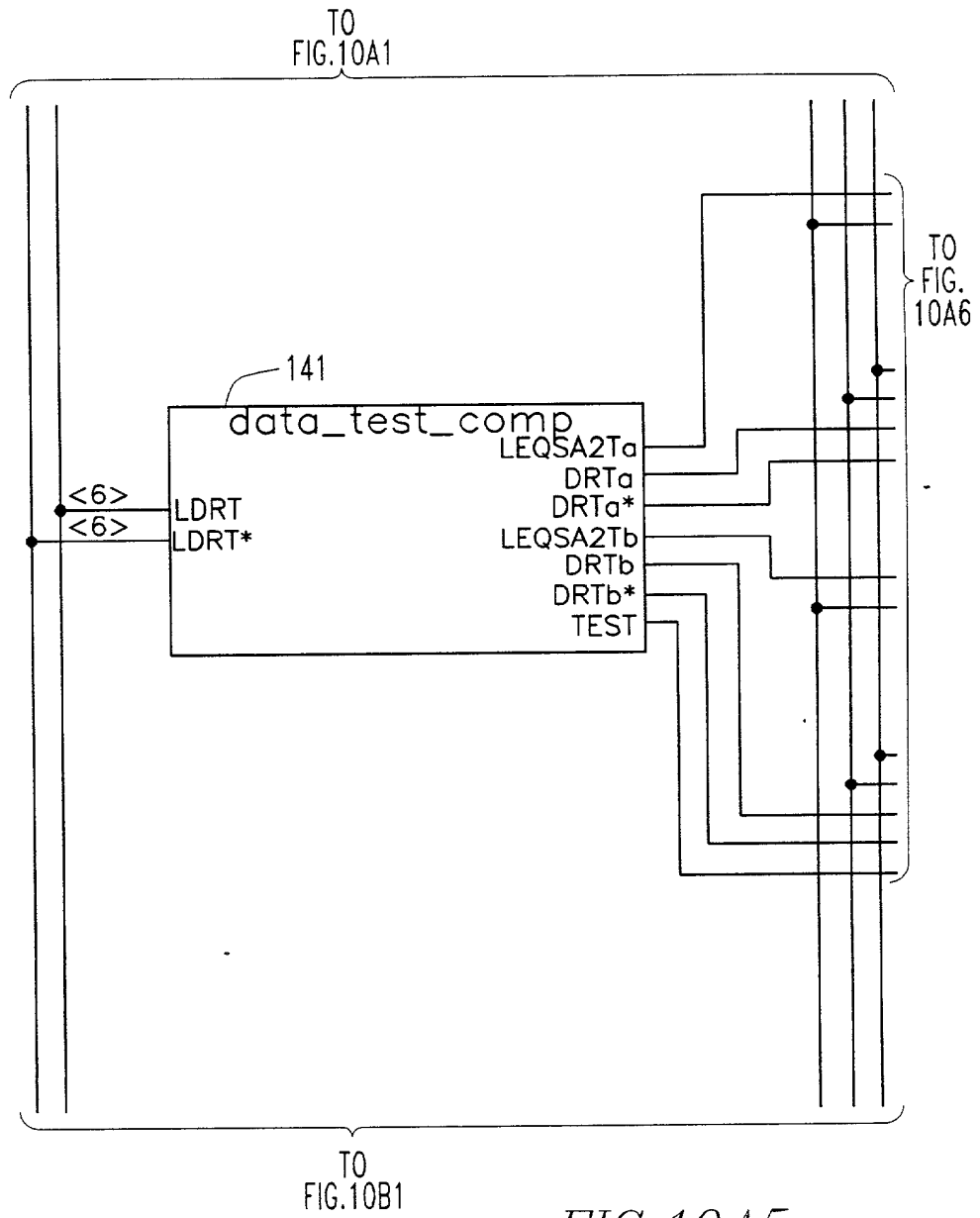
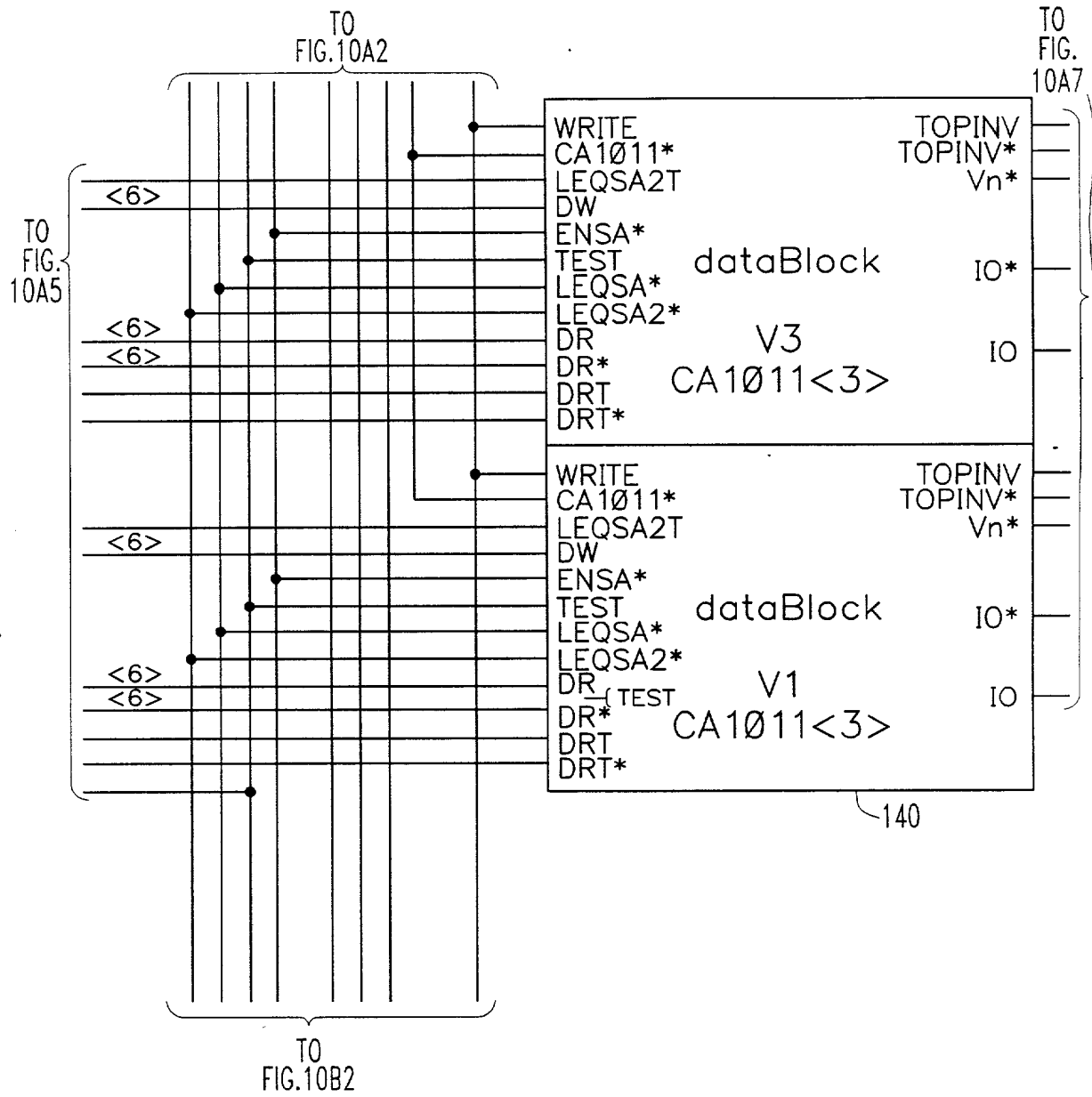


FIG.10A5



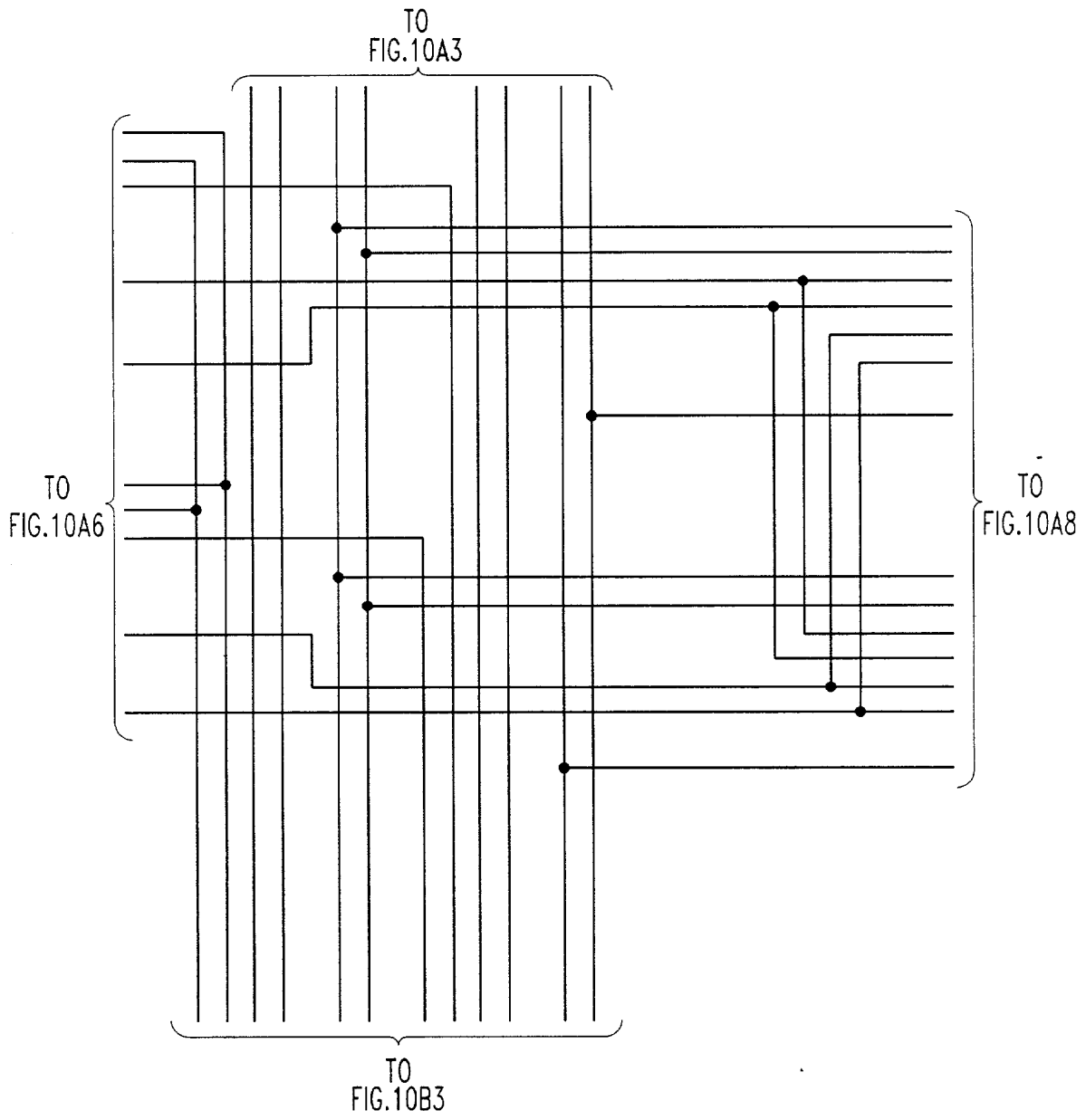


FIG. 10A7

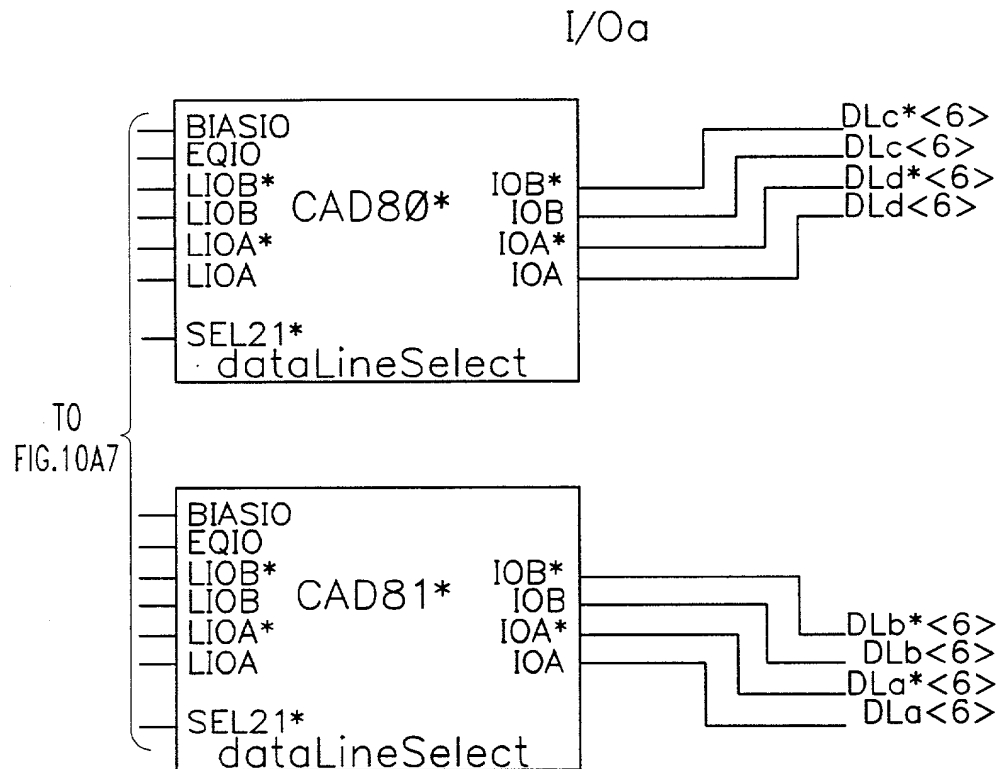


FIG. 10A8

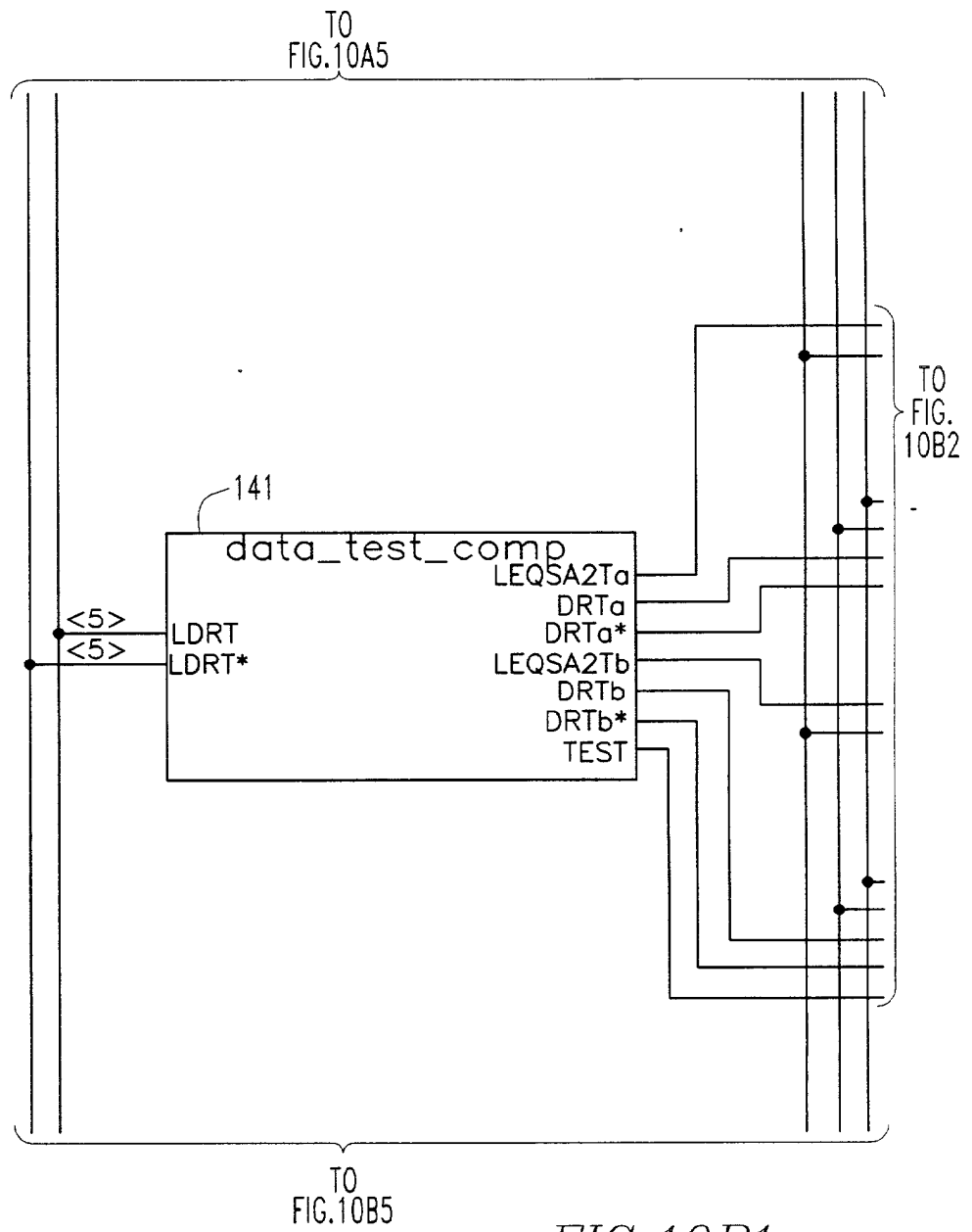


FIG. 10B1

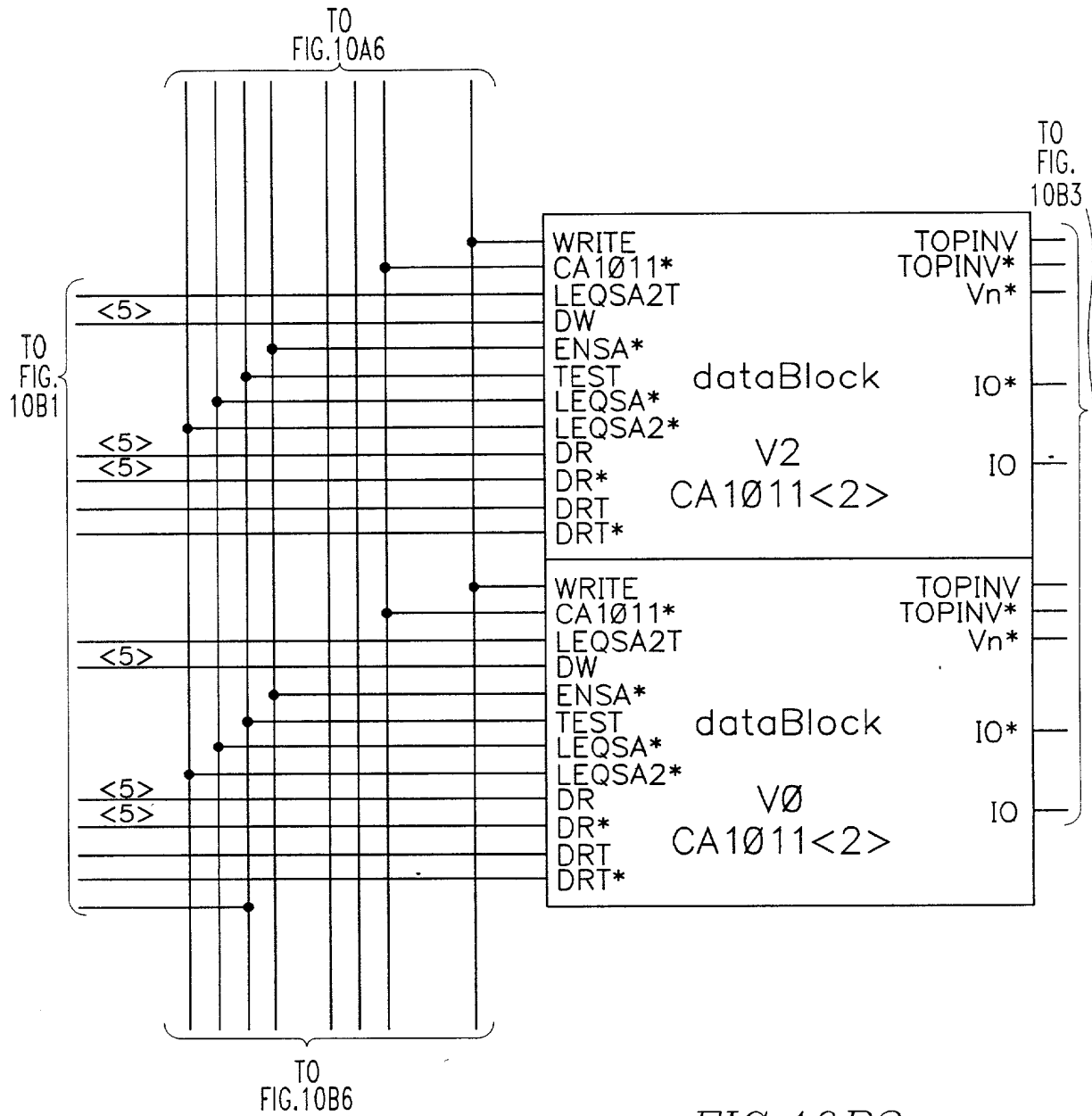


FIG. 10B2

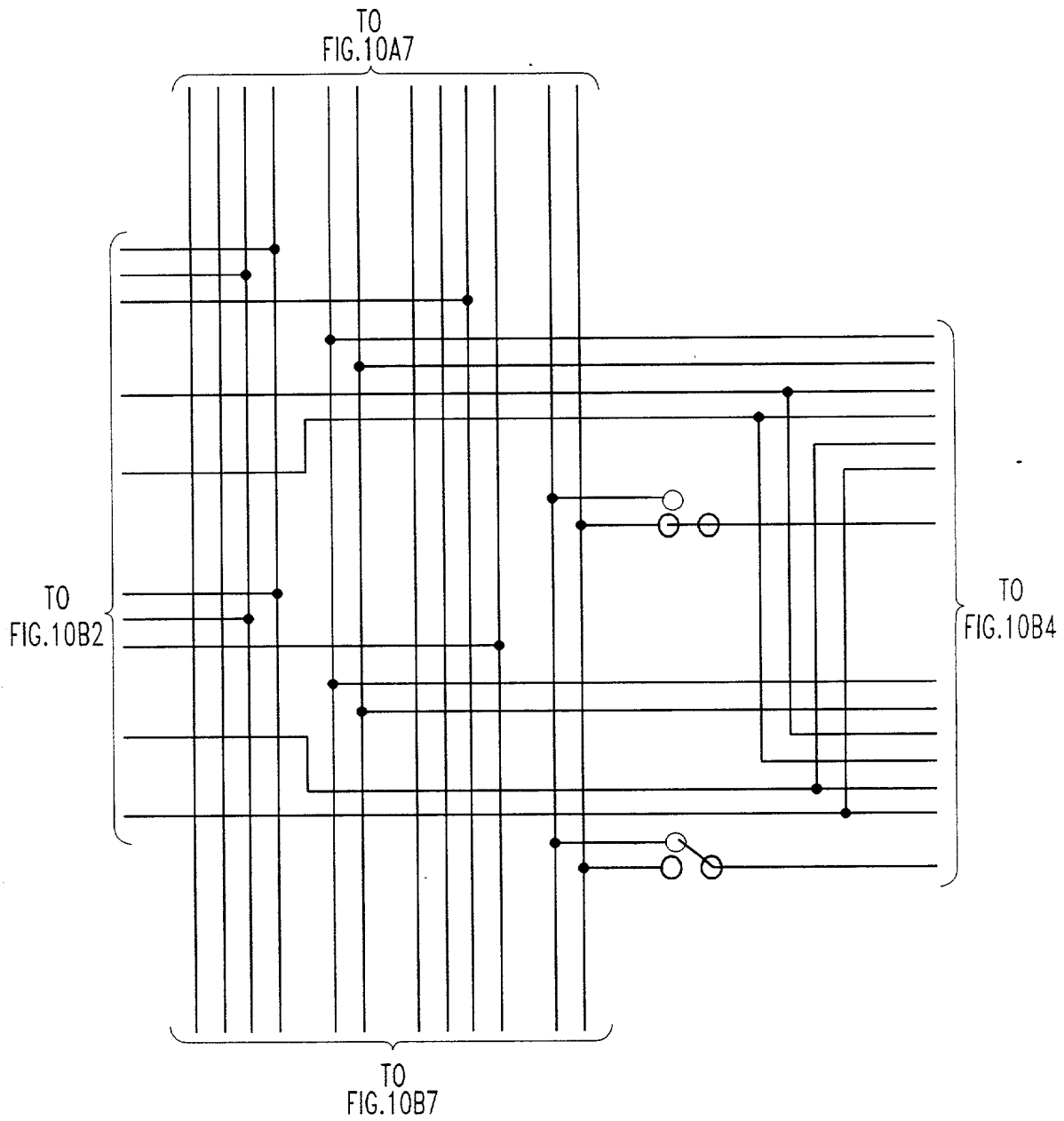


FIG. 10B3

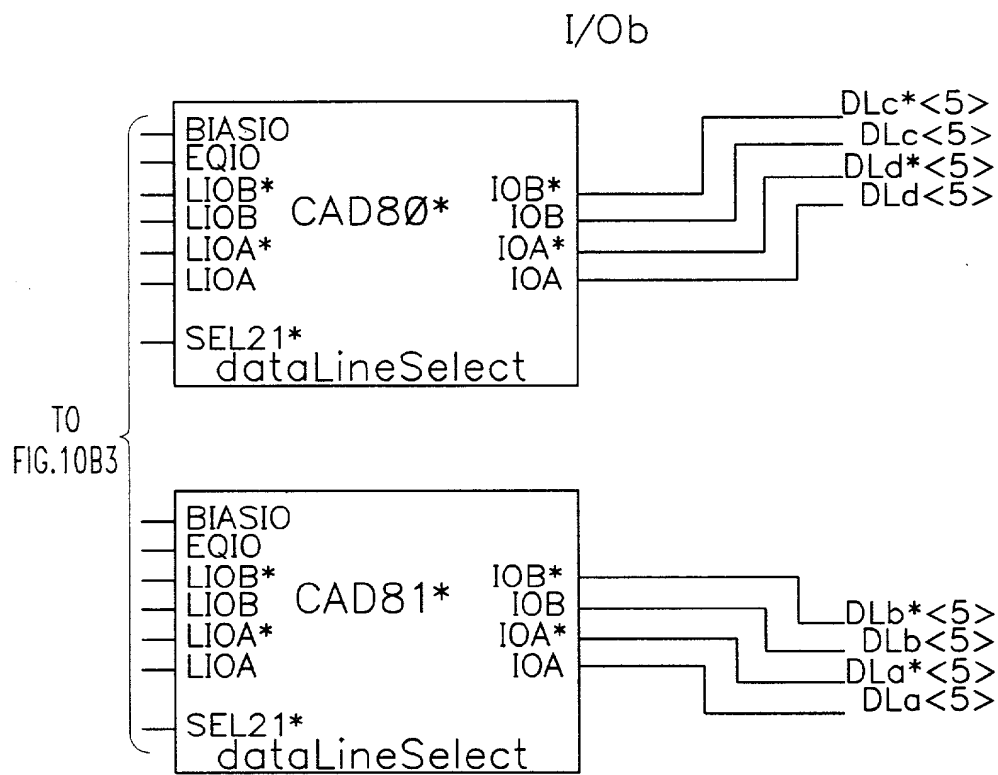


FIG.10B4

FIG. 10B5

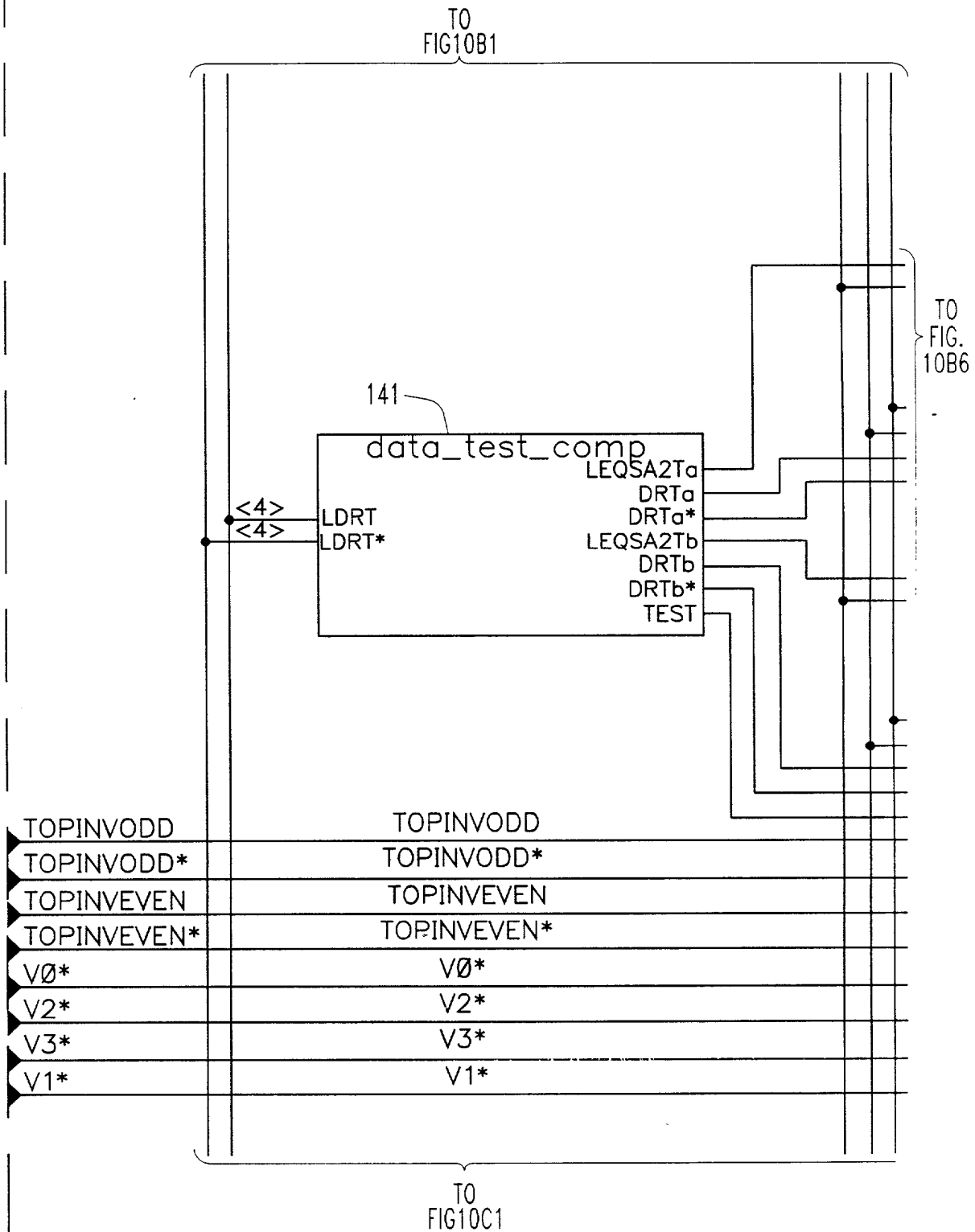


FIG. 10B6

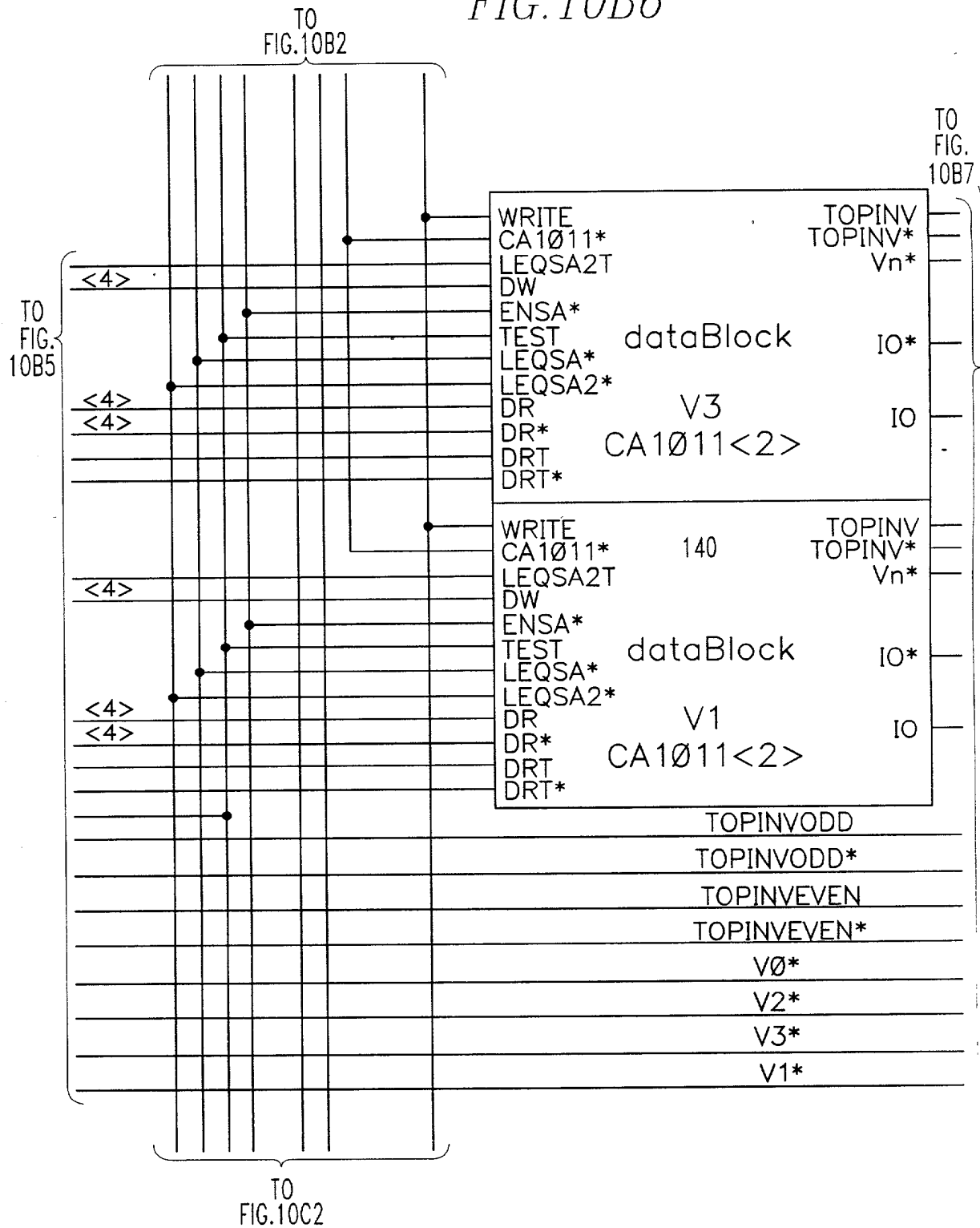


FIG. 10B7

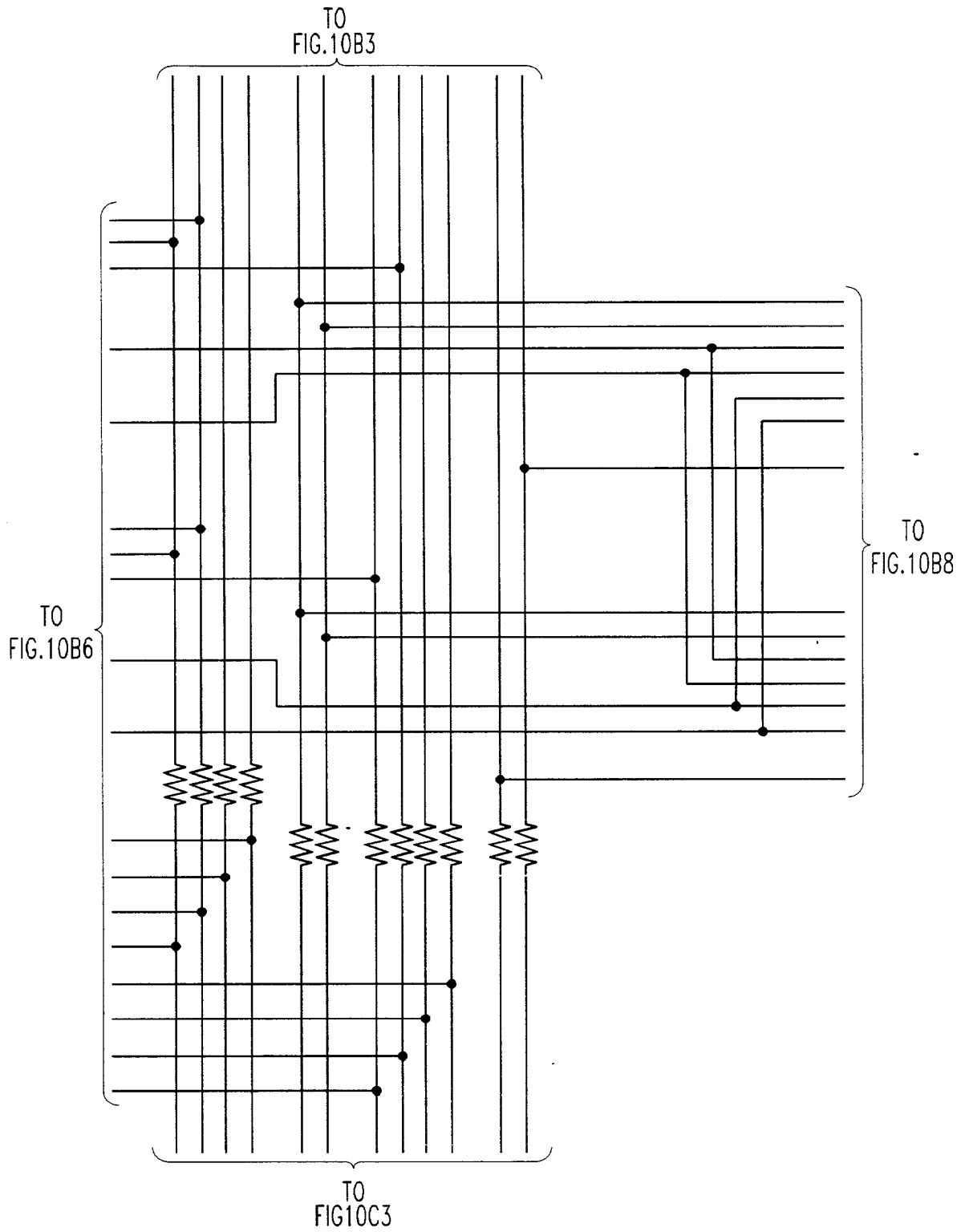
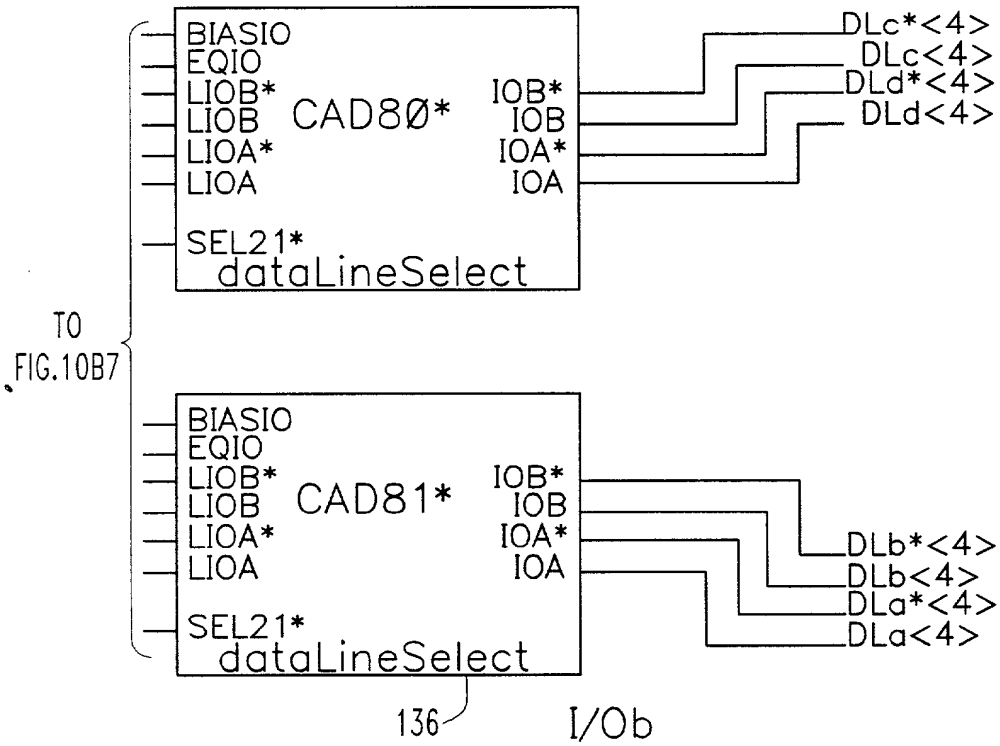


FIG. 10B8

I/Oa



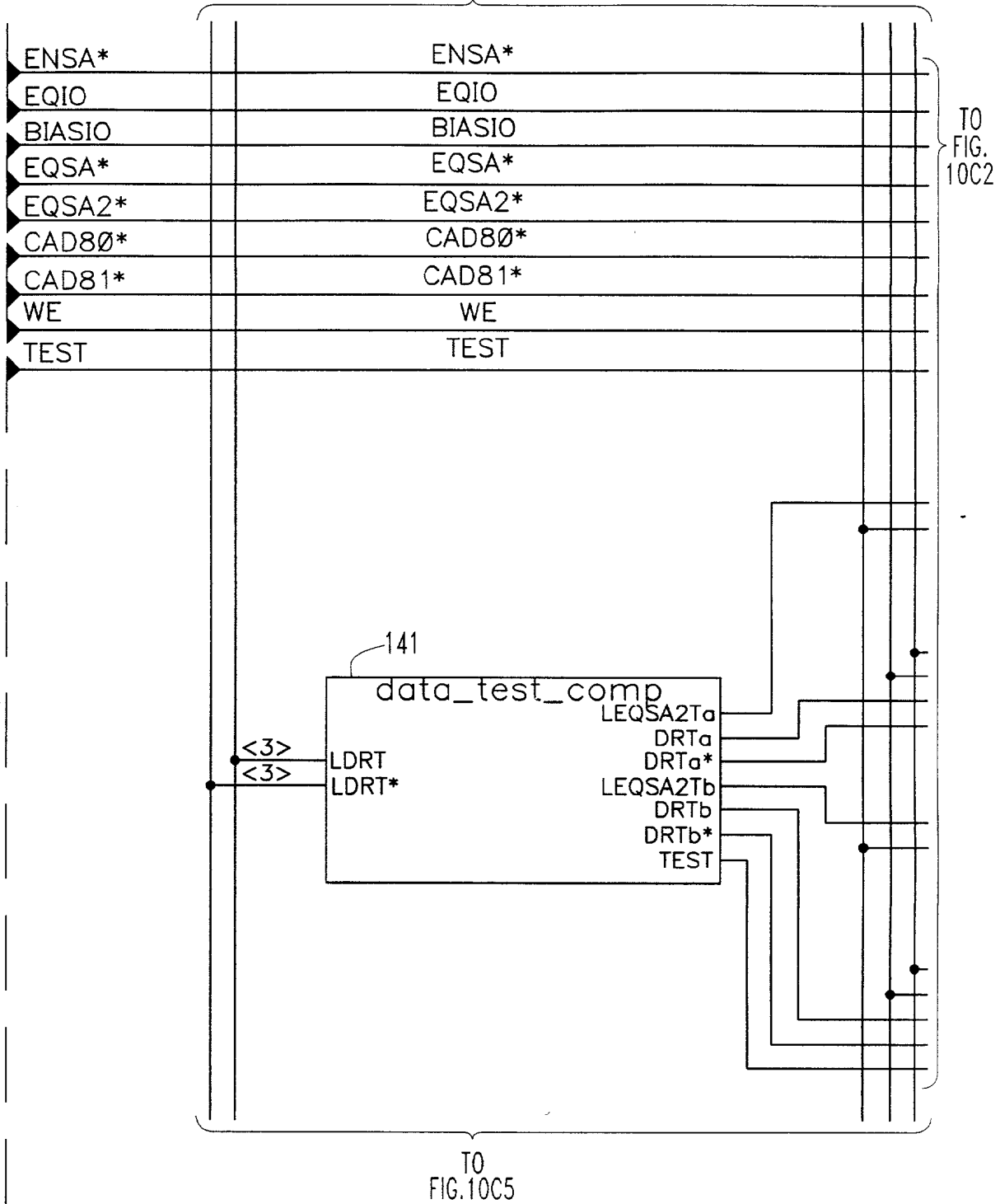
TO
FIG. 10B5

FIG. 10C1

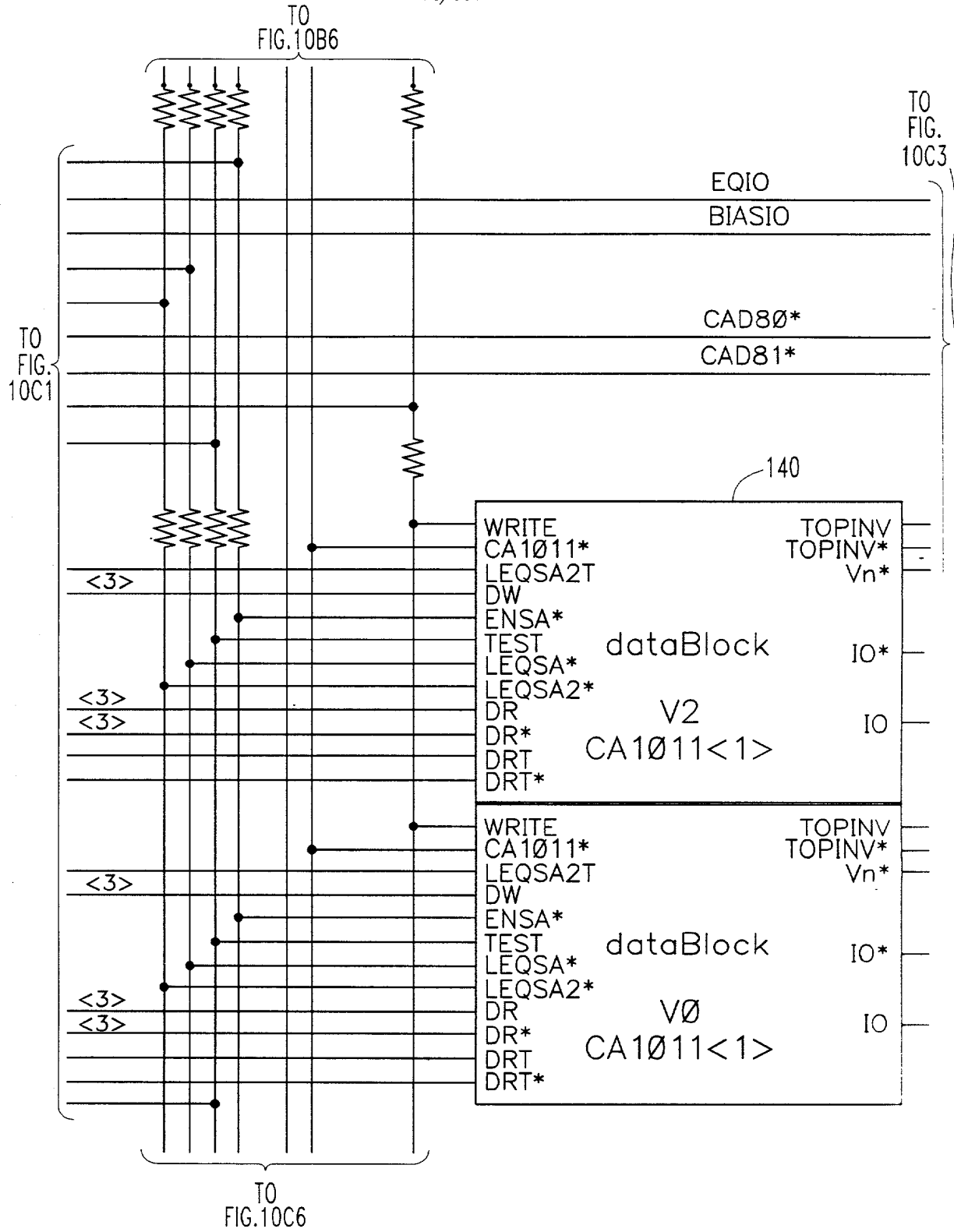


FIG. 10C2

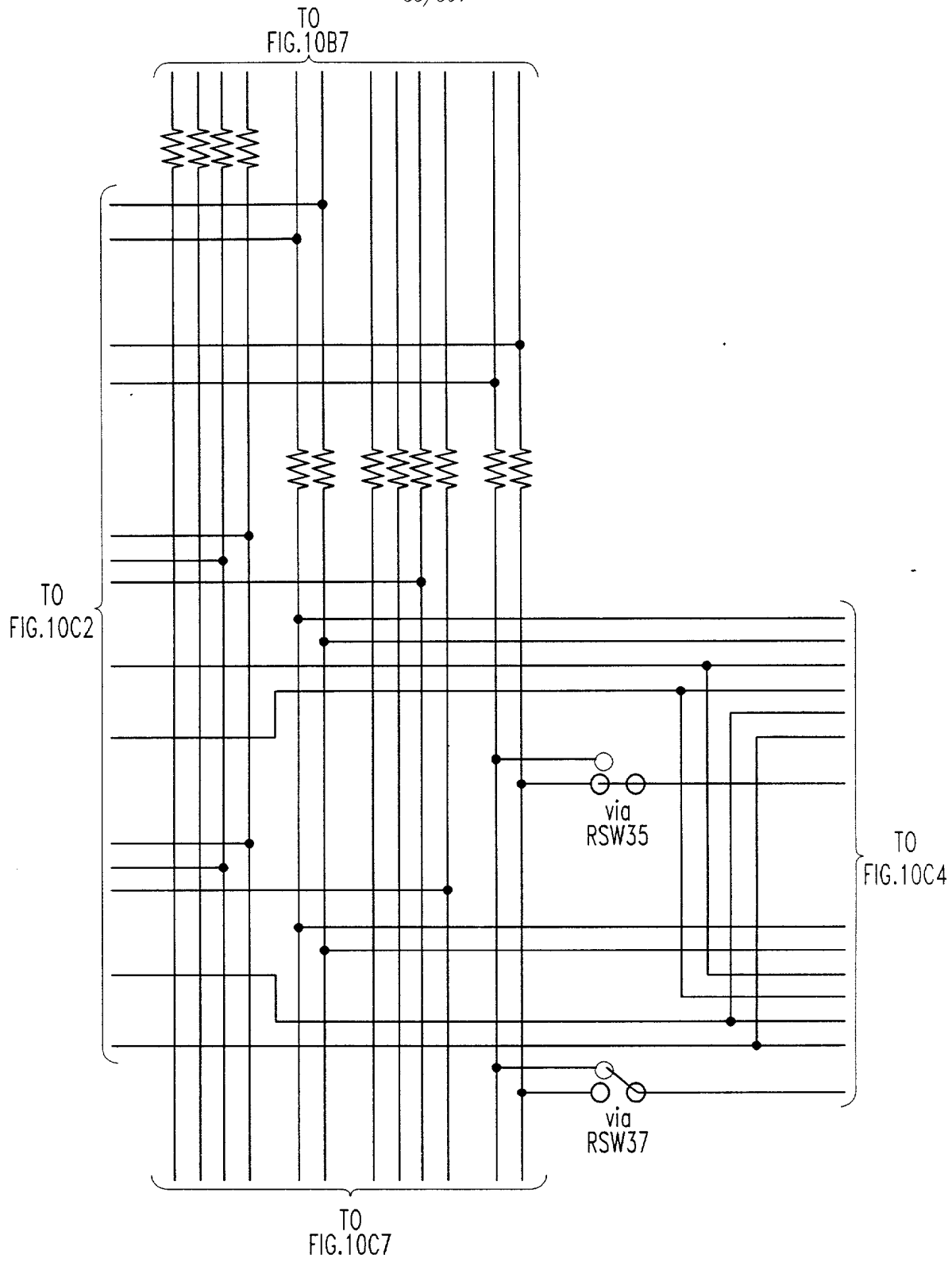
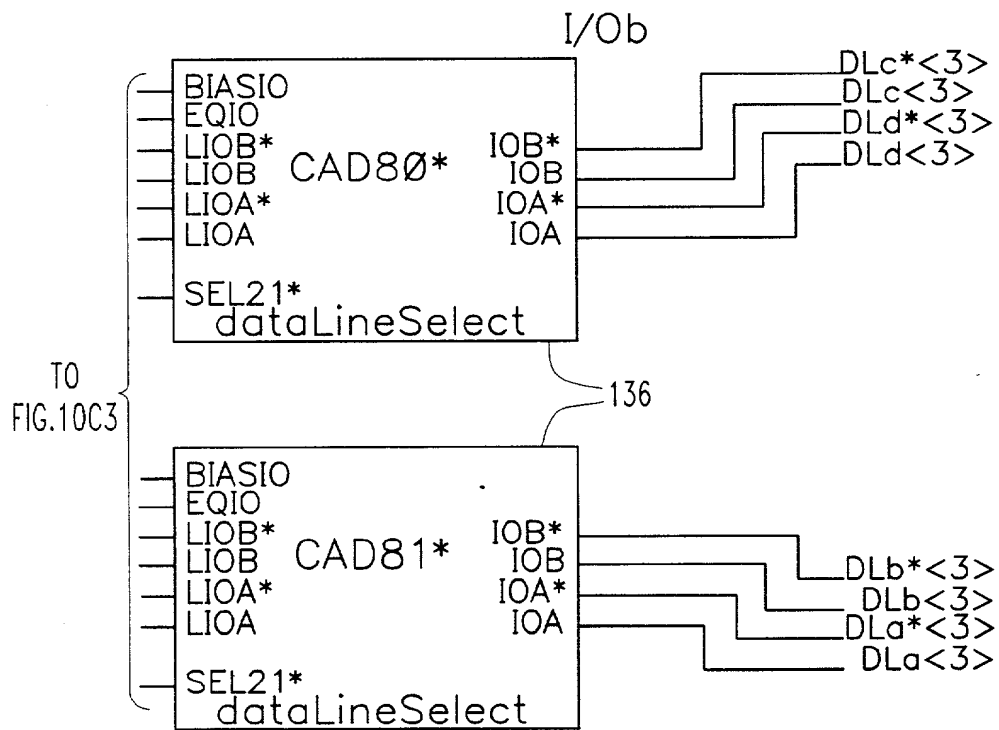


FIG. 10C3

FIG. 10C4



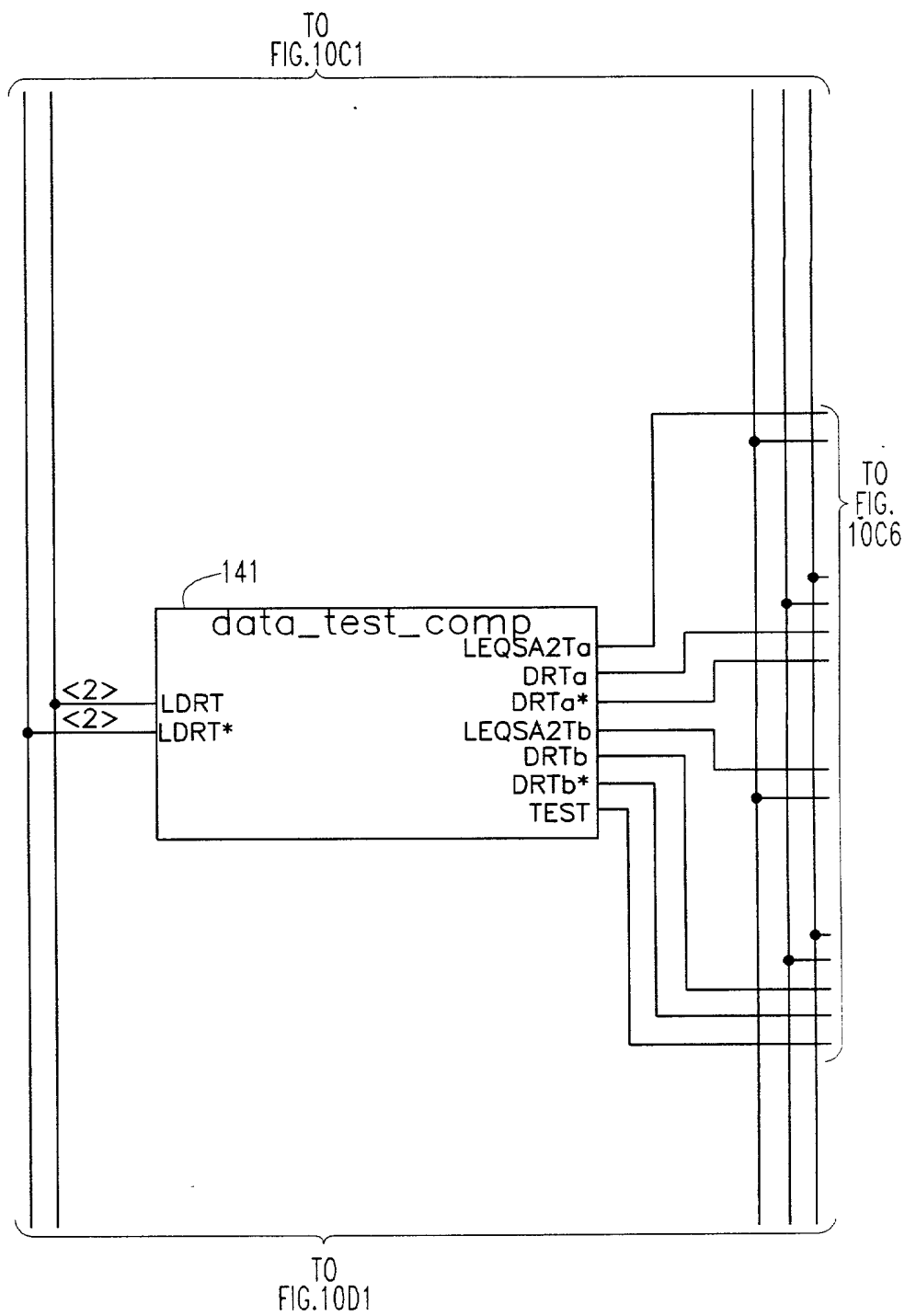


FIG. 10C5

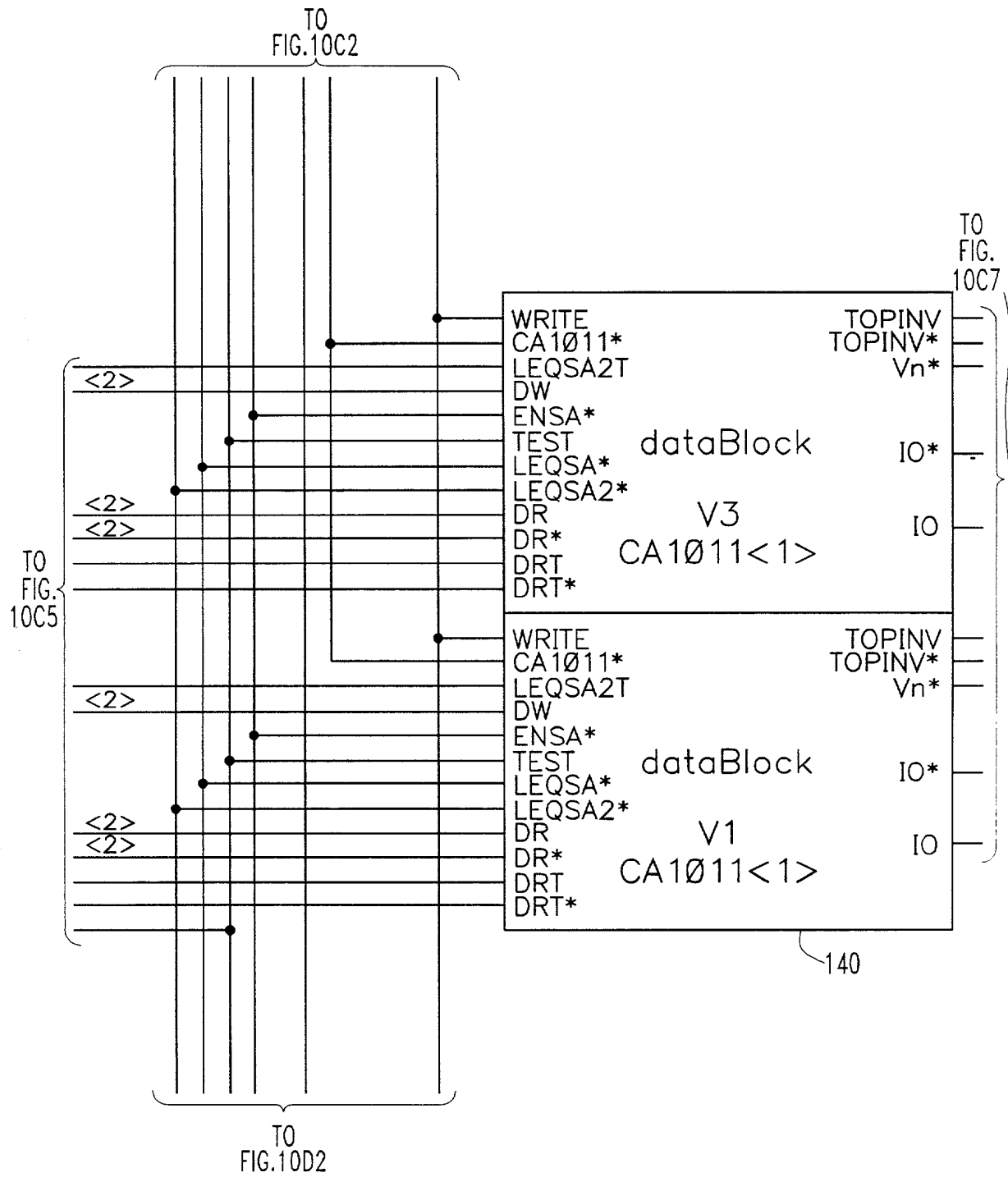


FIG. 10C6

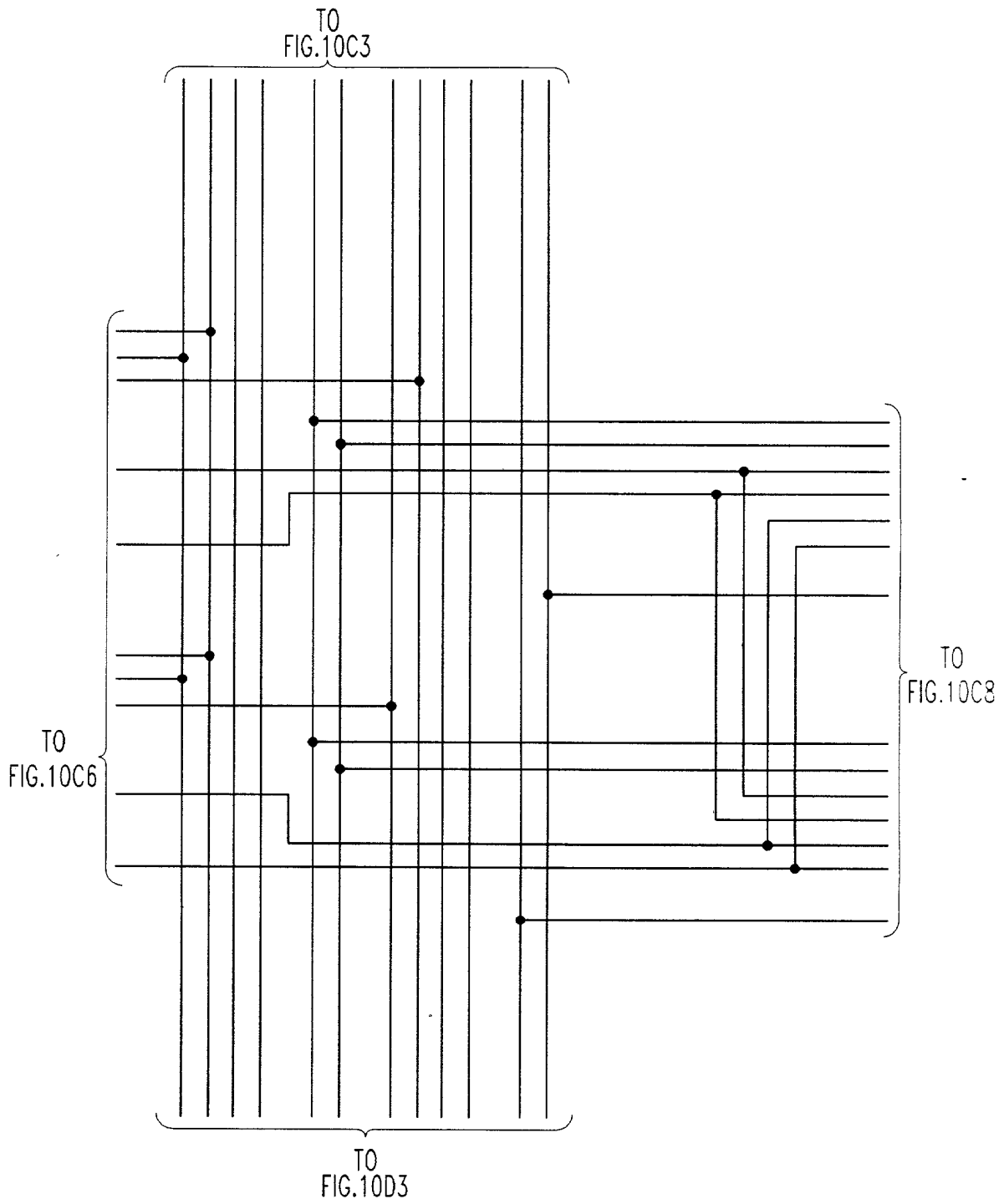


FIG.10C7

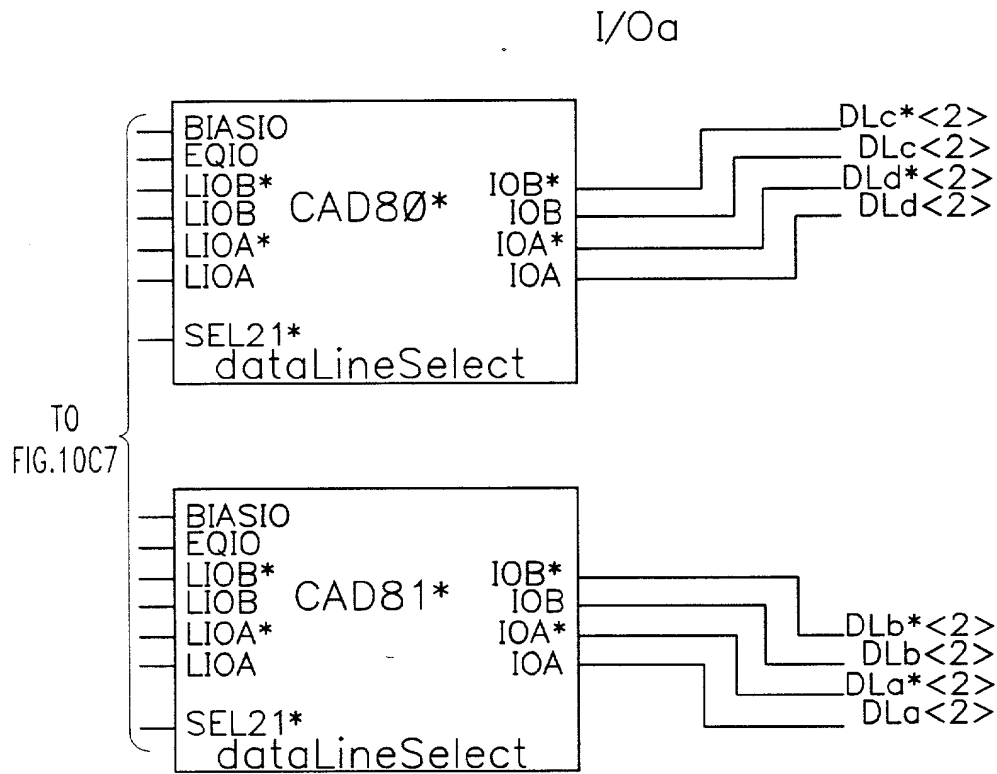


FIG.10C8

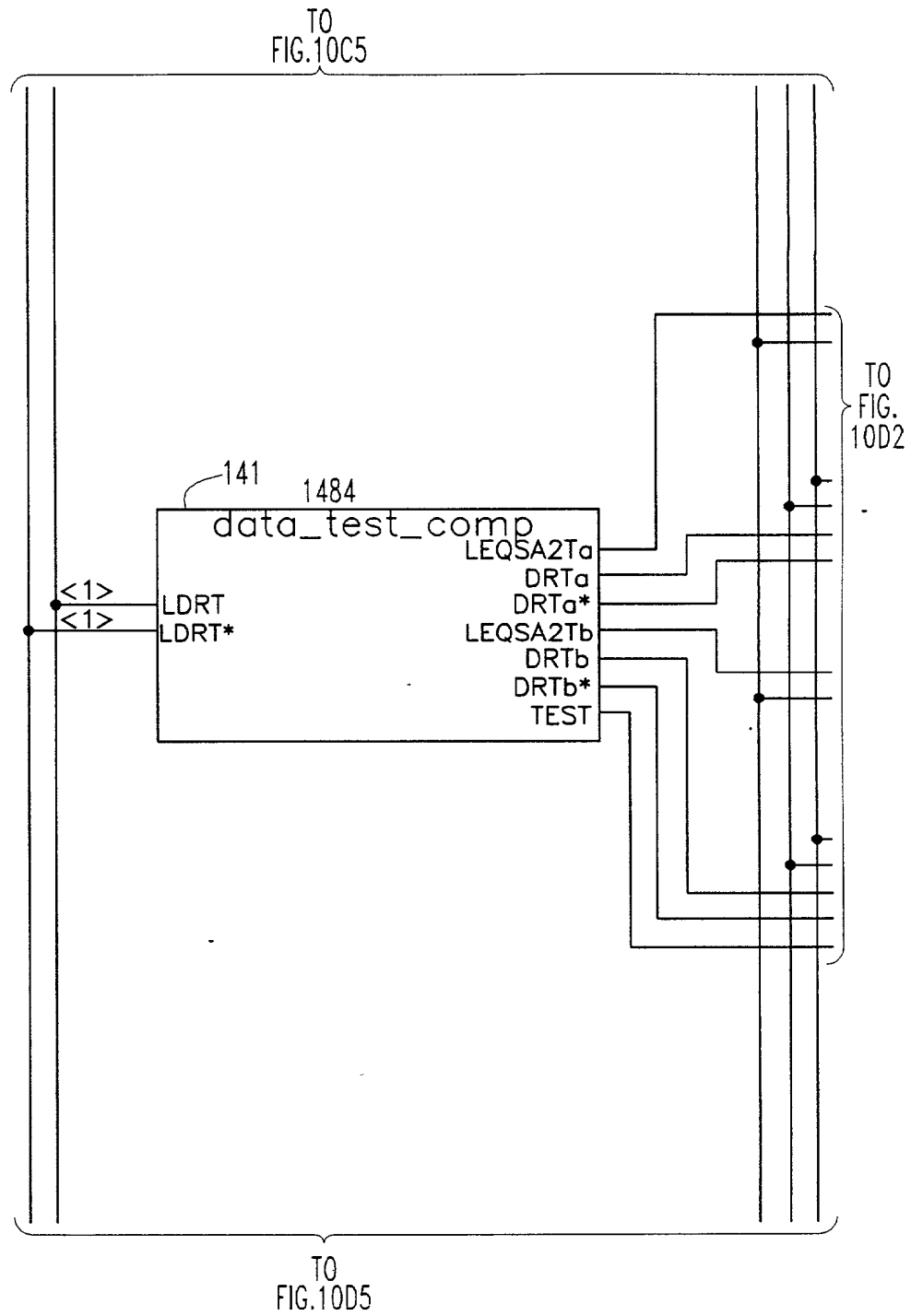


FIG.10D1

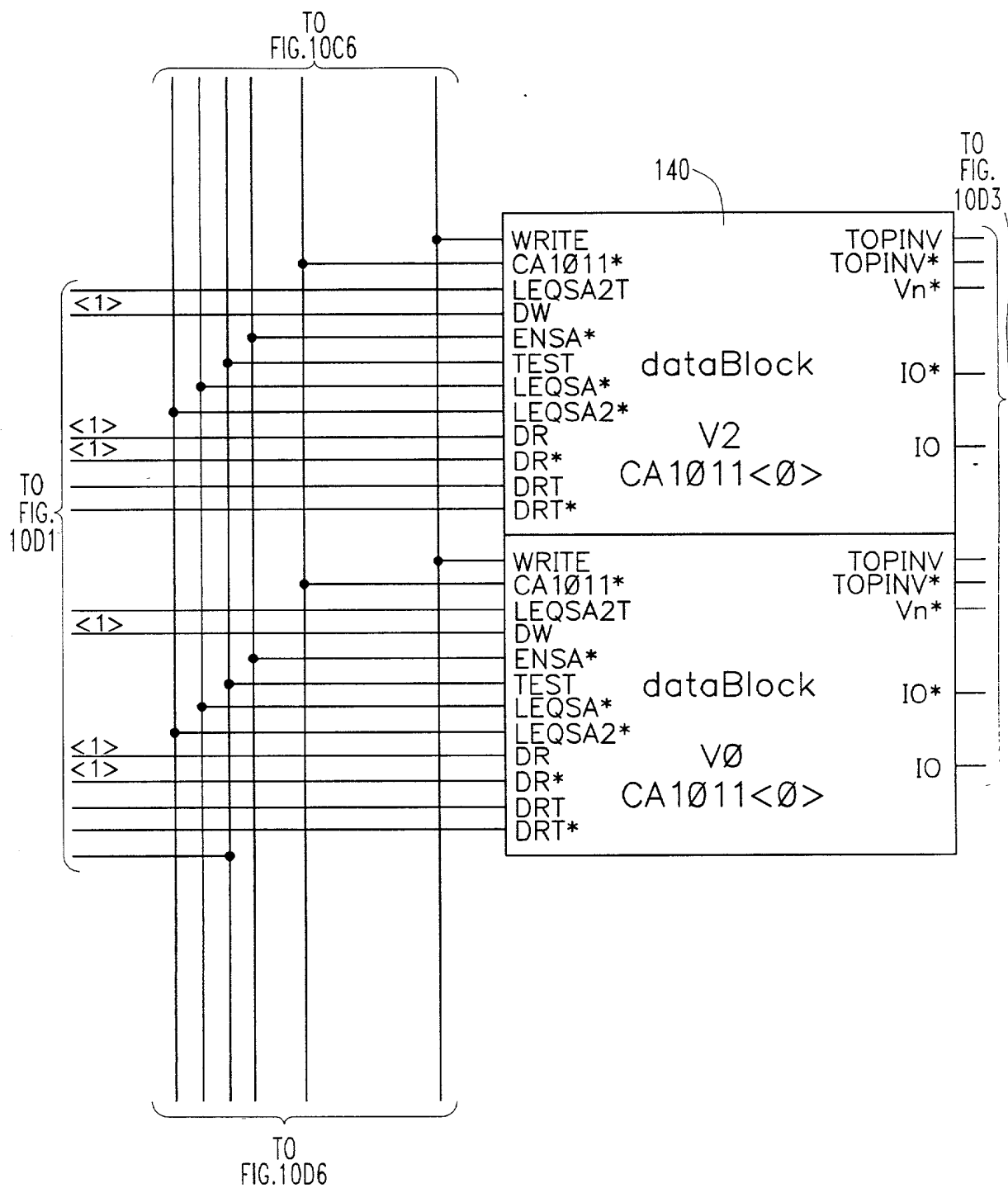


FIG. 10D2

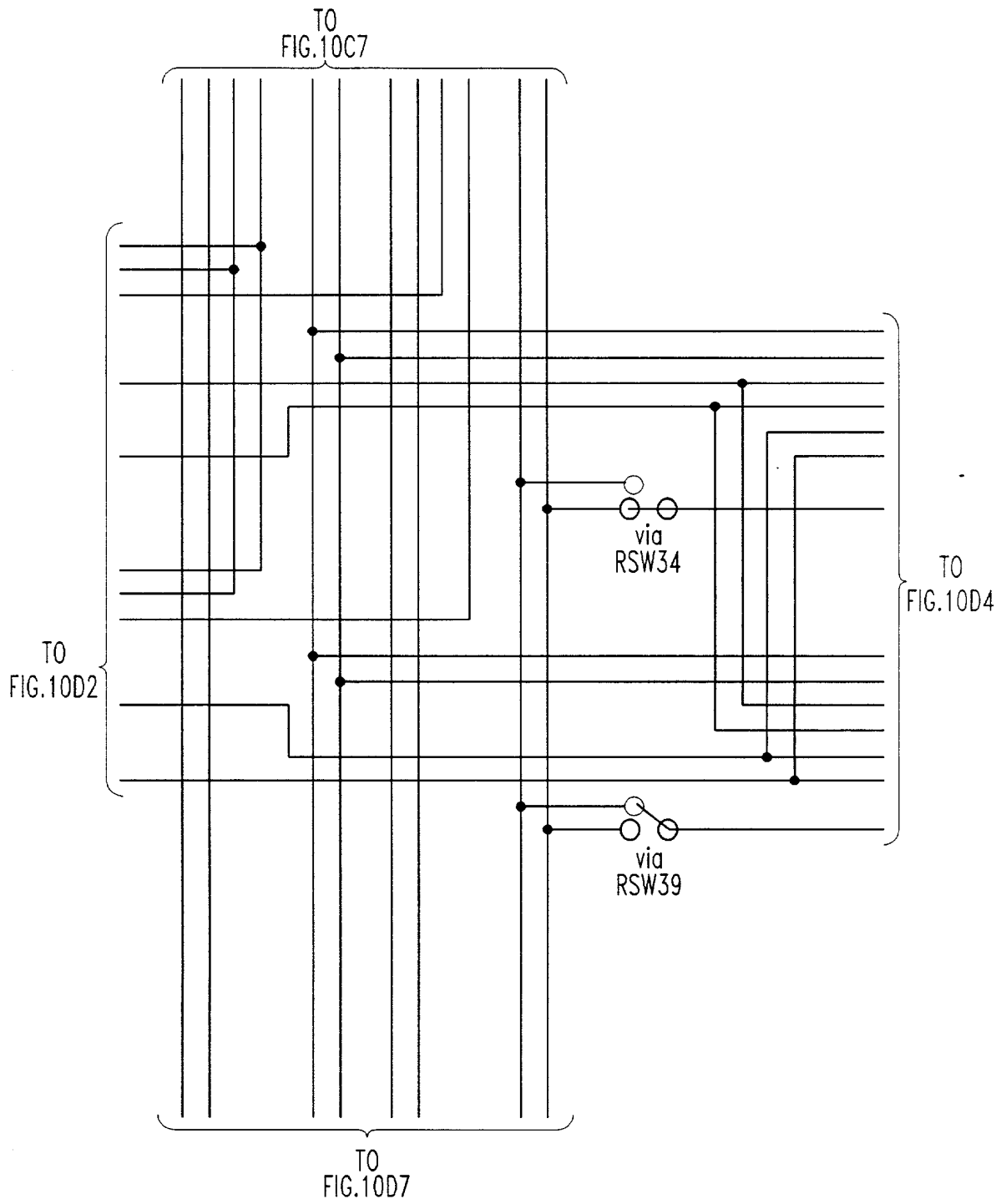


FIG. 10D3

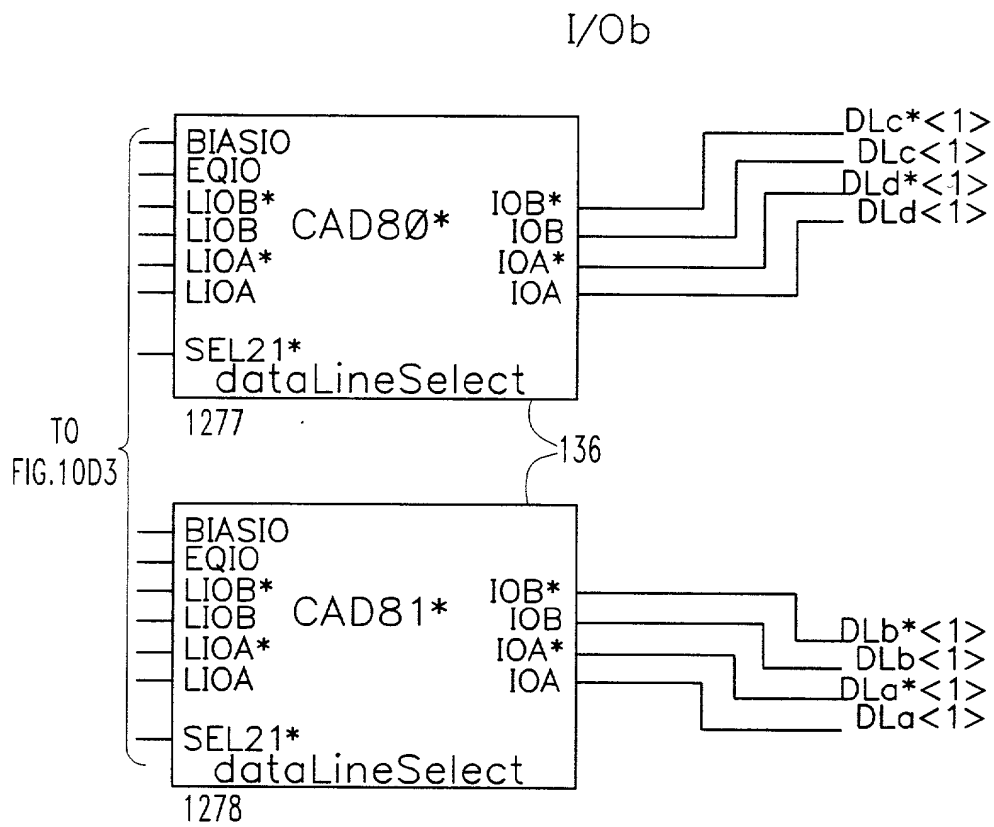


FIG.10D4

TO
FIG. 10D1

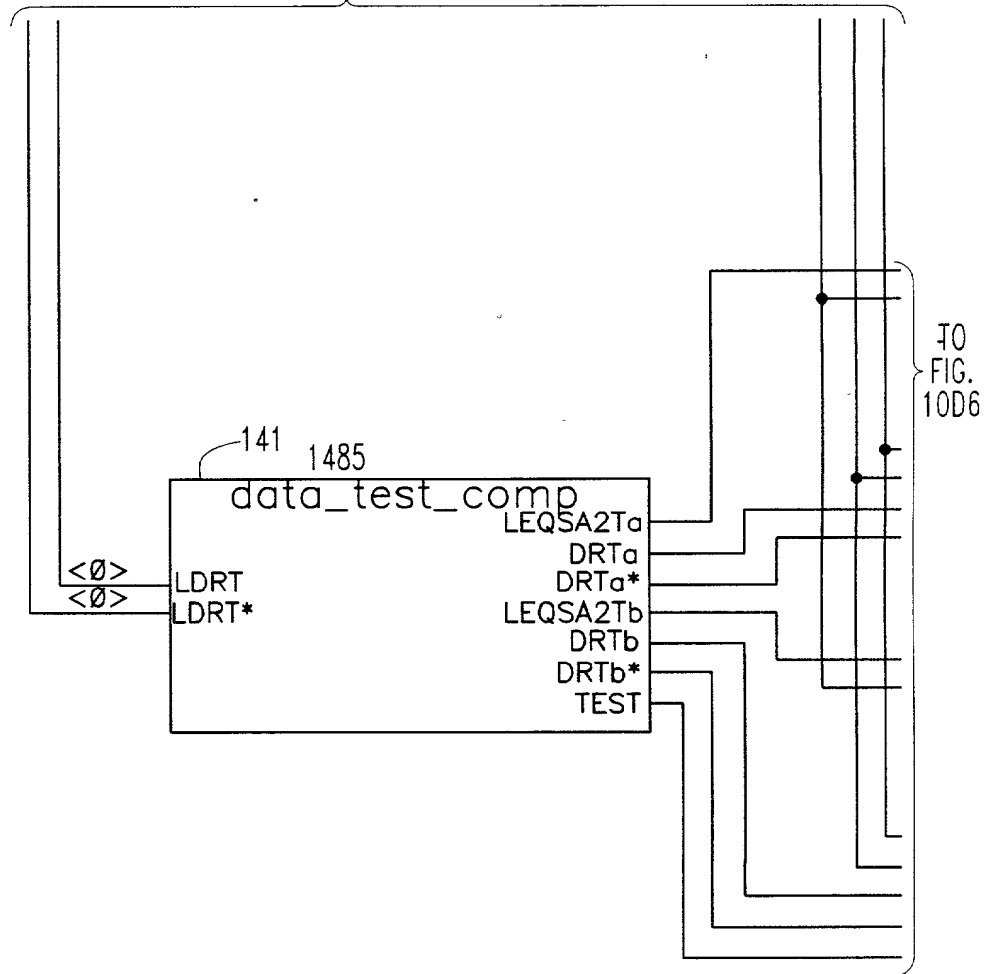


FIG. 10D5

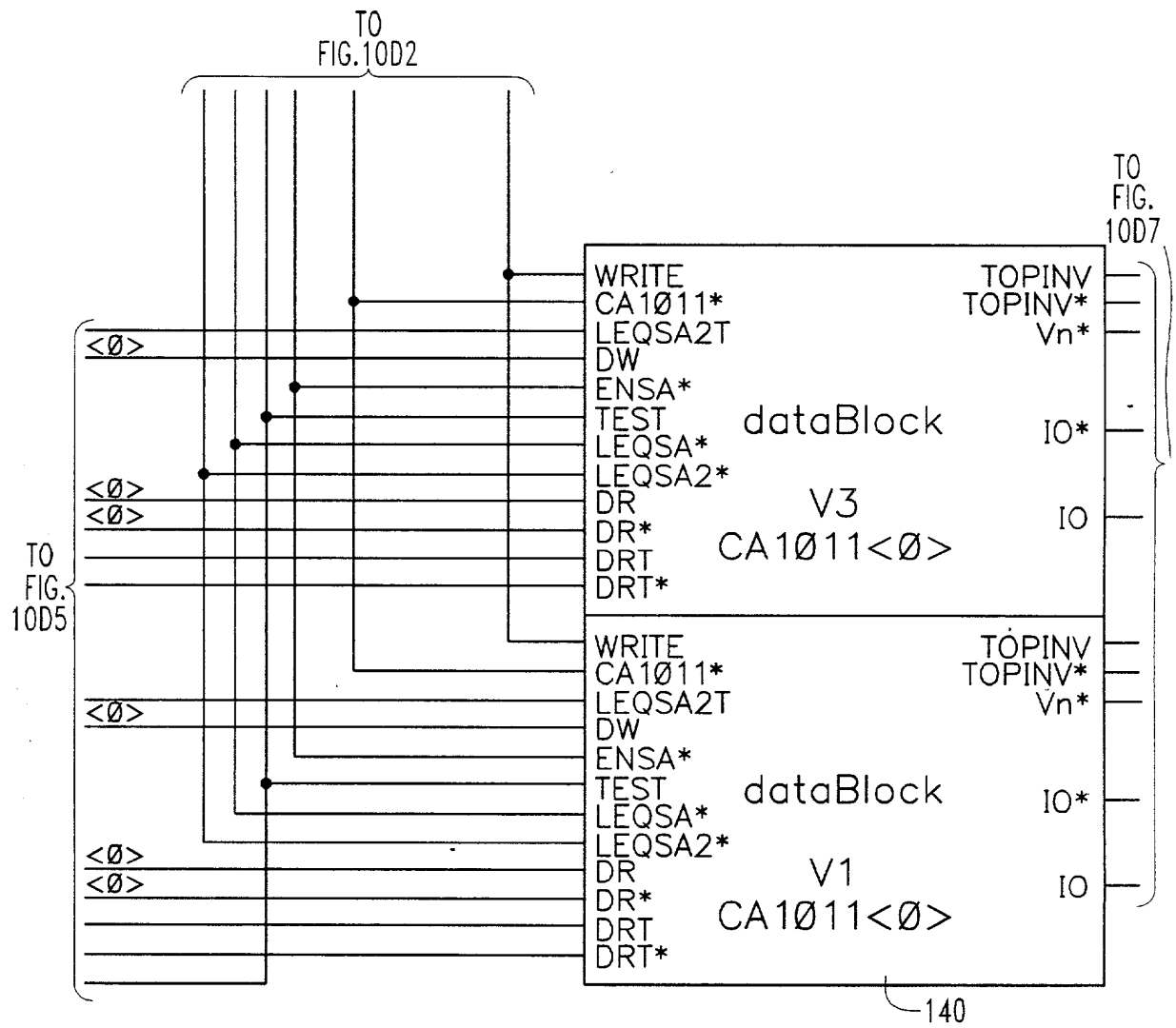


FIG. 10D6



FIG. 10D7

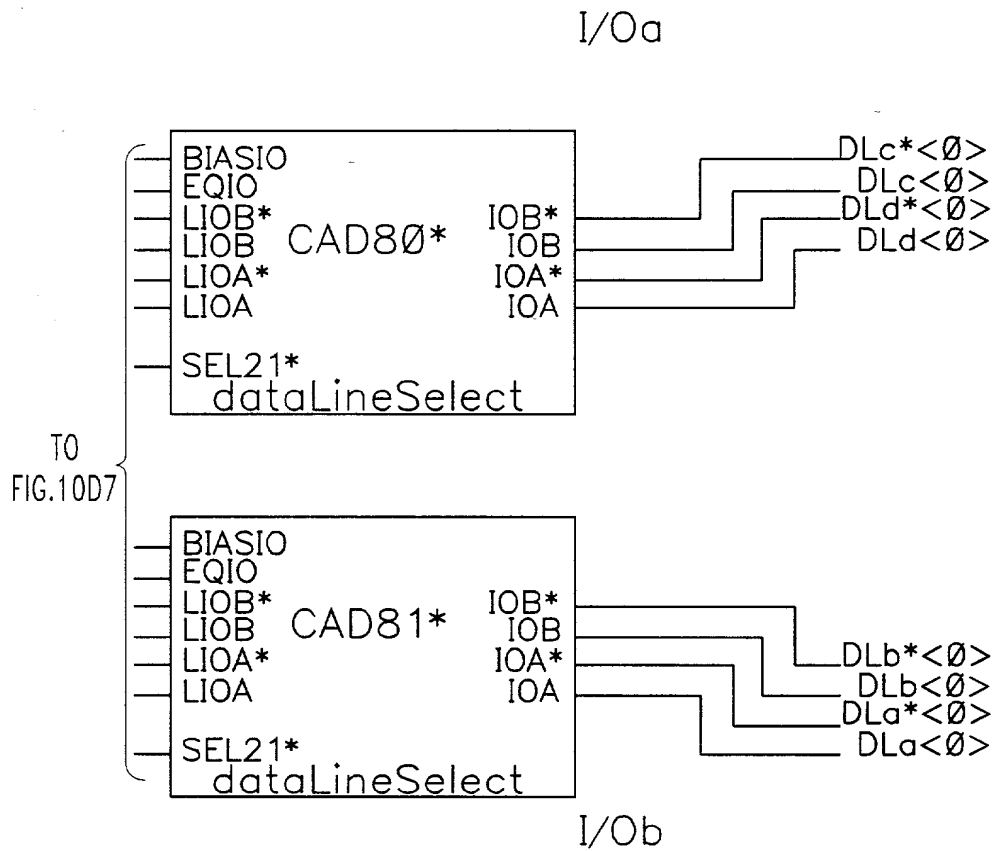


FIG. 10D8

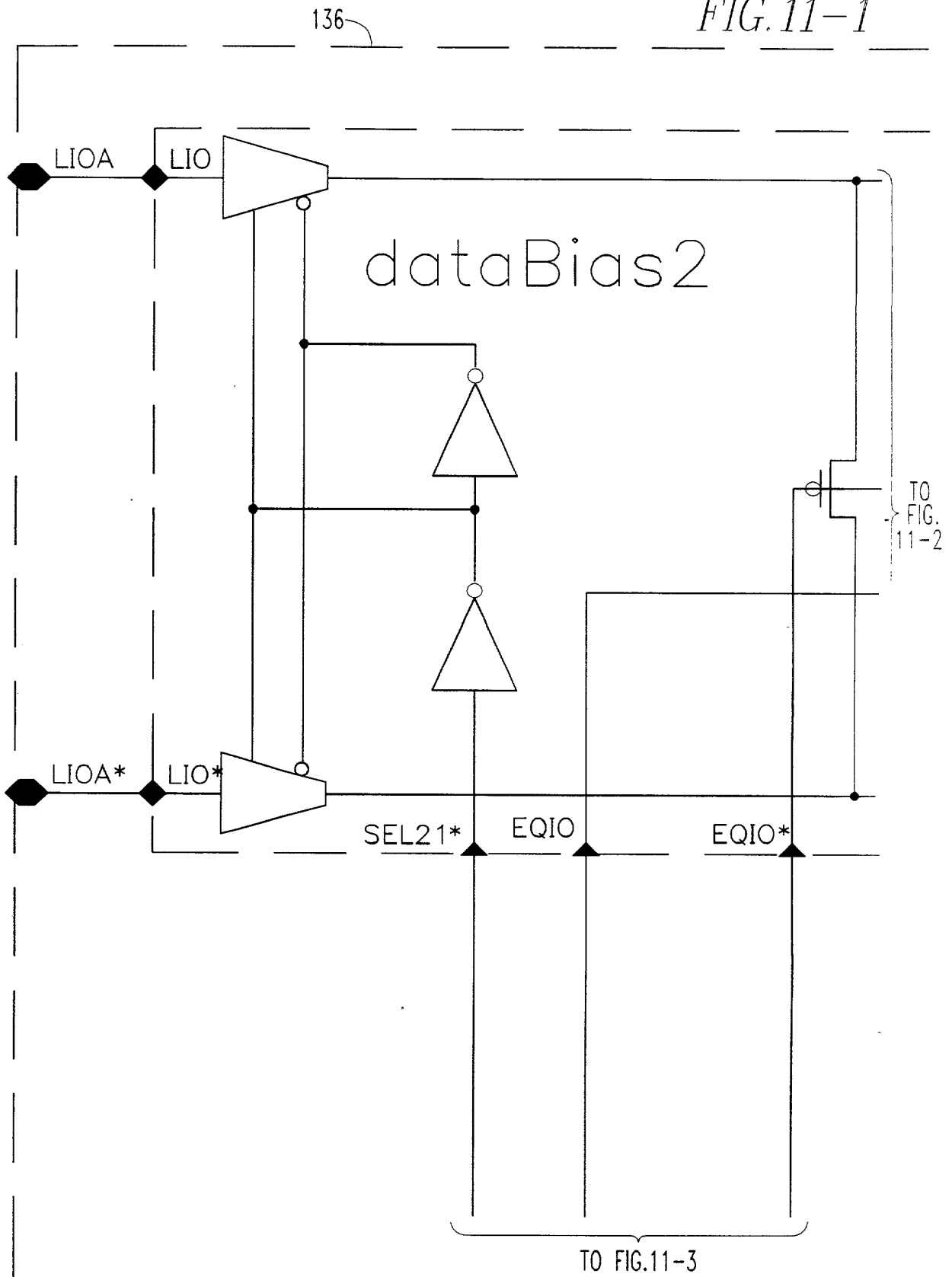
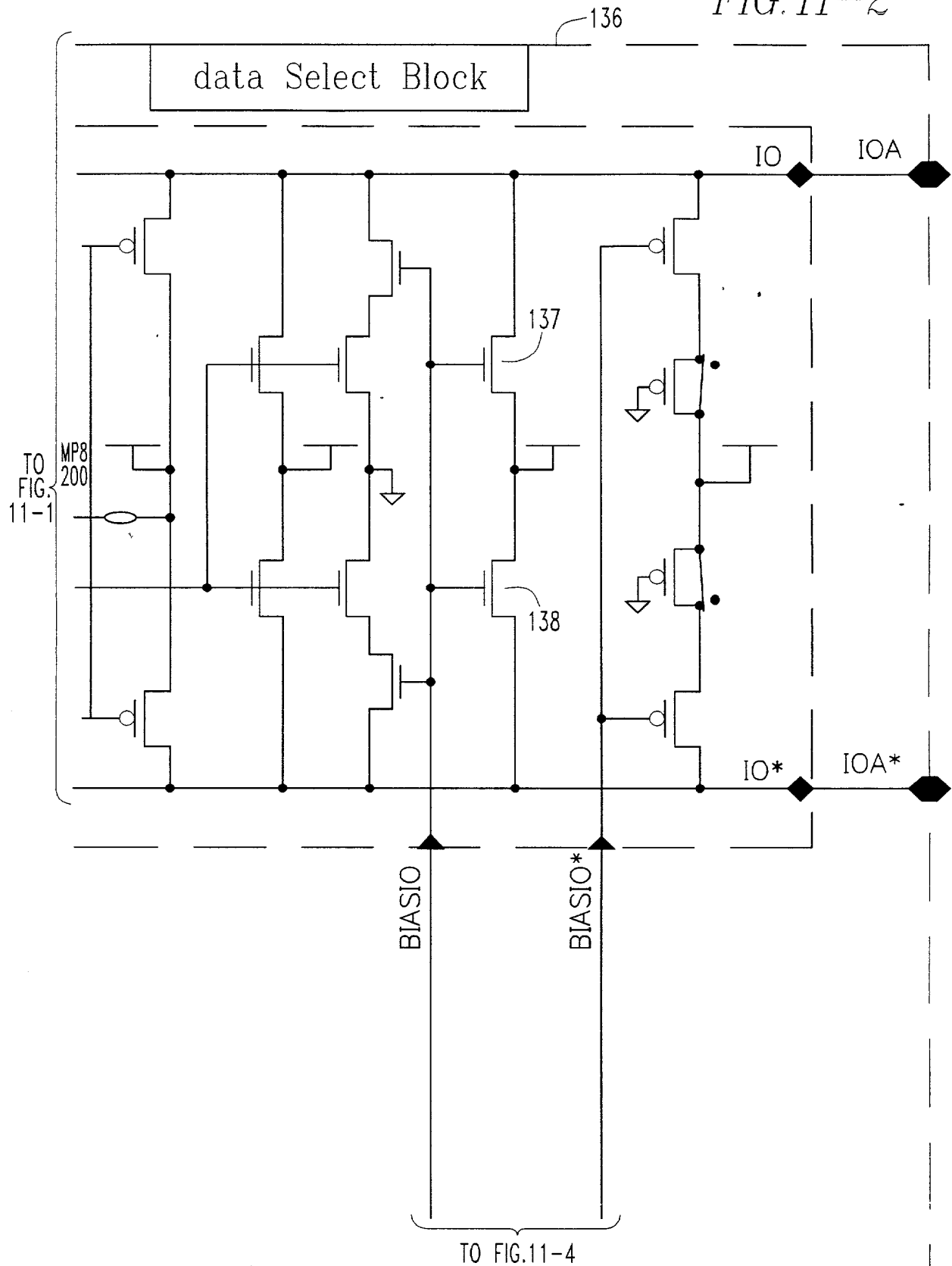


FIG. 11-2



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TO FIG.11-1

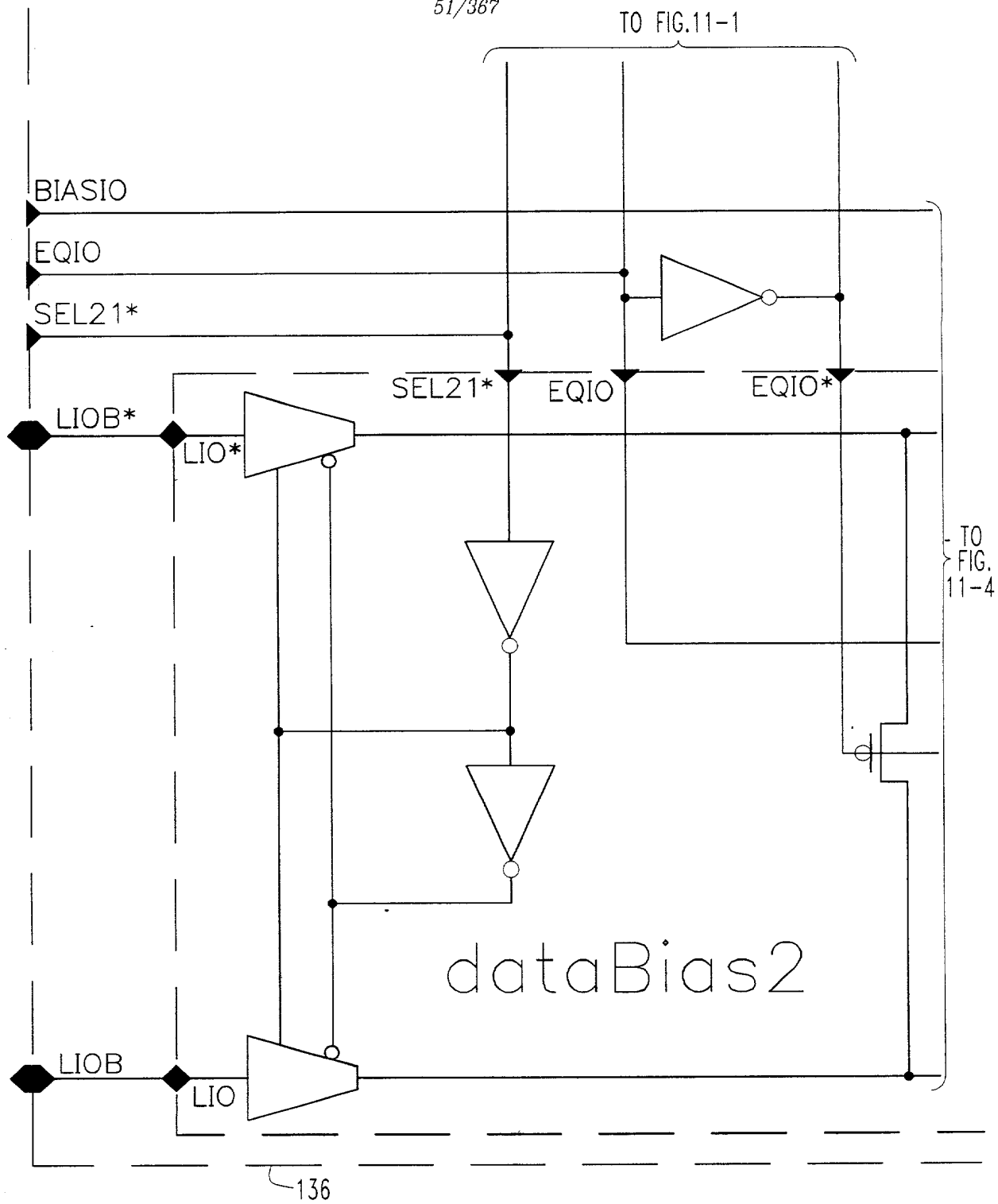


FIG.11-3

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TO FIG.11-2

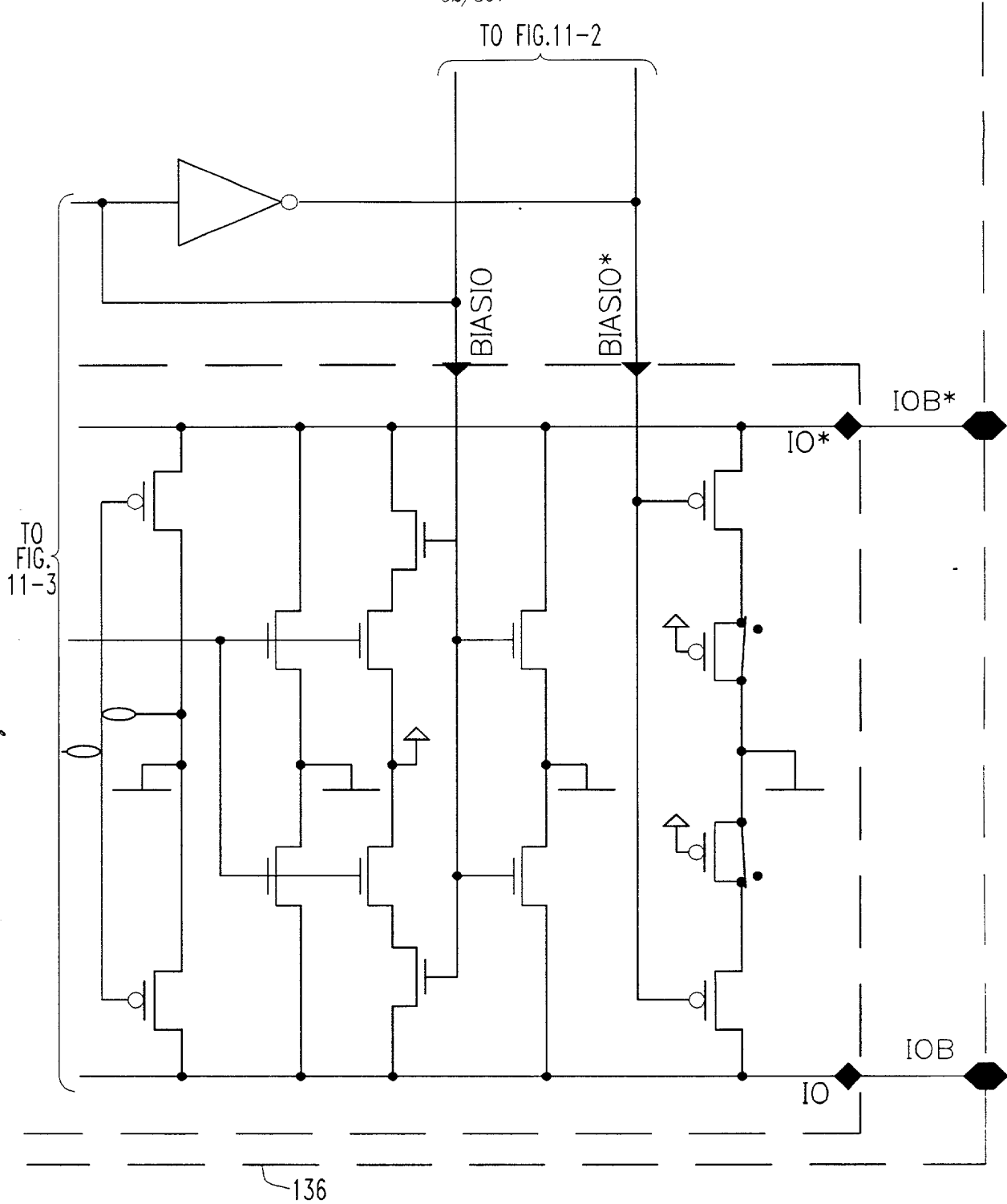
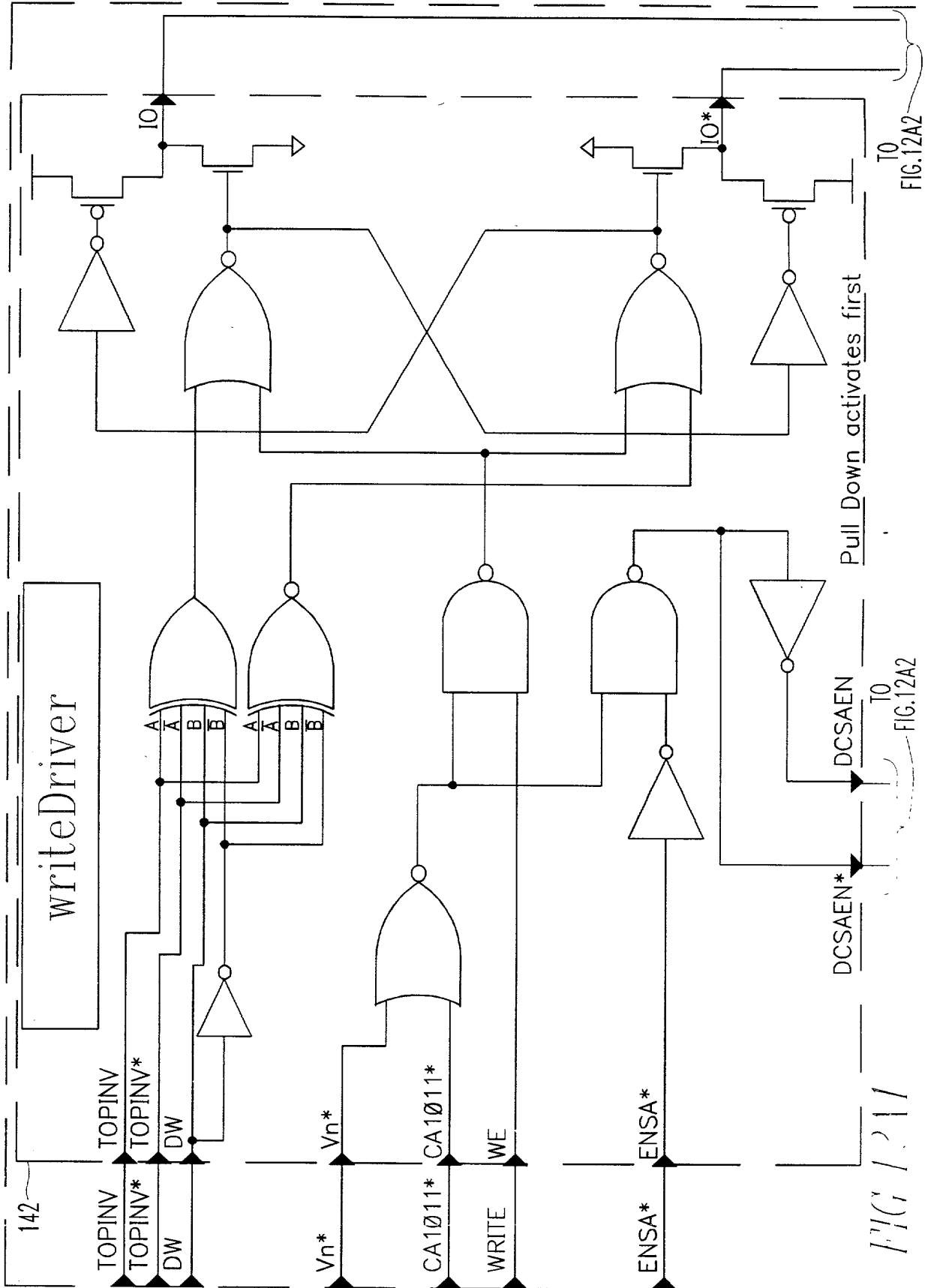


FIG.11-4



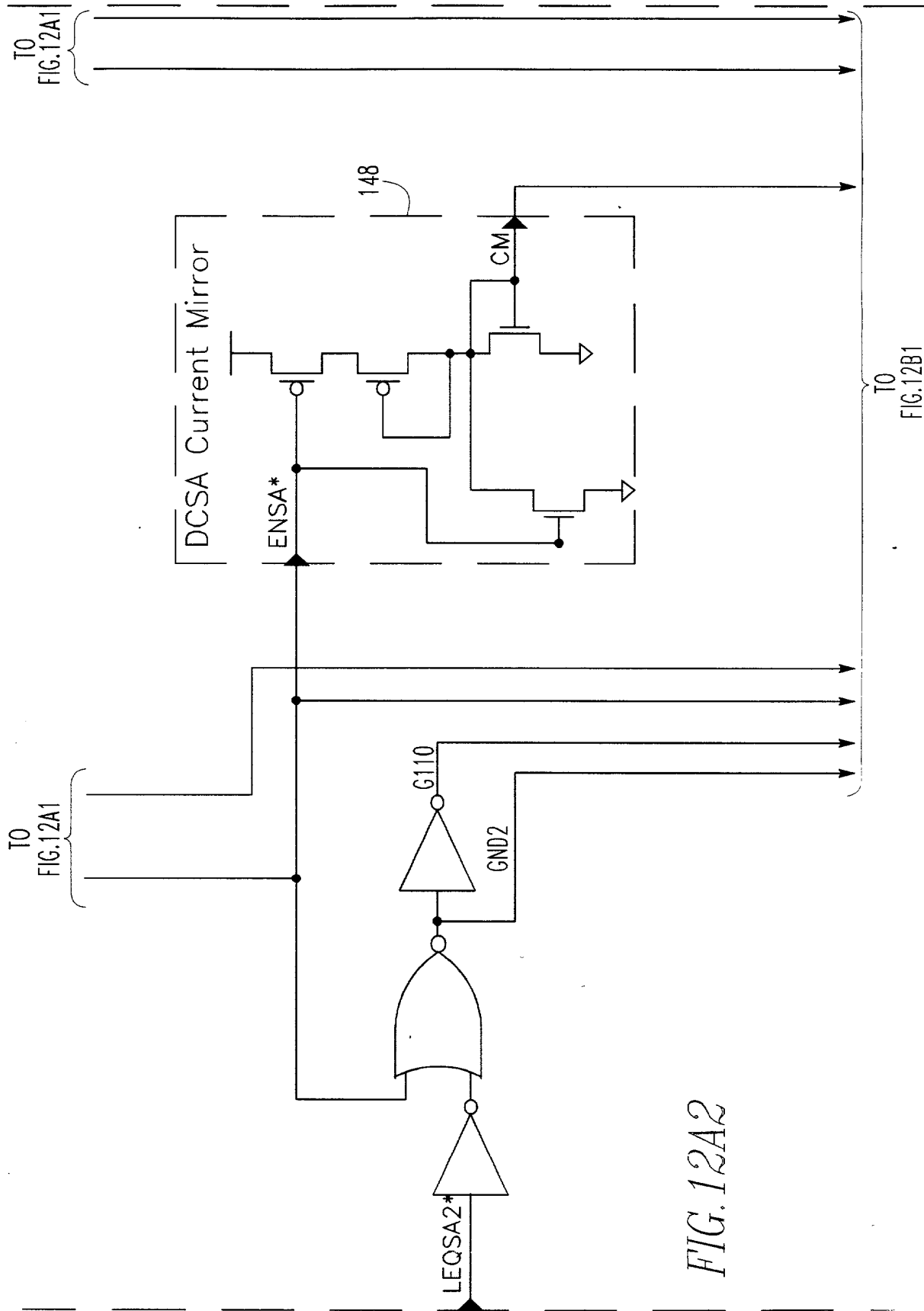
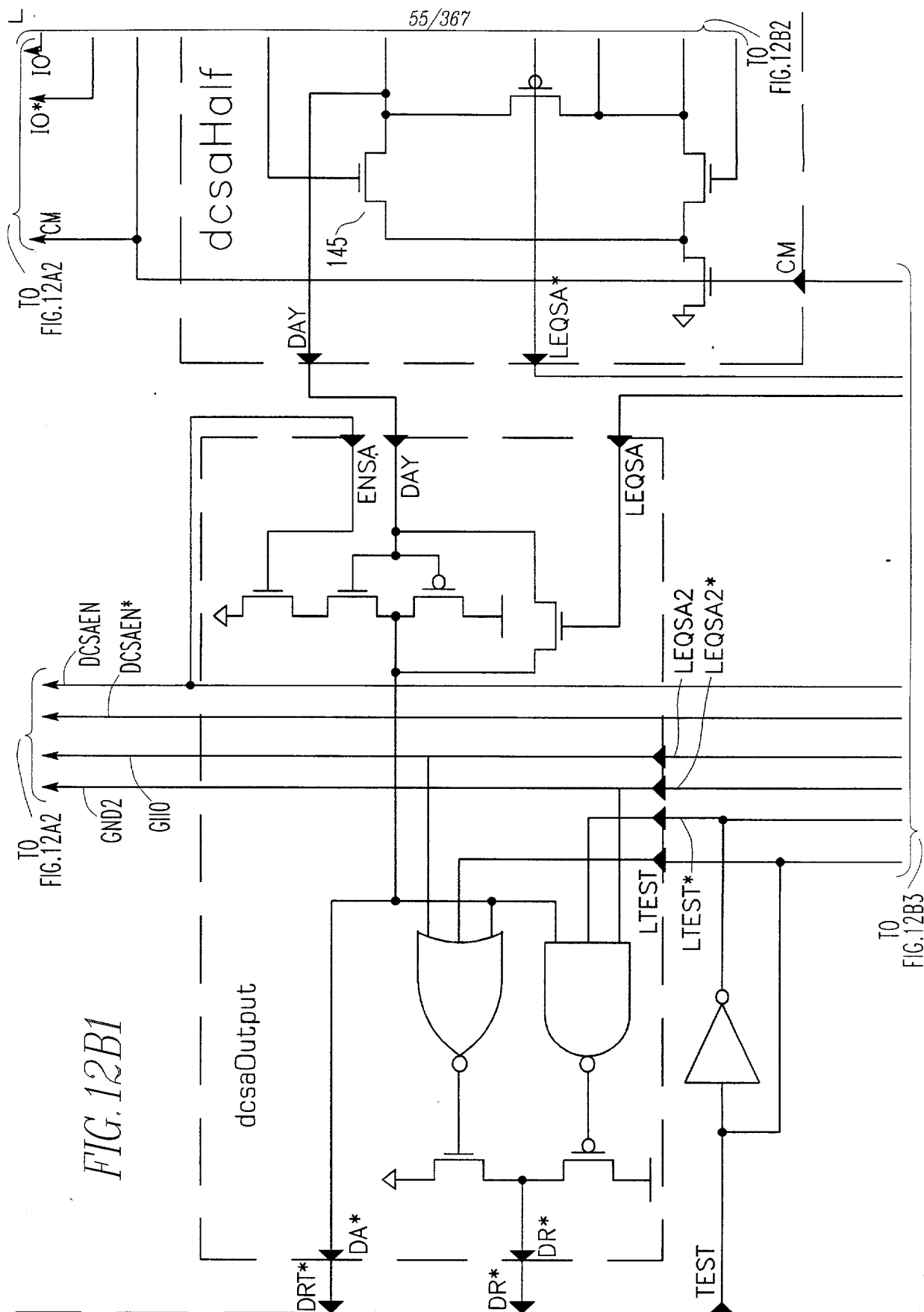


FIG. 12A2



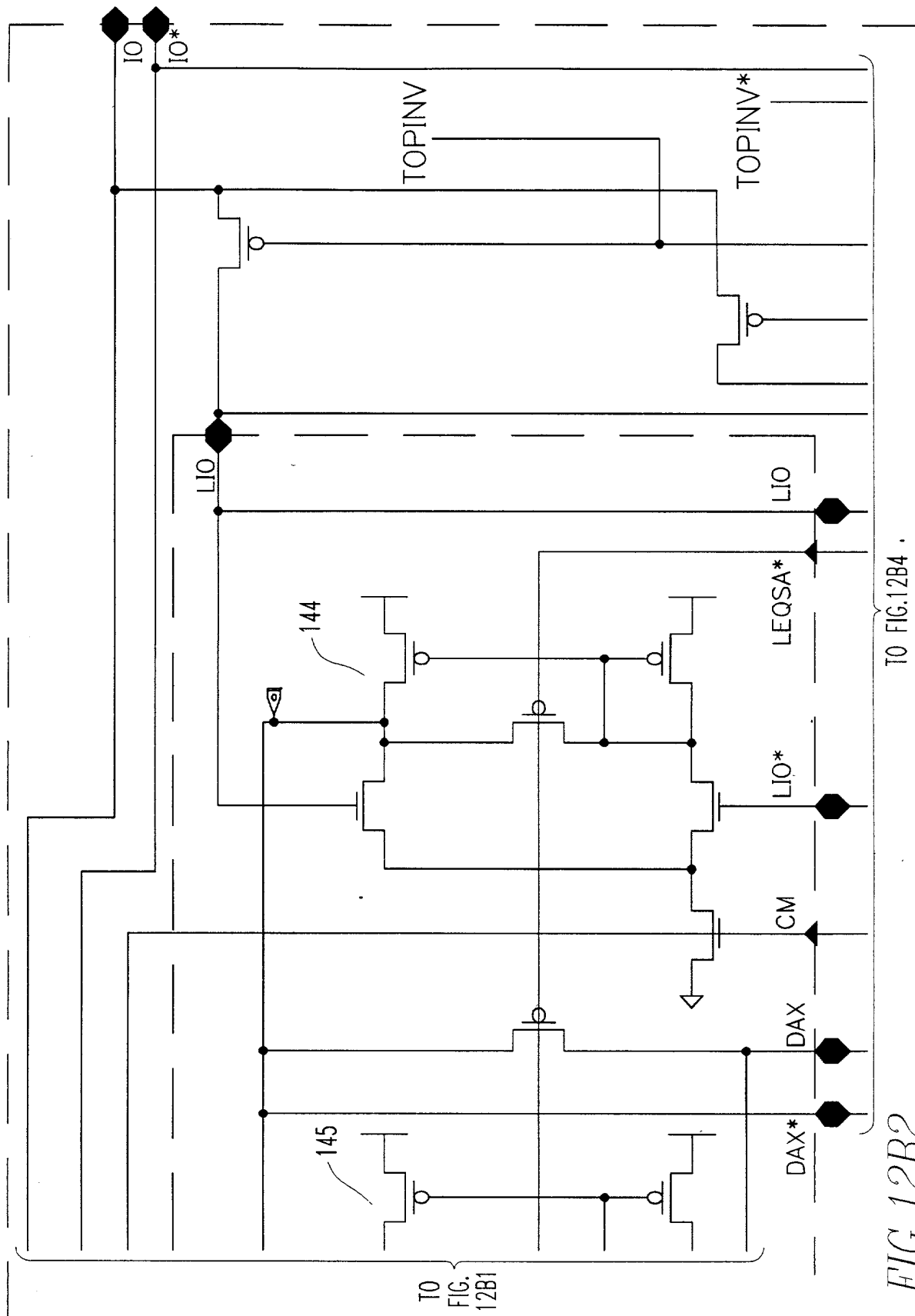
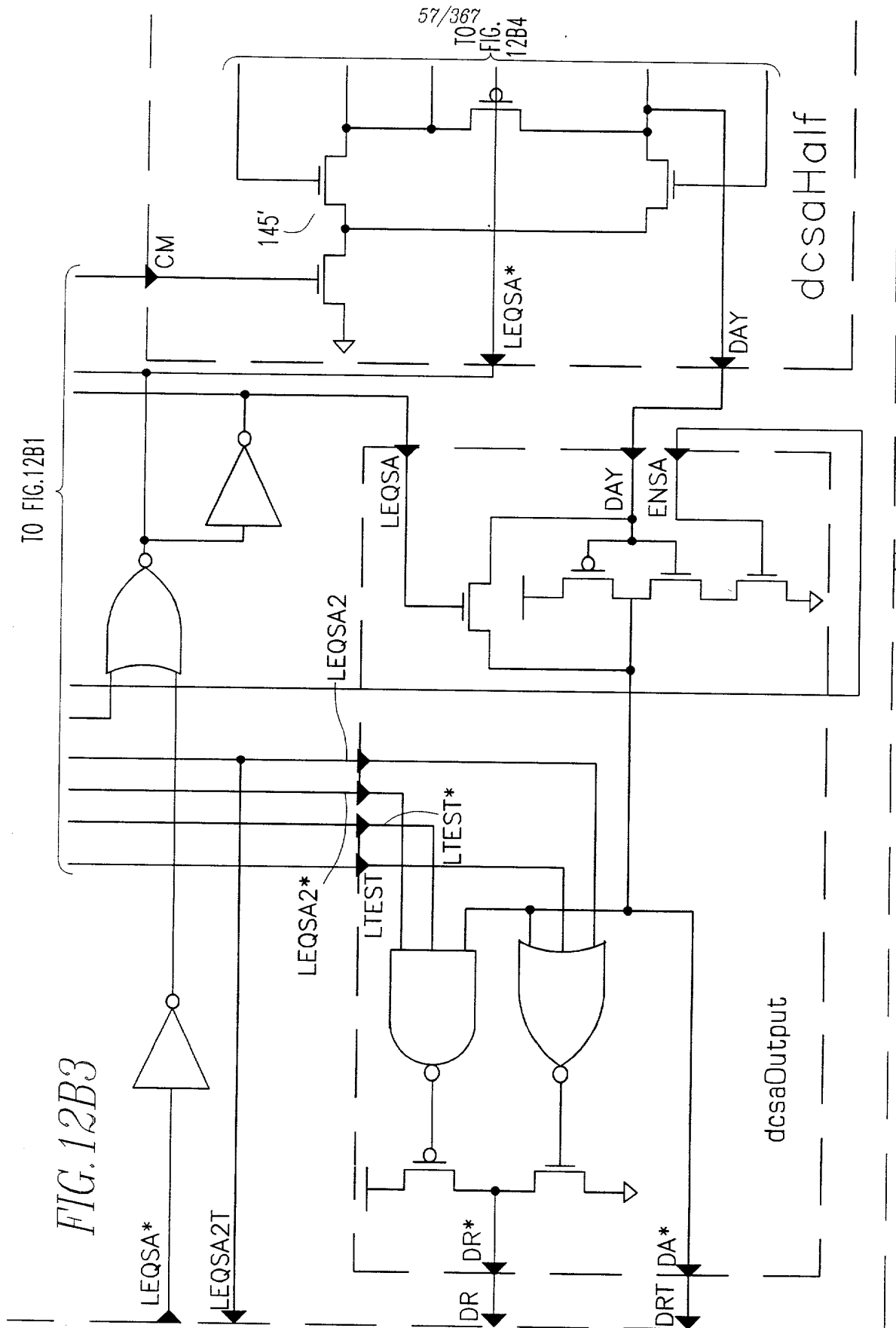
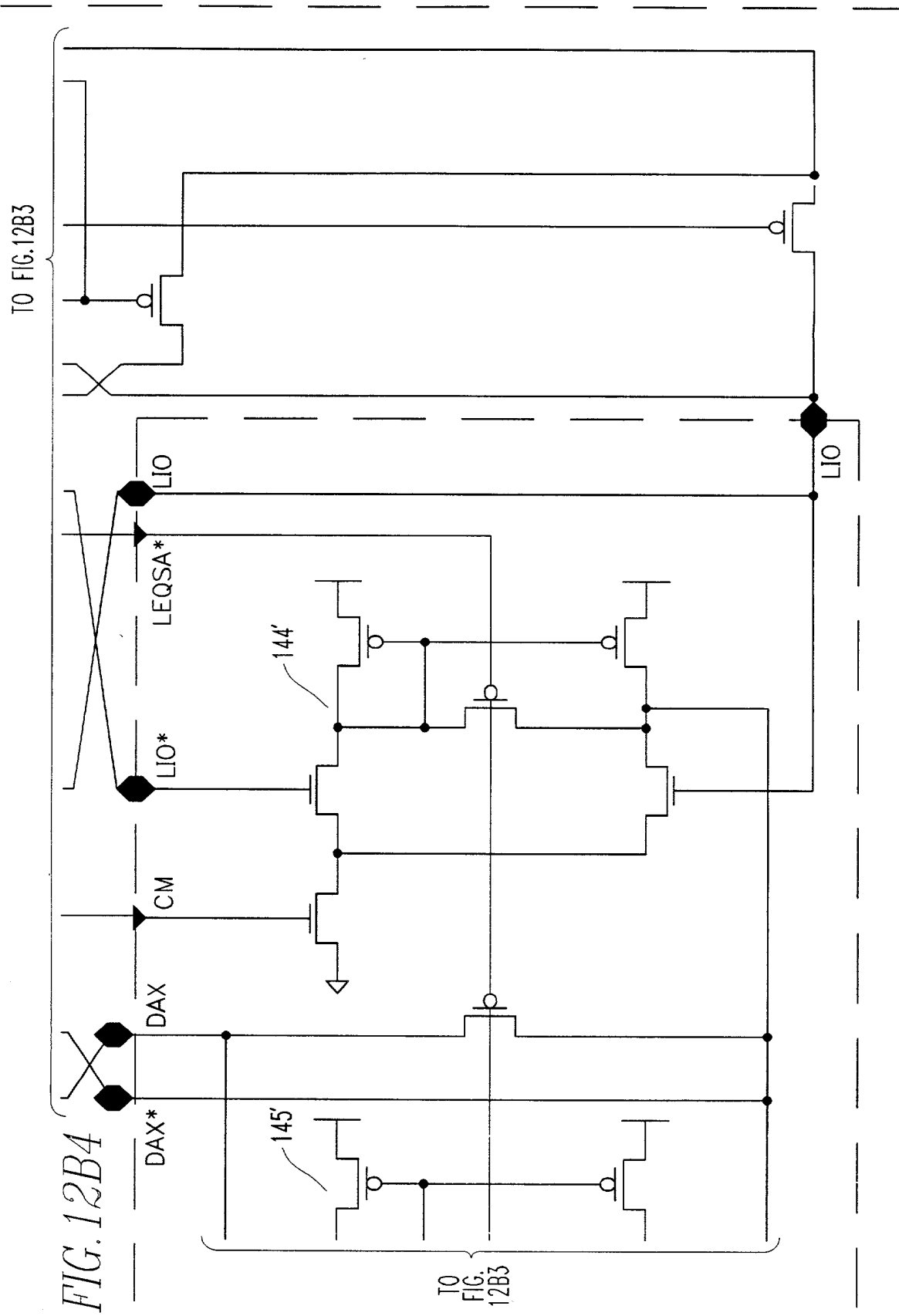
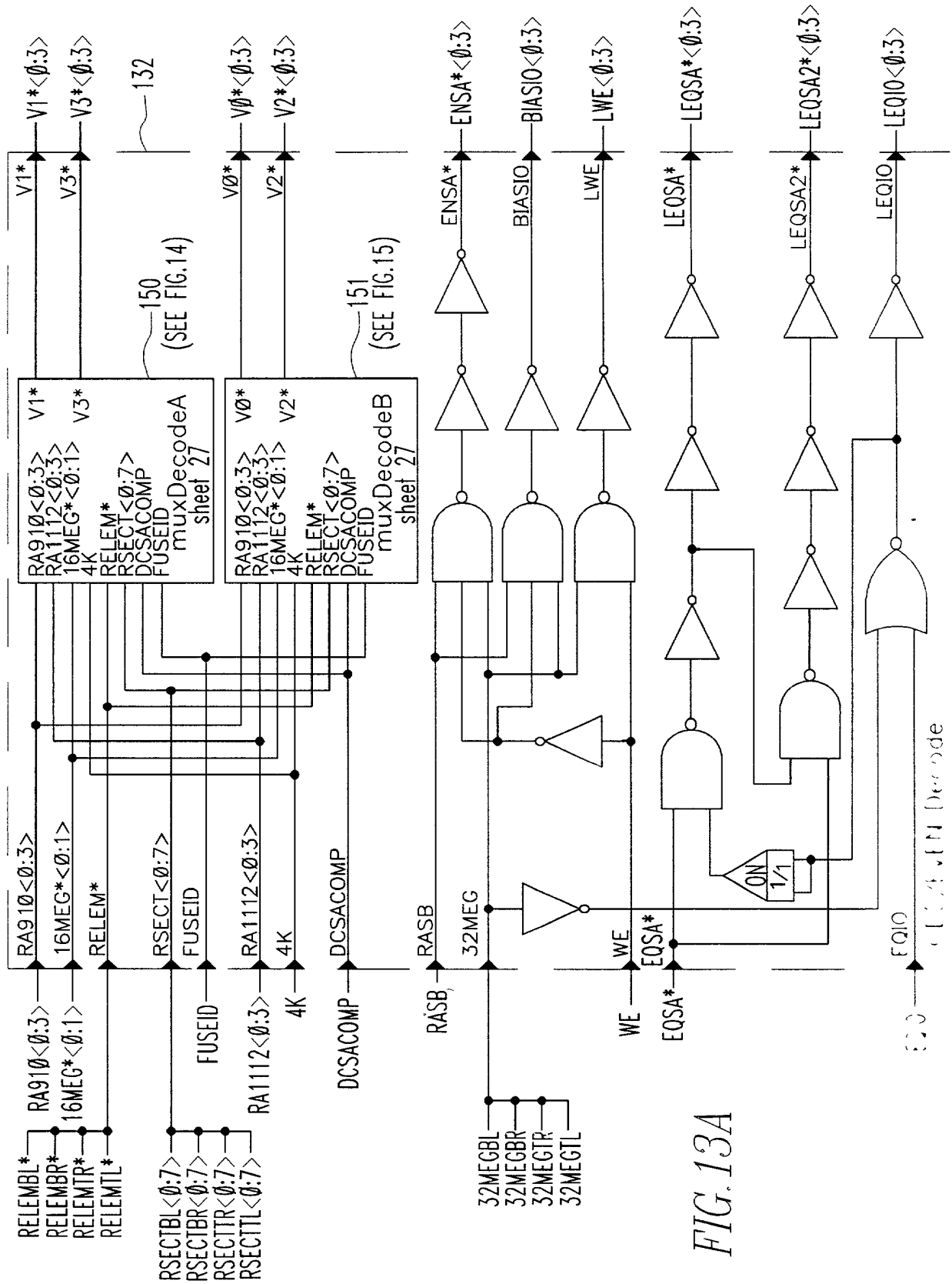


FIG. 12B2

TO FIG. 12B4







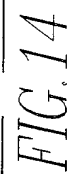


FIG. 15-1

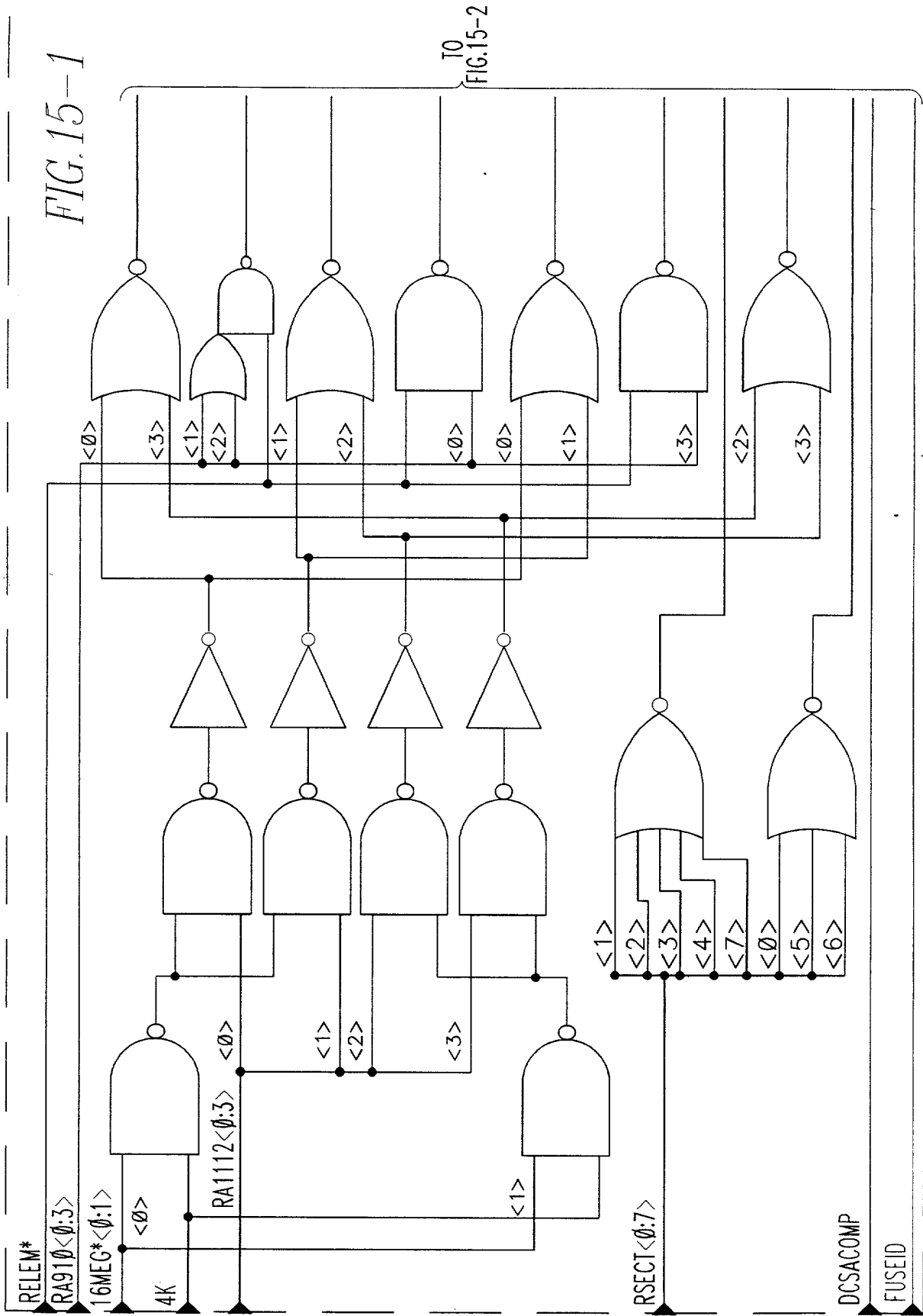


FIG. 15-2

muxDecodeB

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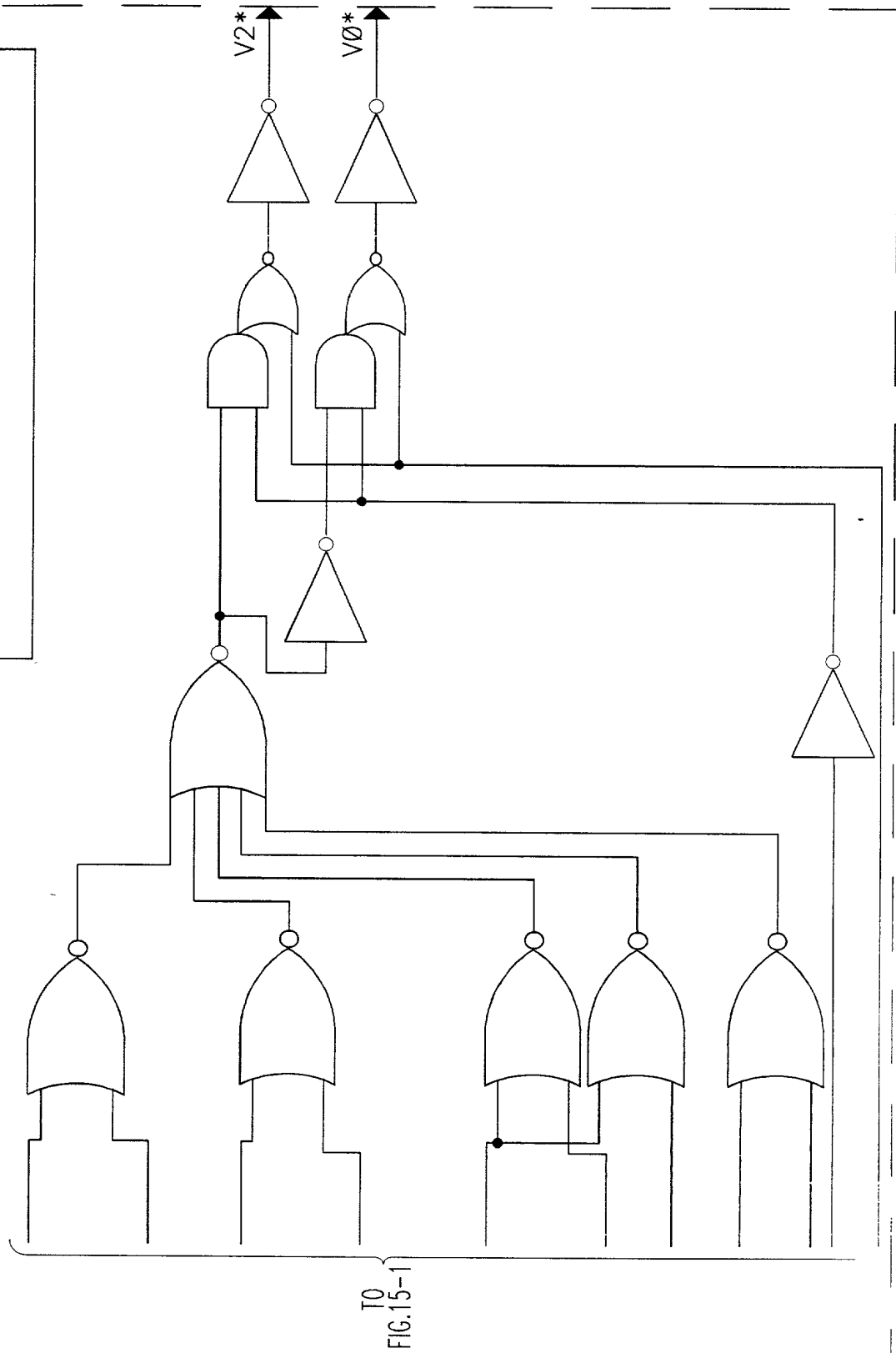
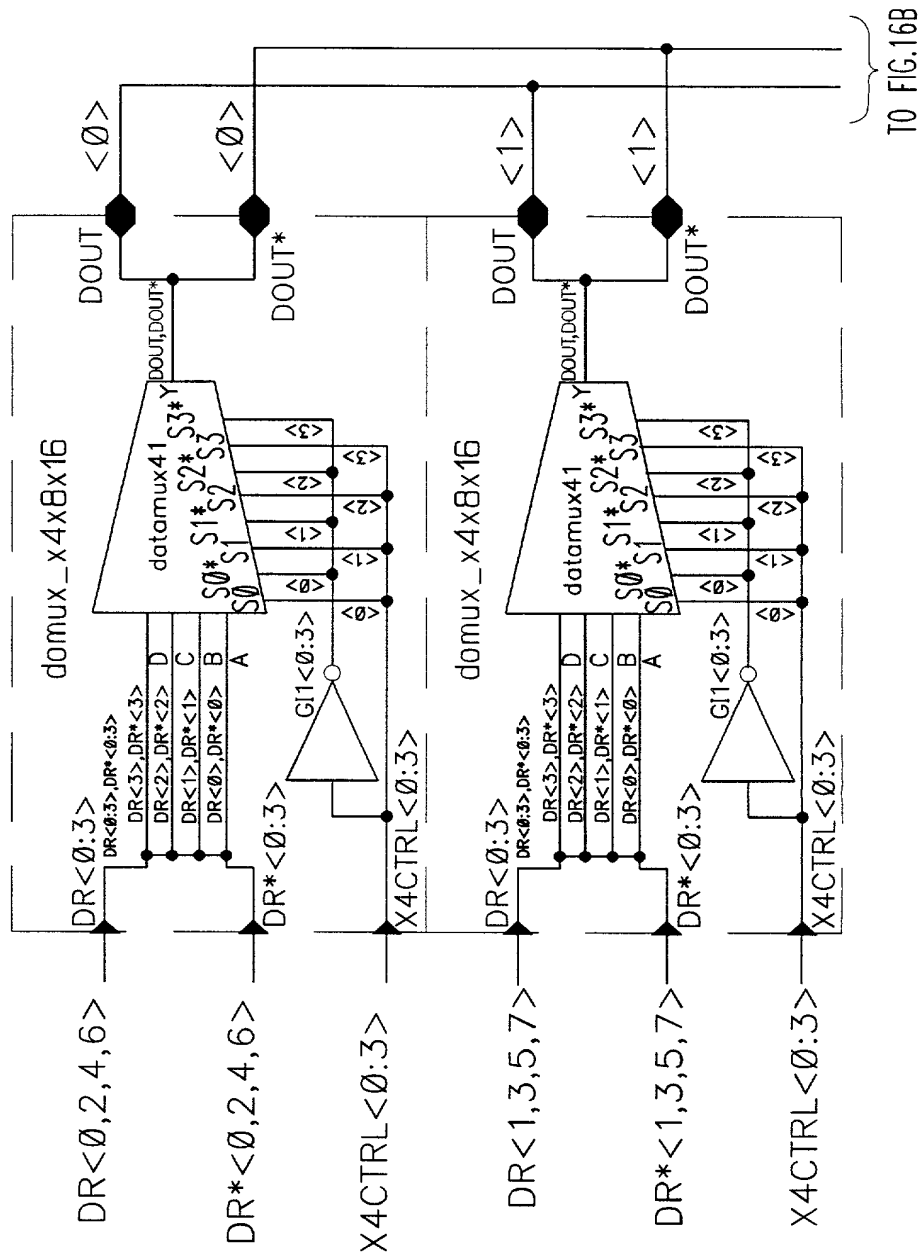
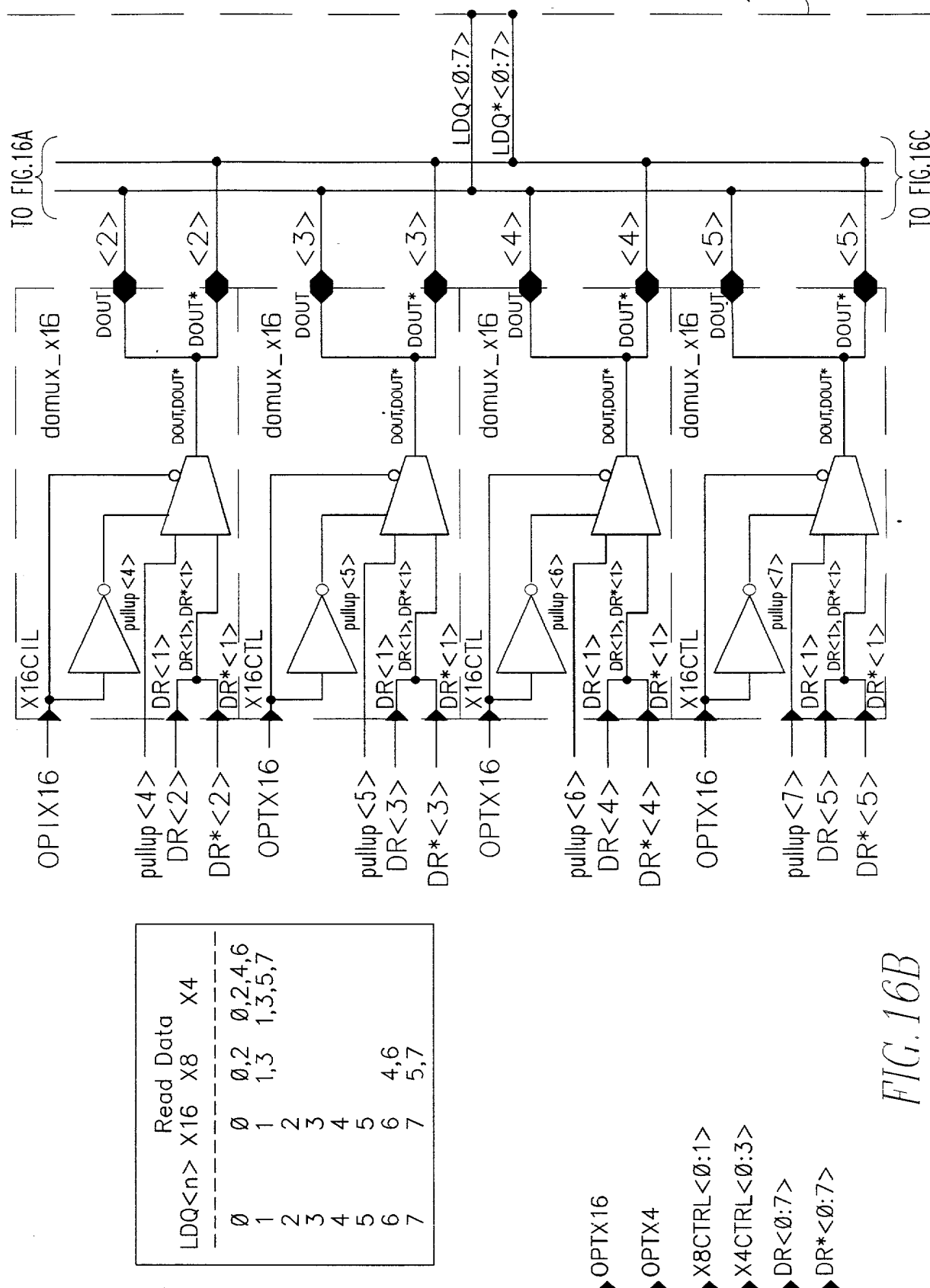


FIG. 16A





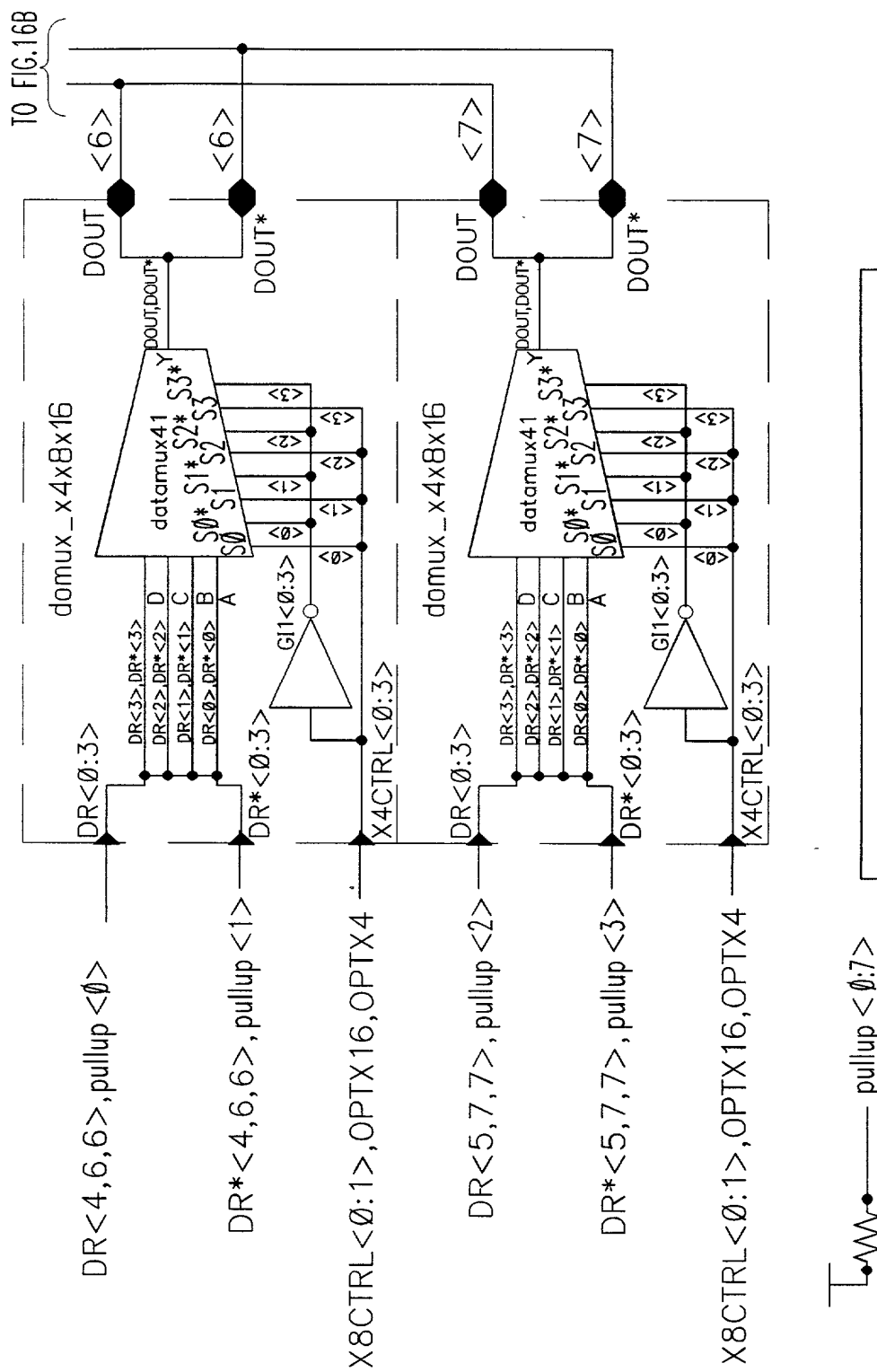
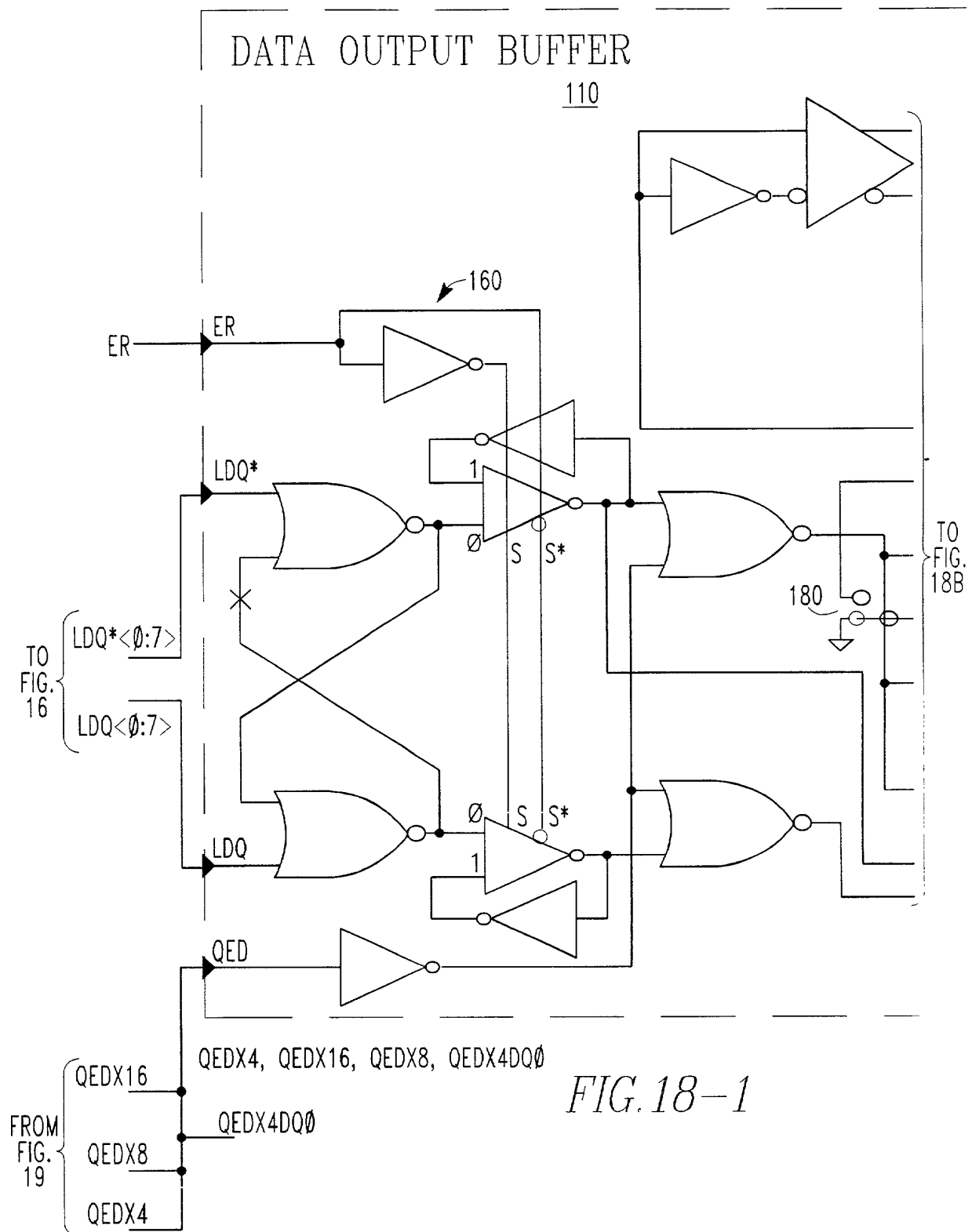


FIG. 16C



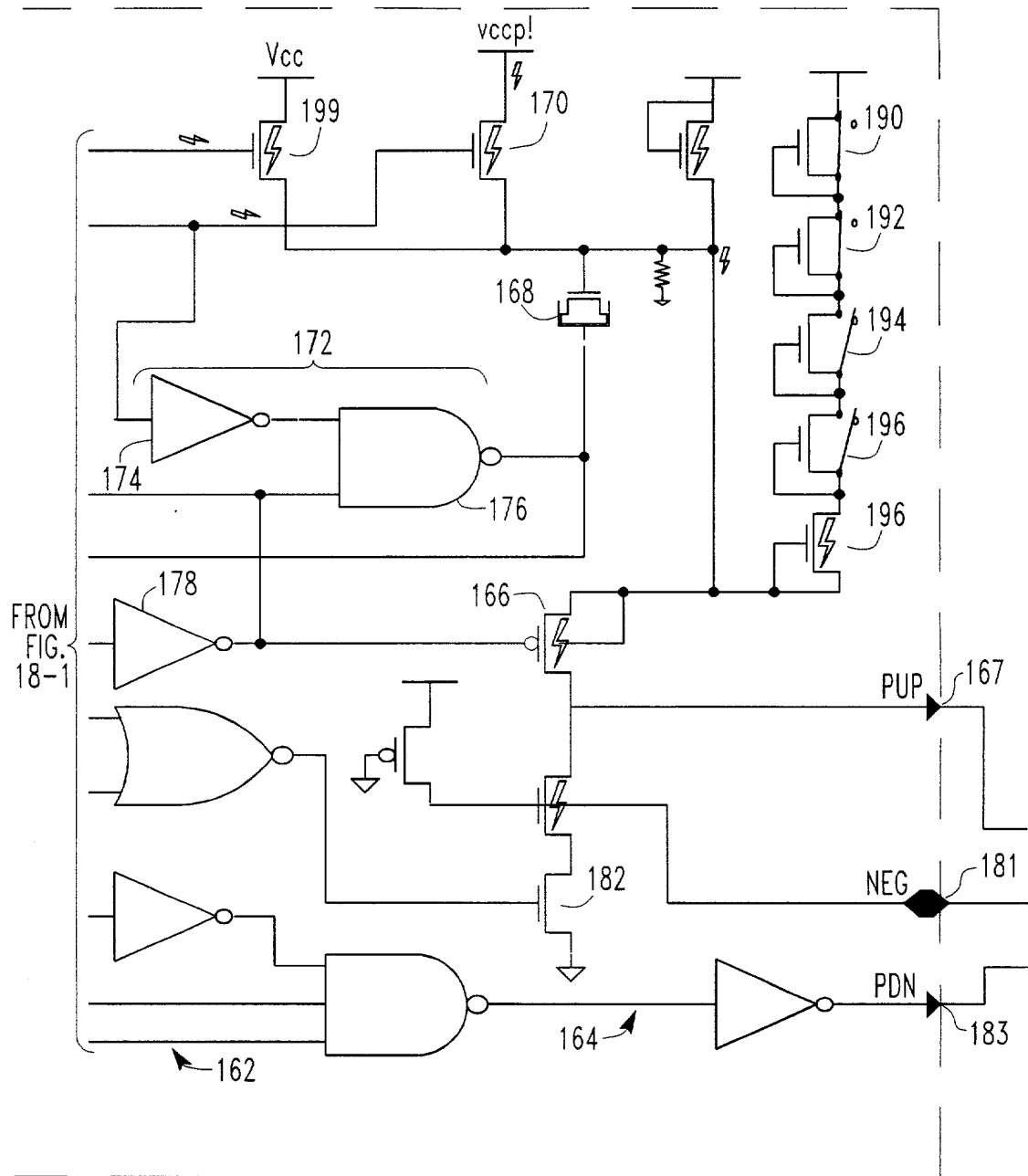


FIG. 18-2

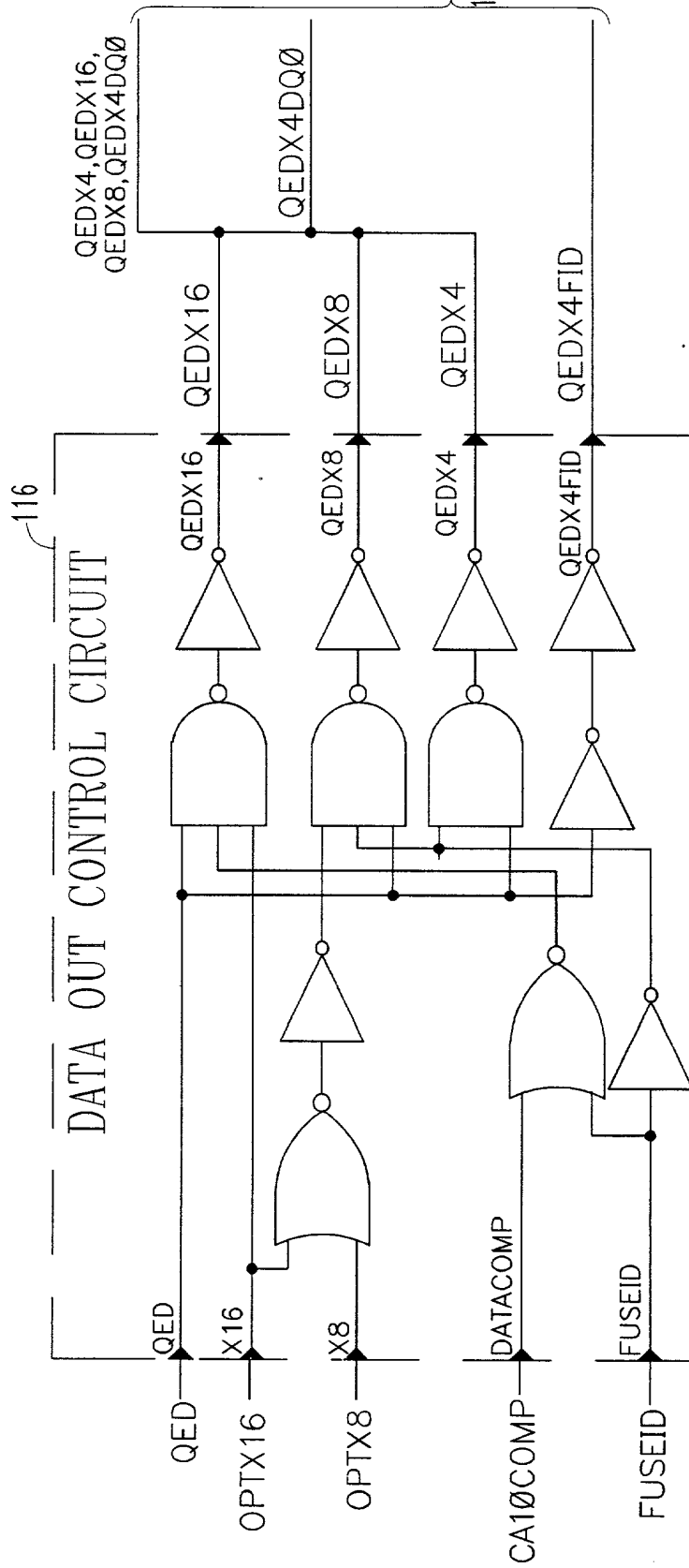


FIG. 19

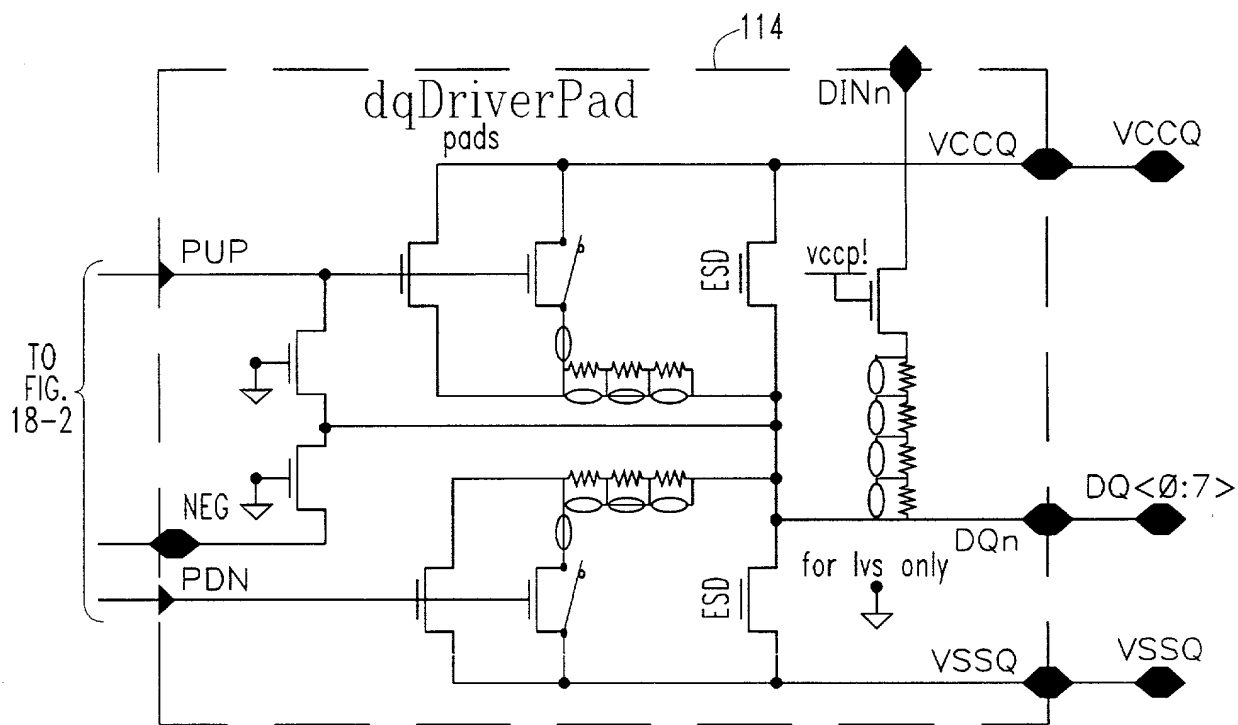


FIG. 20

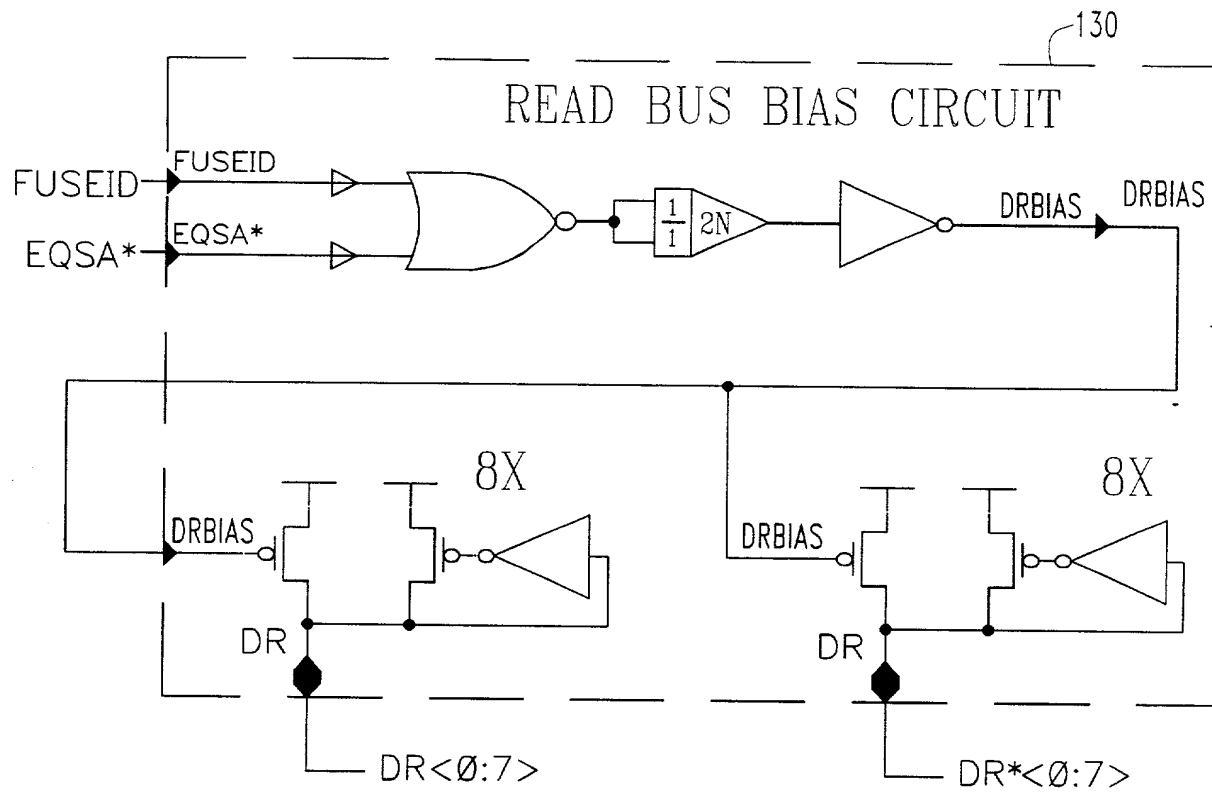
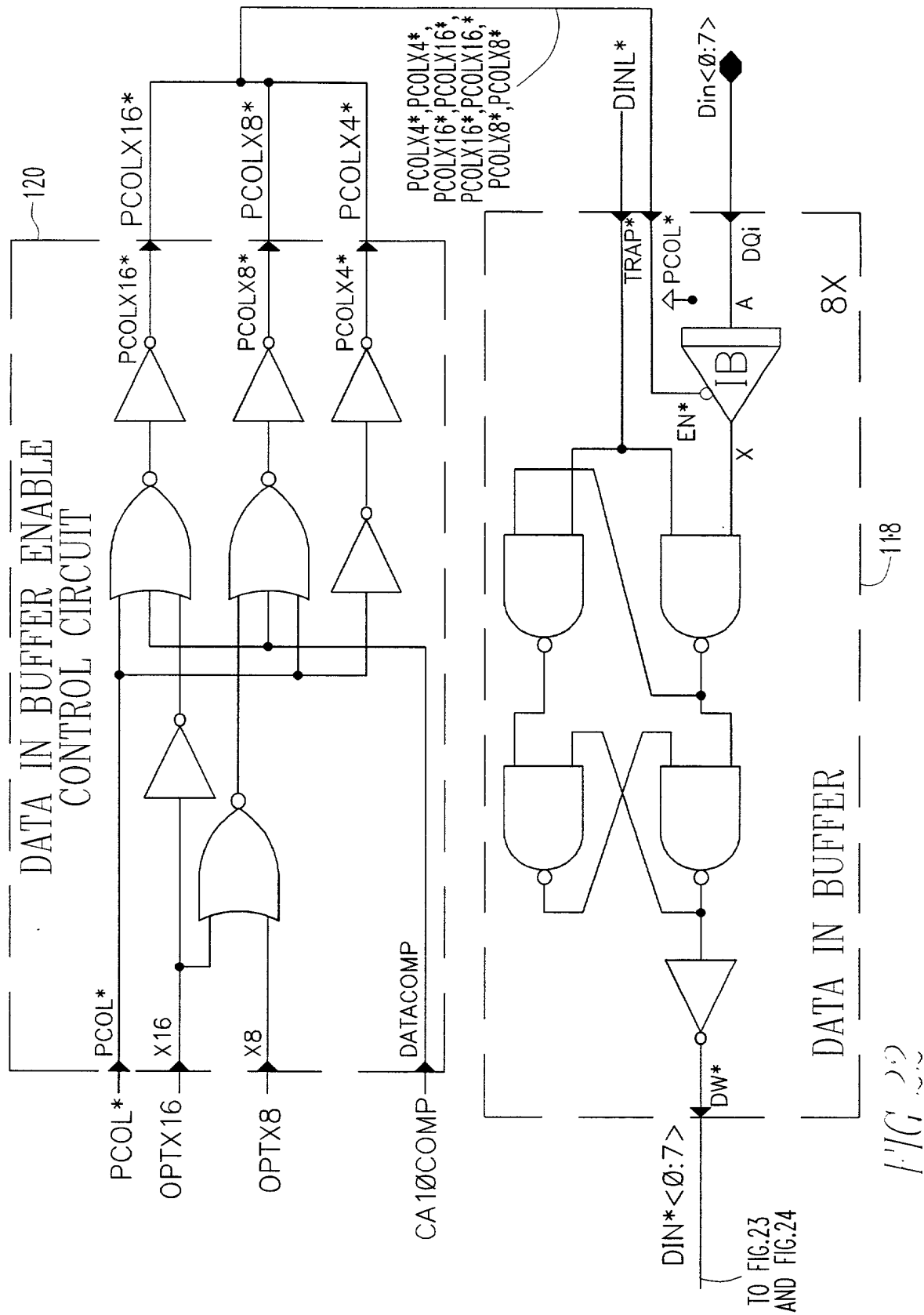
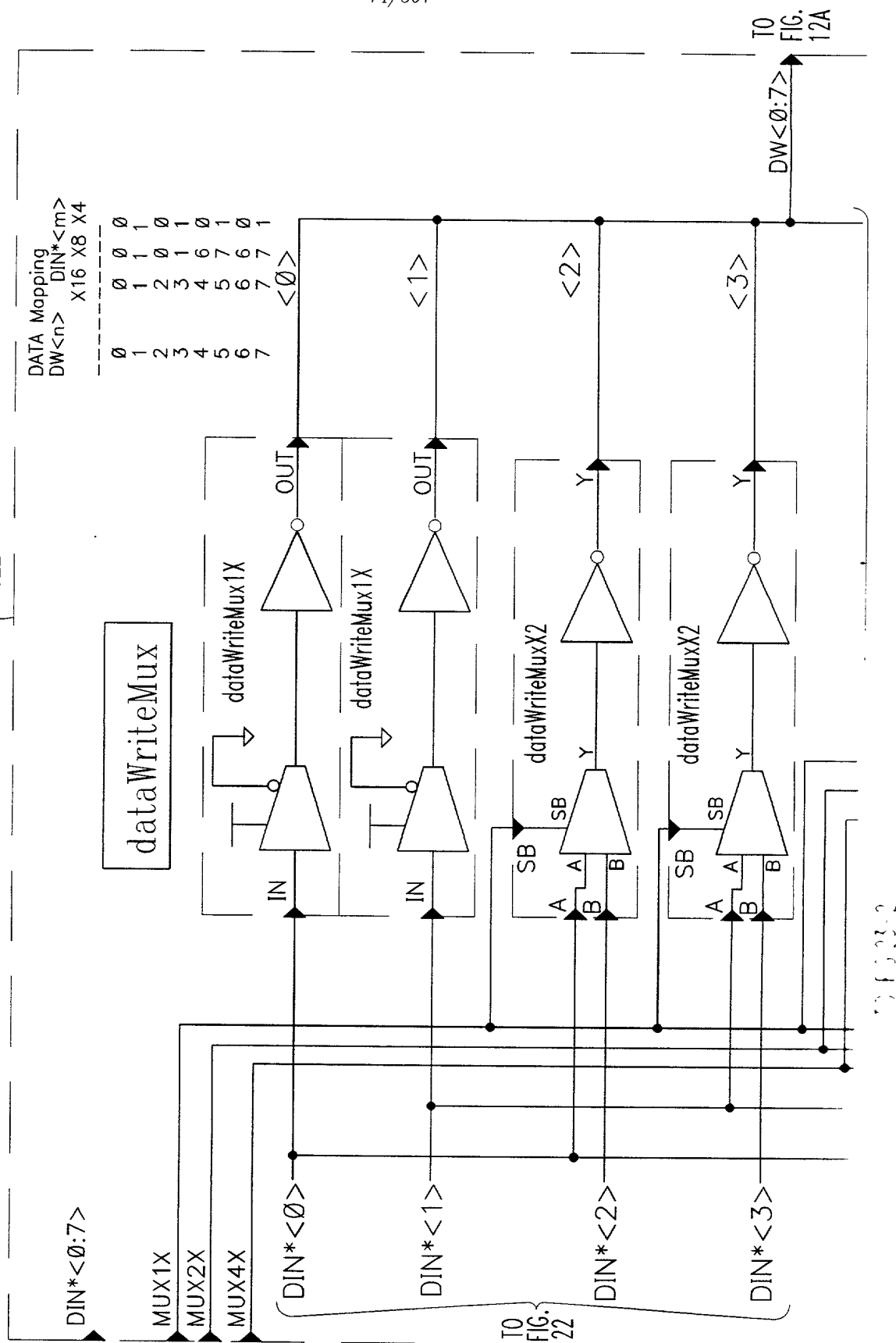
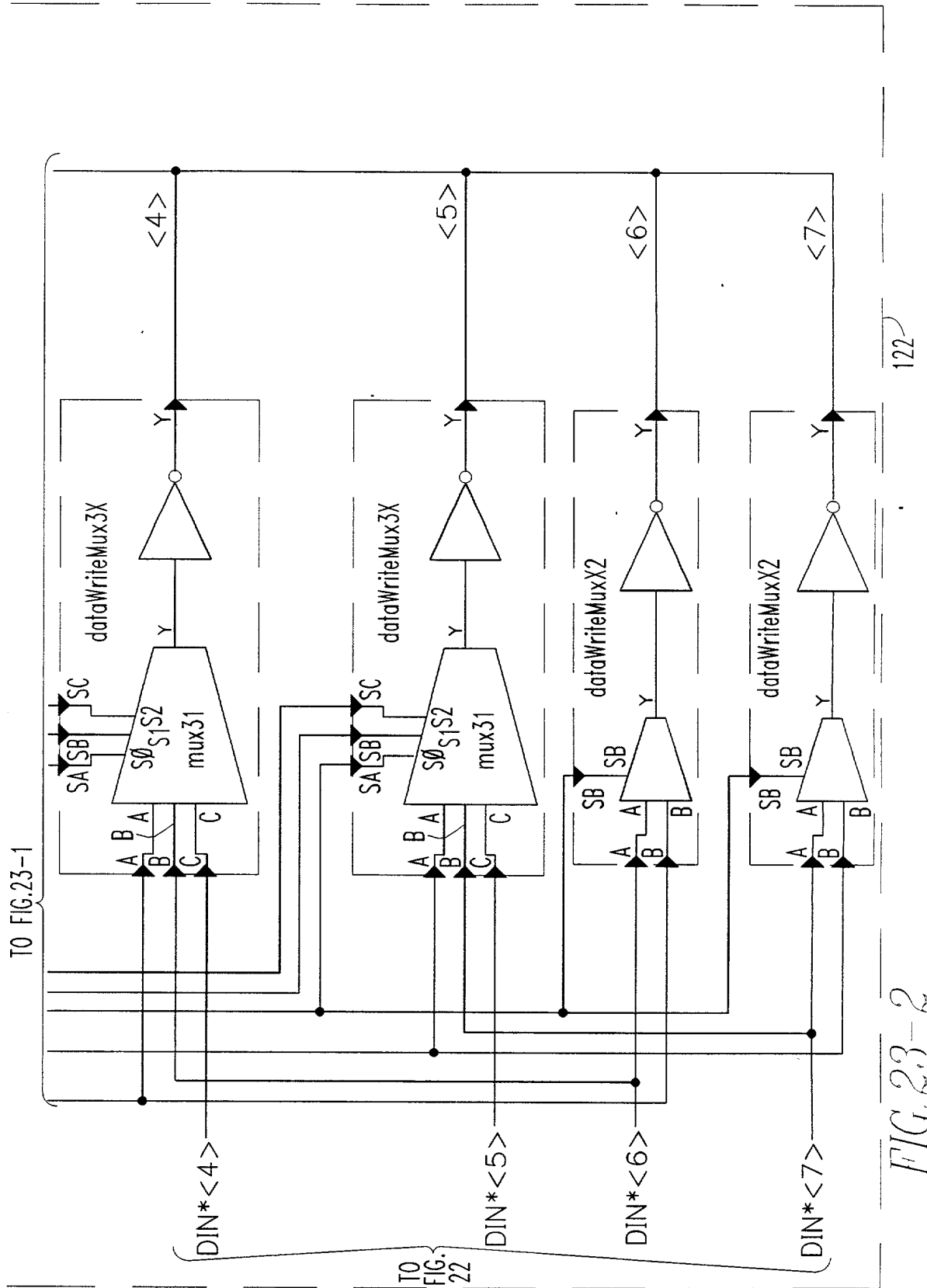


FIG. 21



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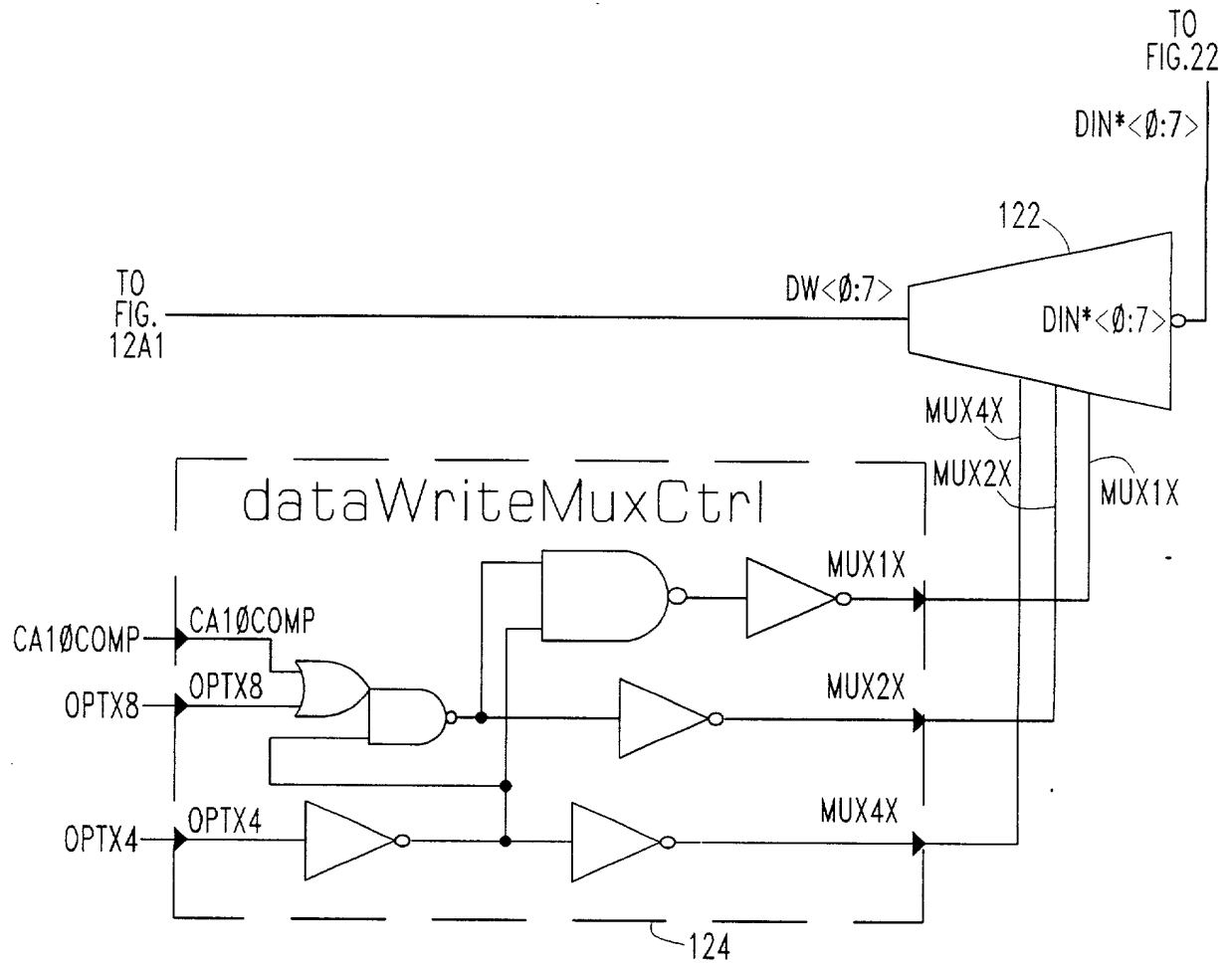
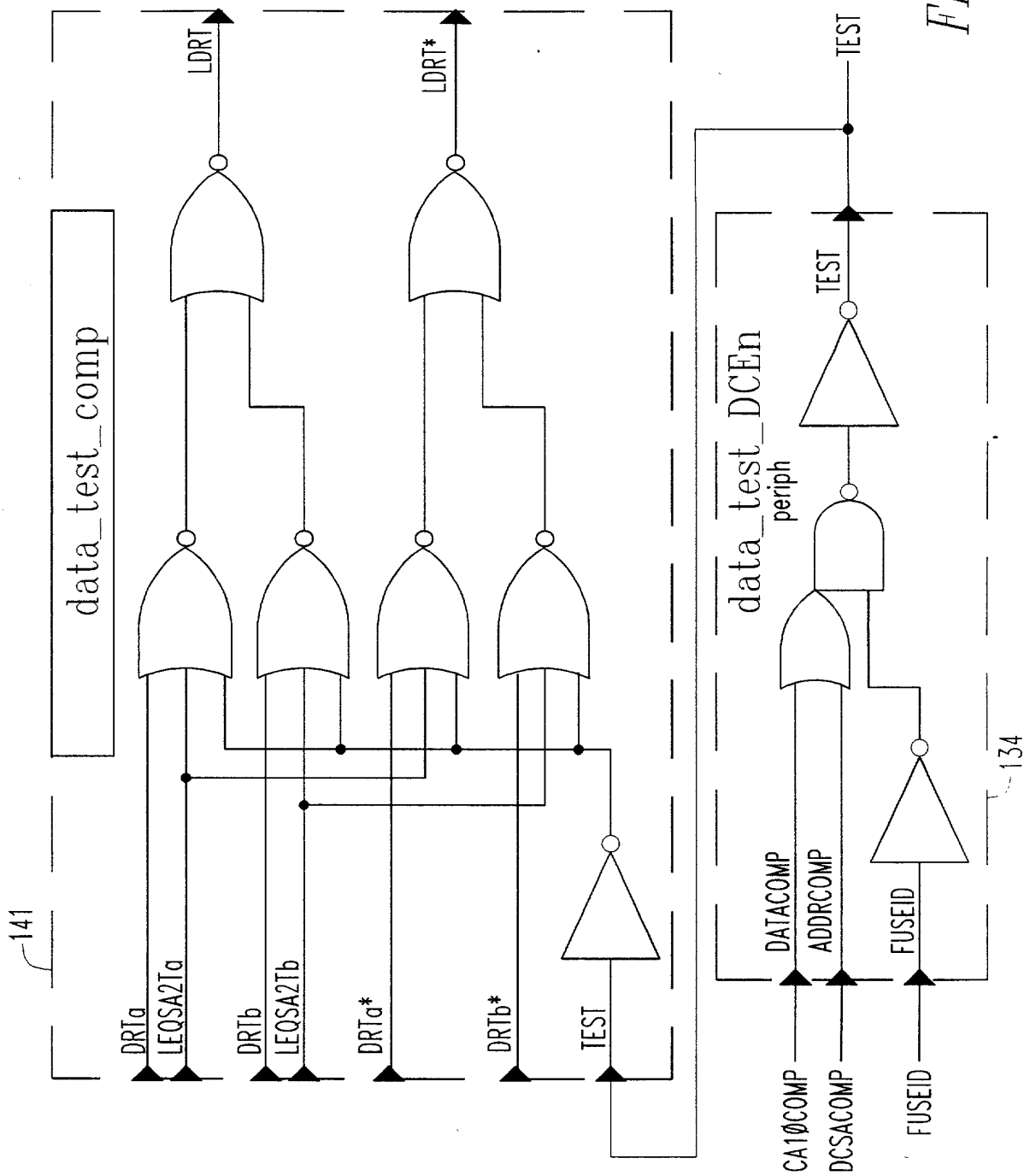


FIG. 24



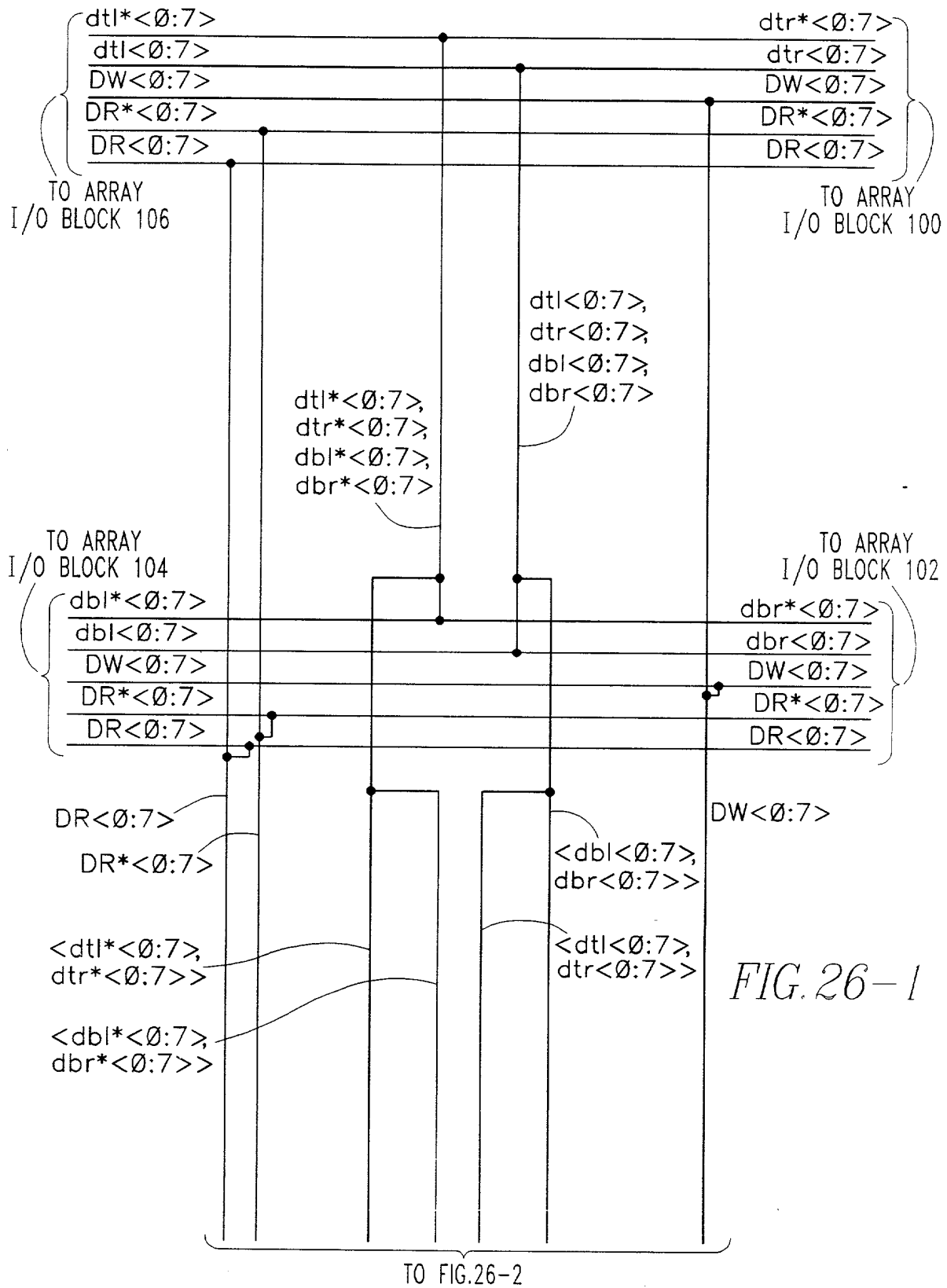


FIG. 26-1

FROM FIG.26-1

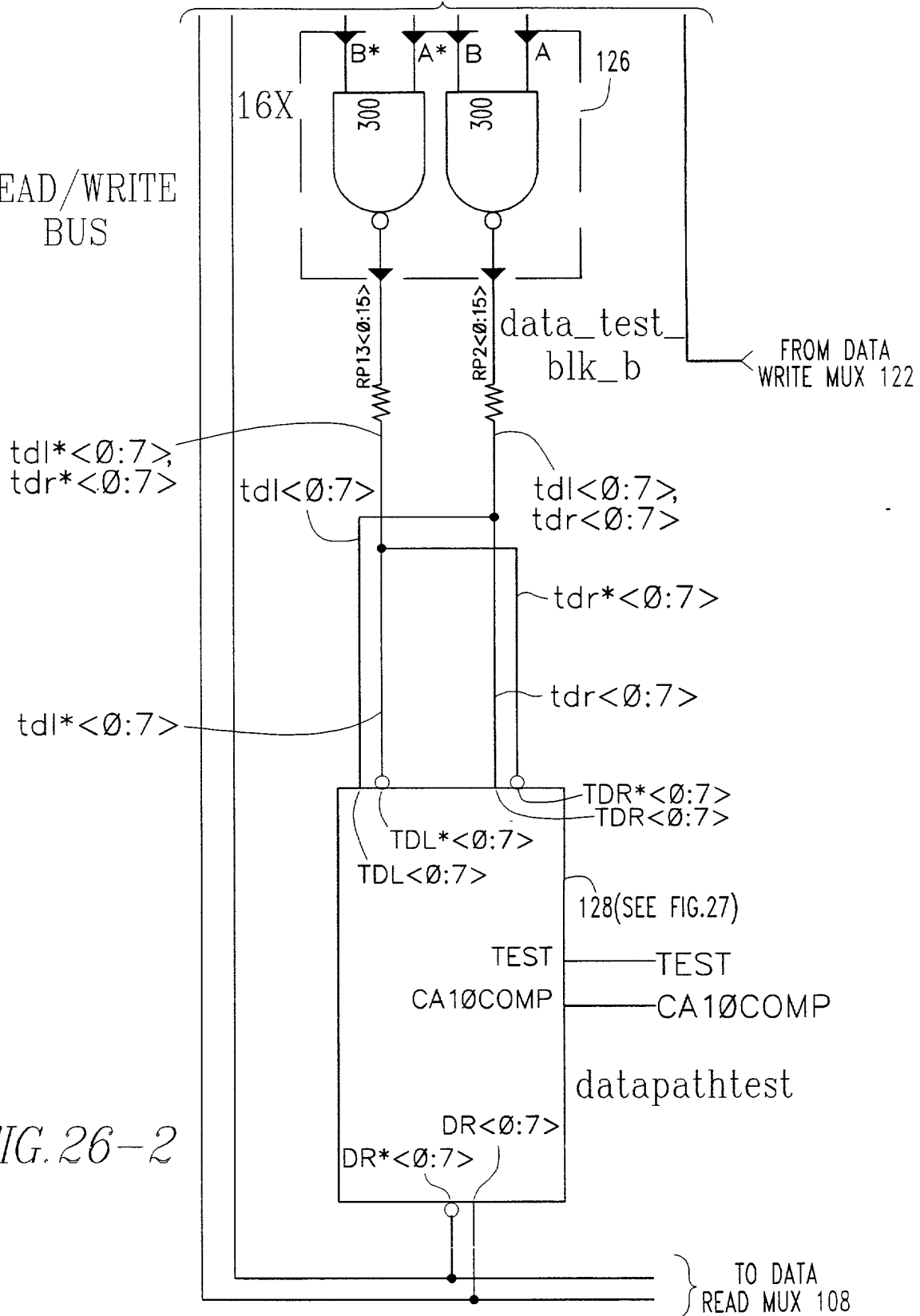
READ/WRITE
BUS

FIG. 26-2

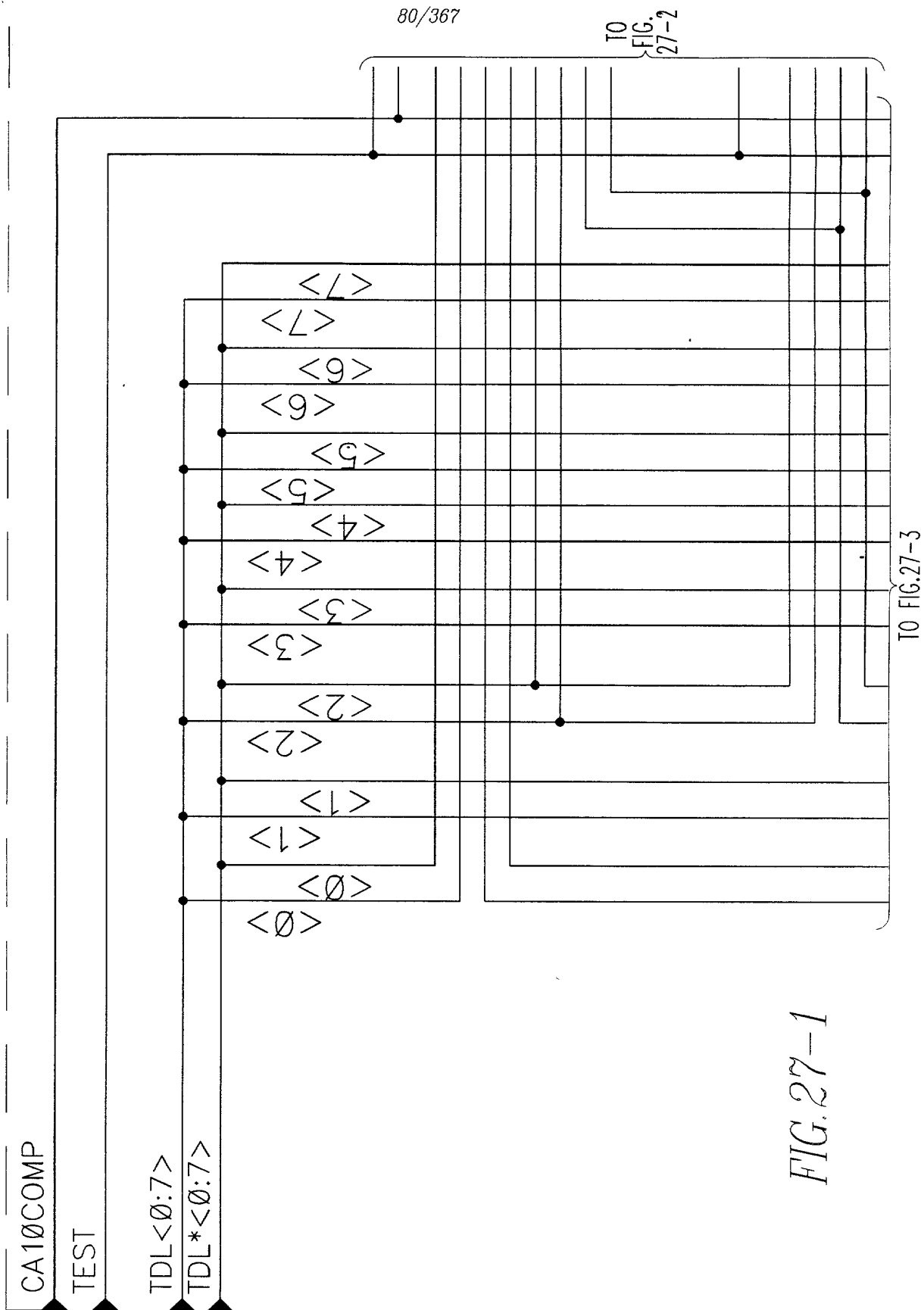
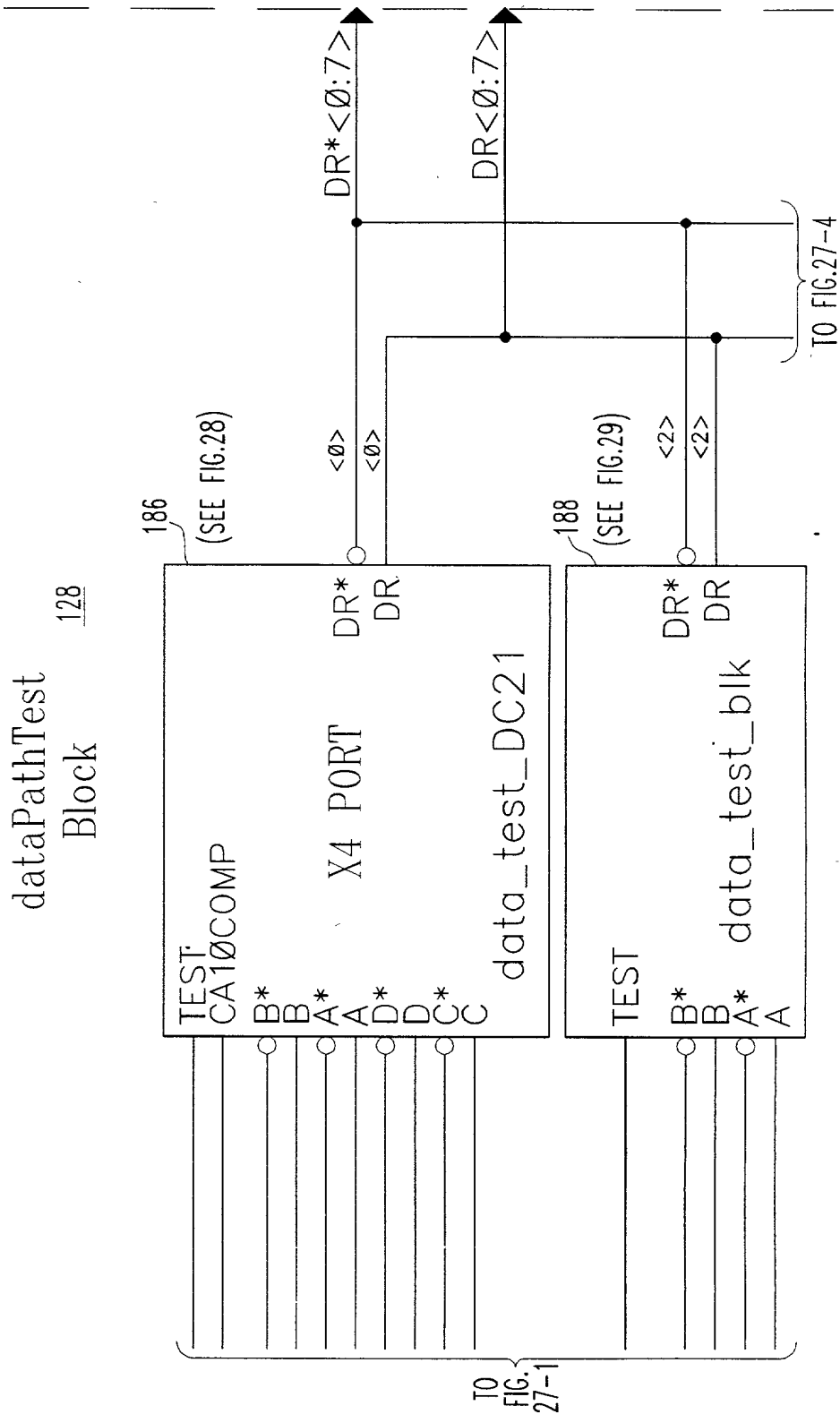


FIG. 27-2



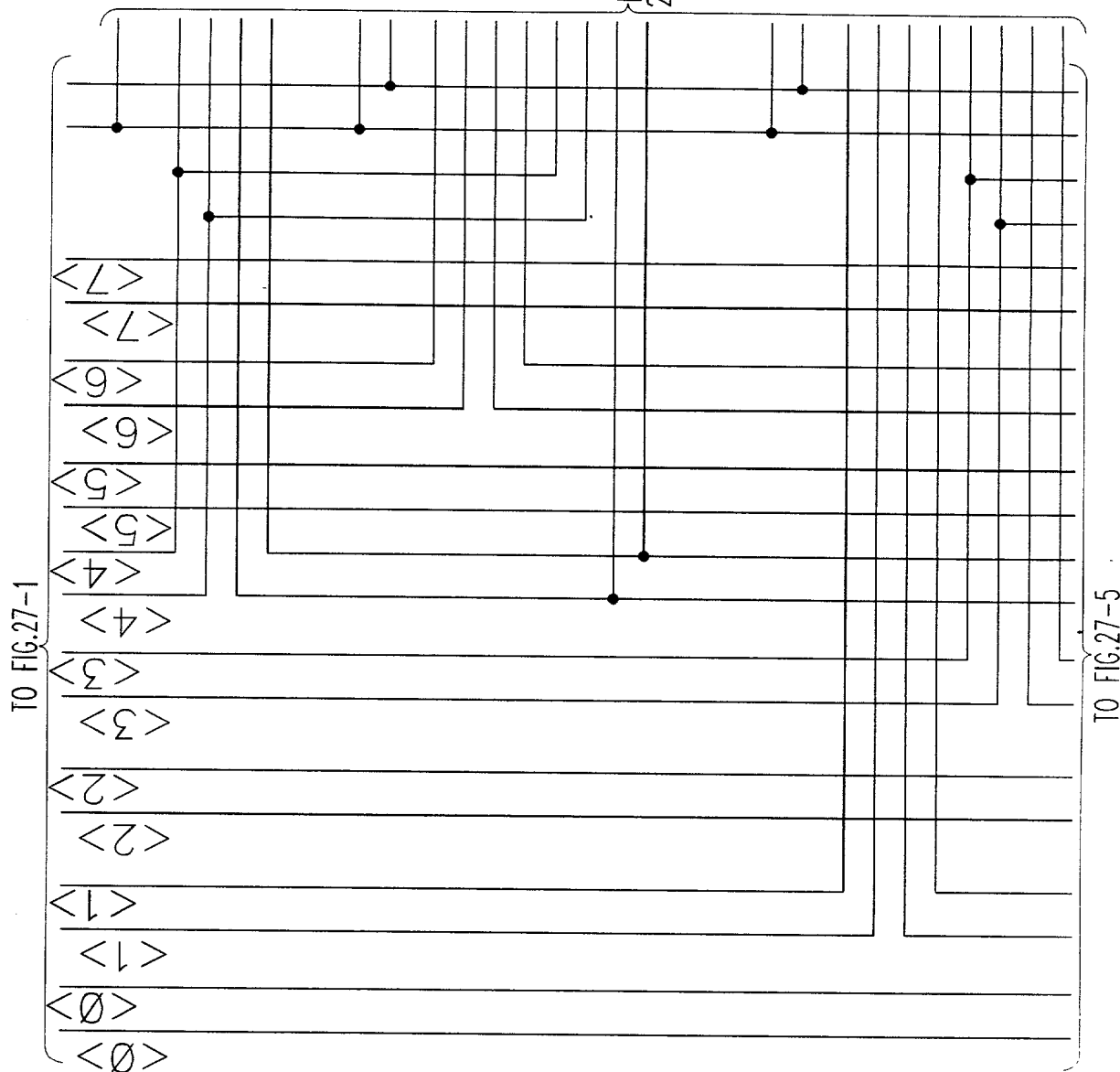


FIG 27-3

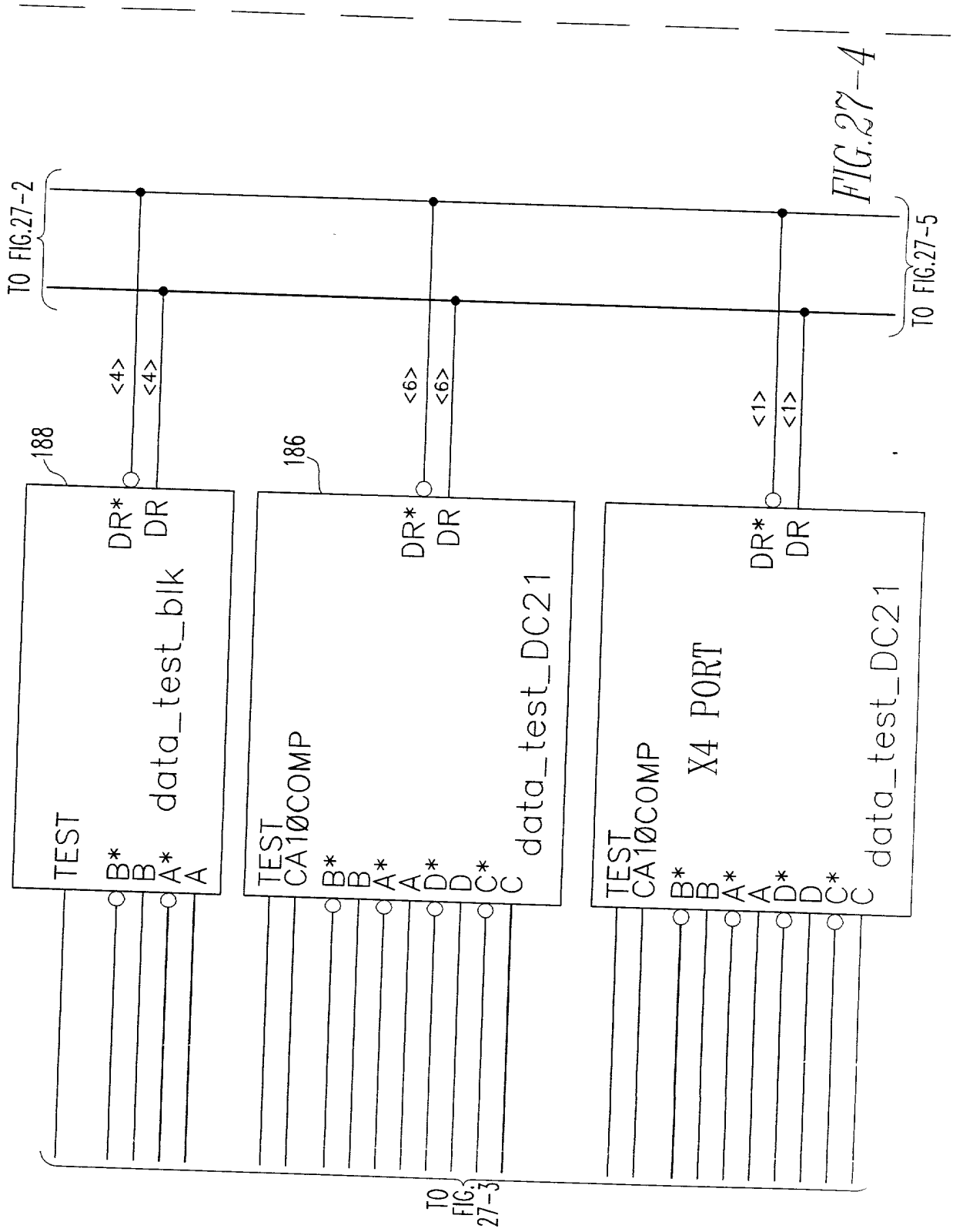


FIG. 27-5

TO FIG. 27-3

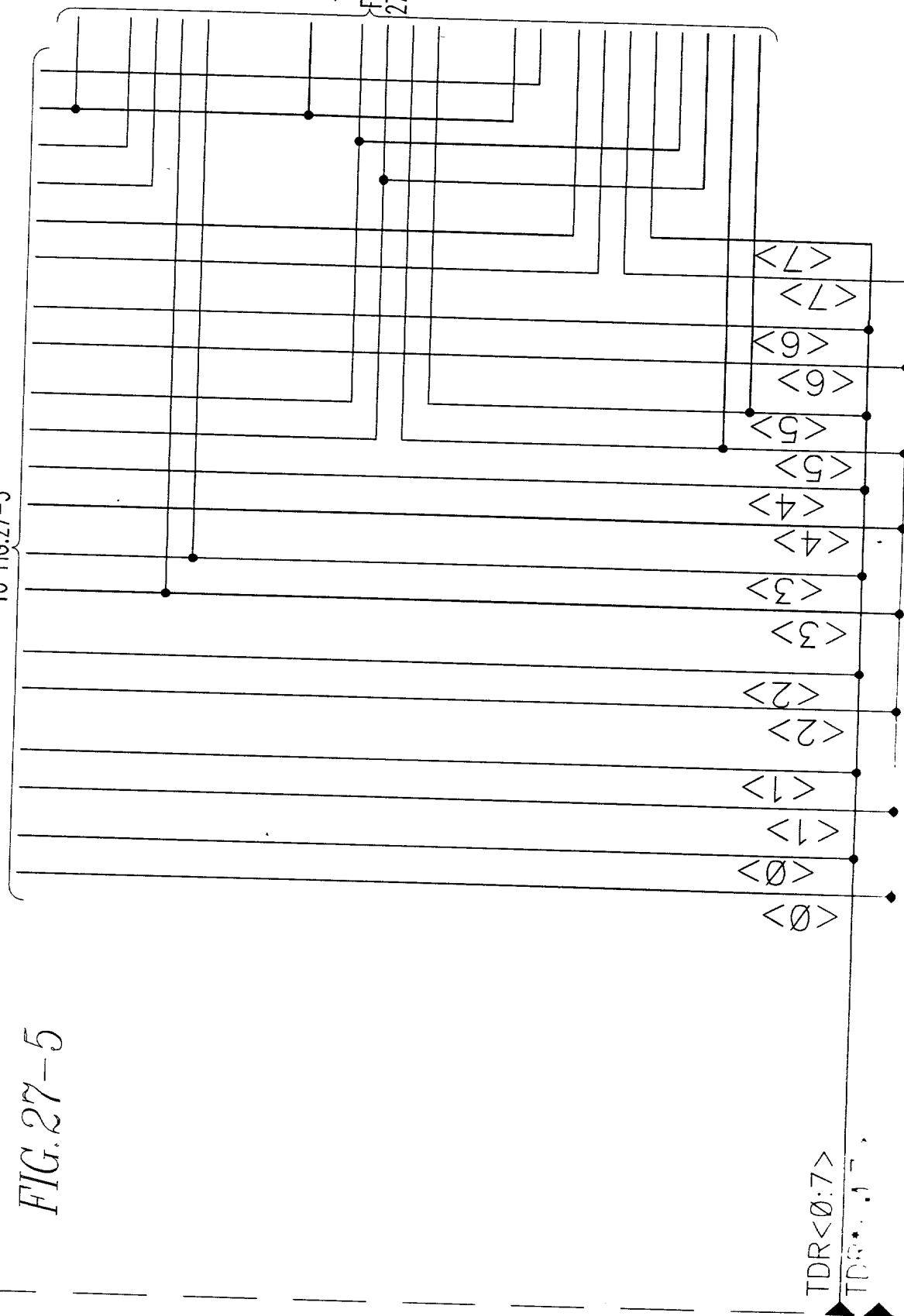
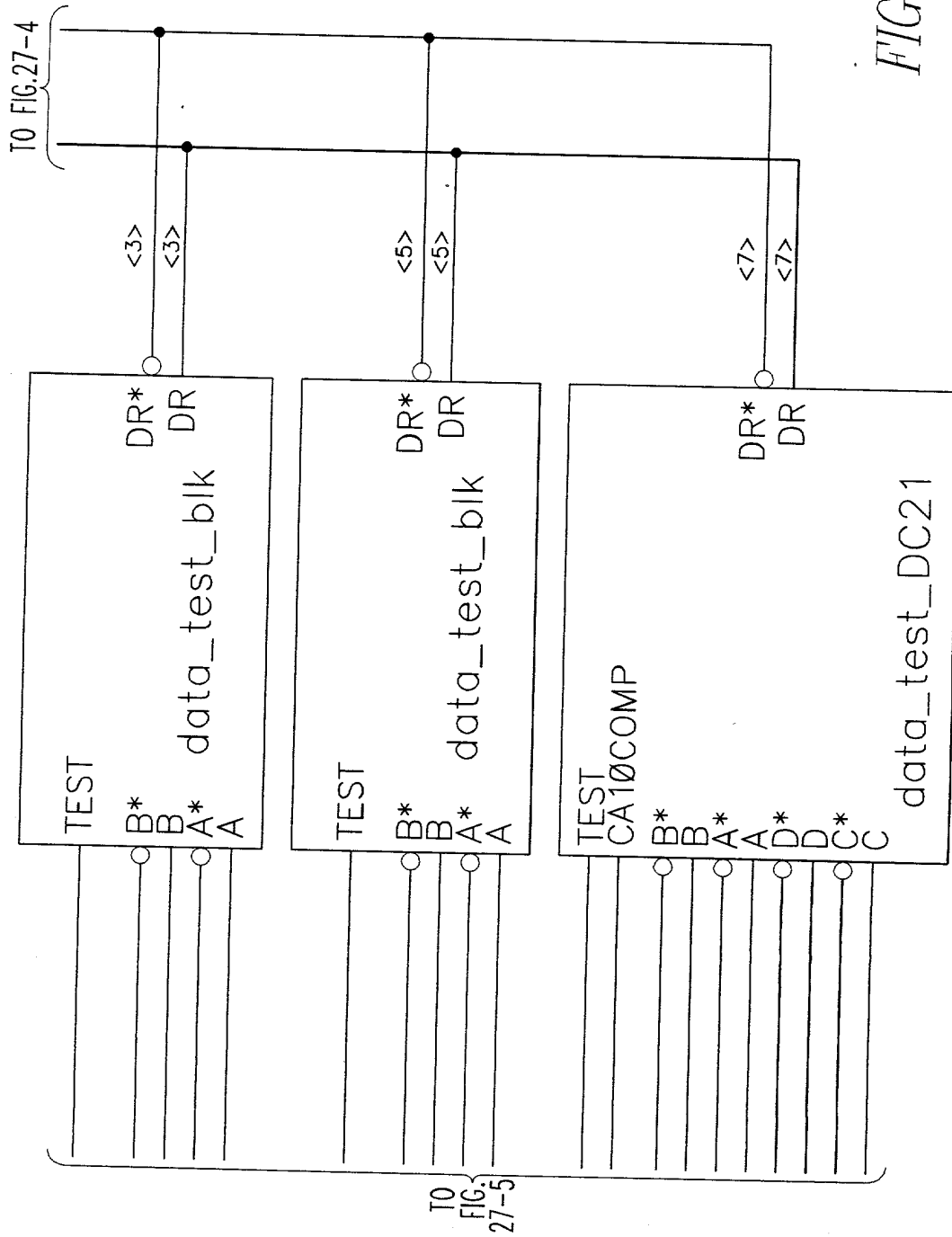


FIG. 27-6 84/367



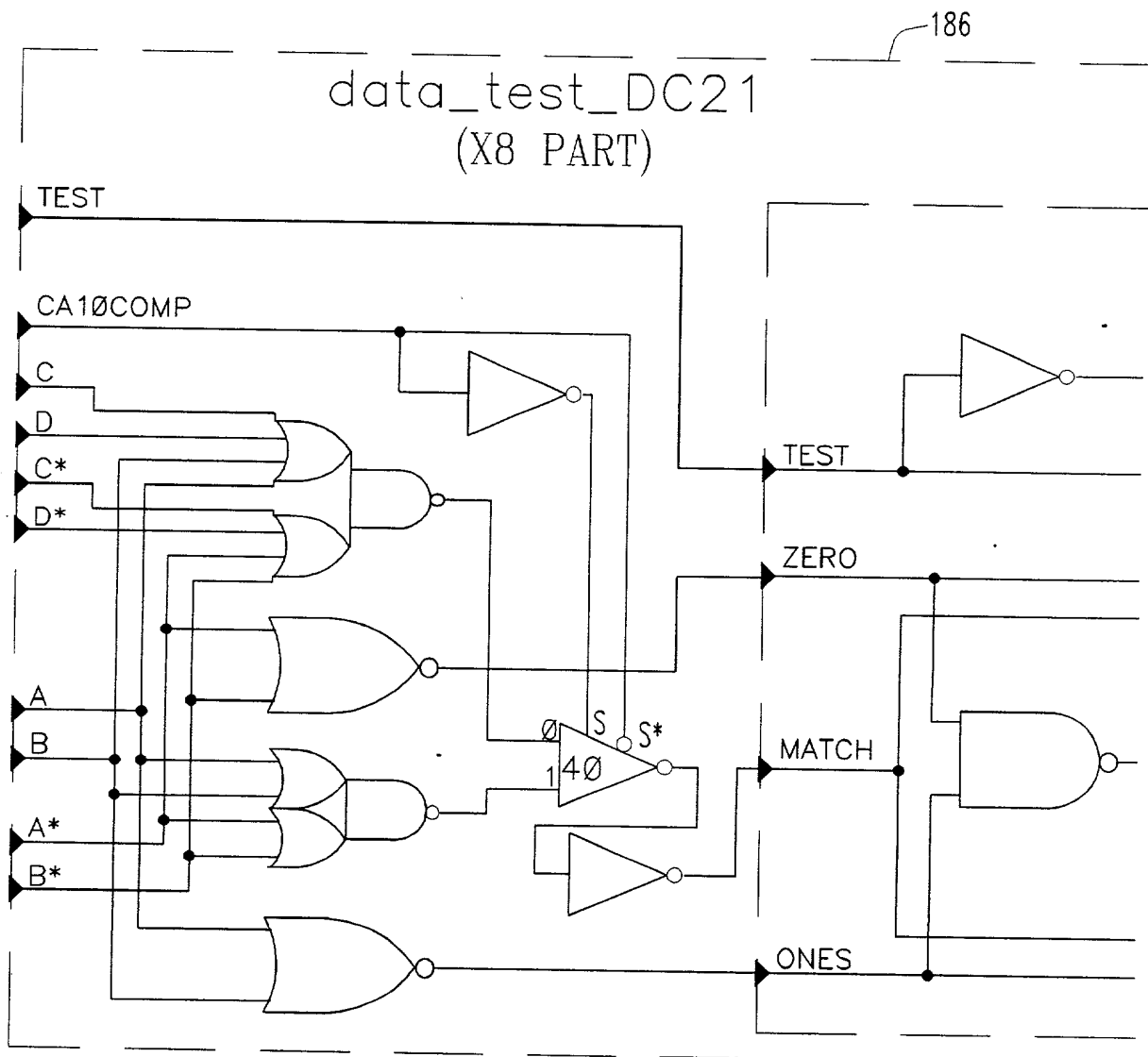


FIG. 28-1

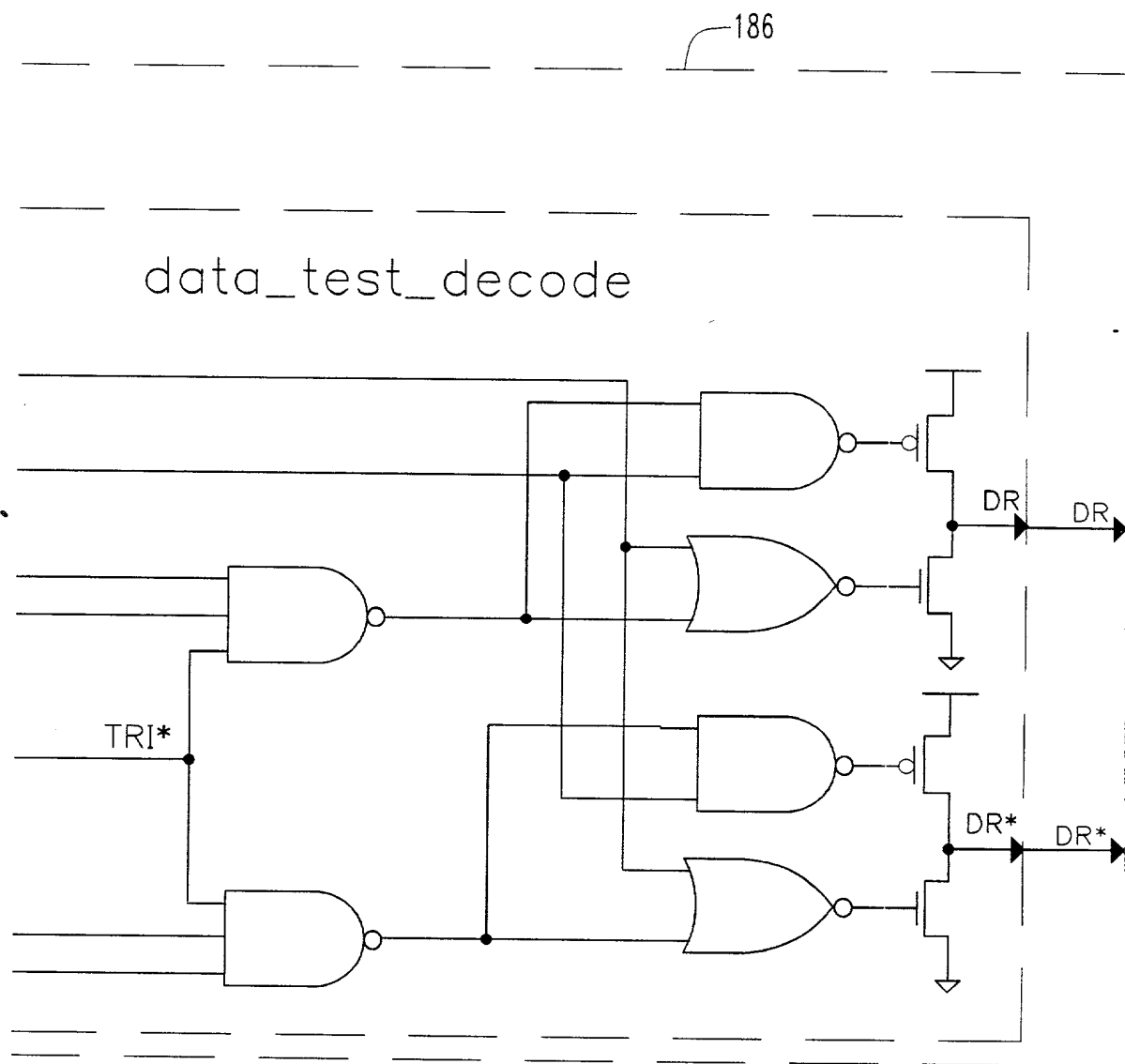


FIG. 28-2

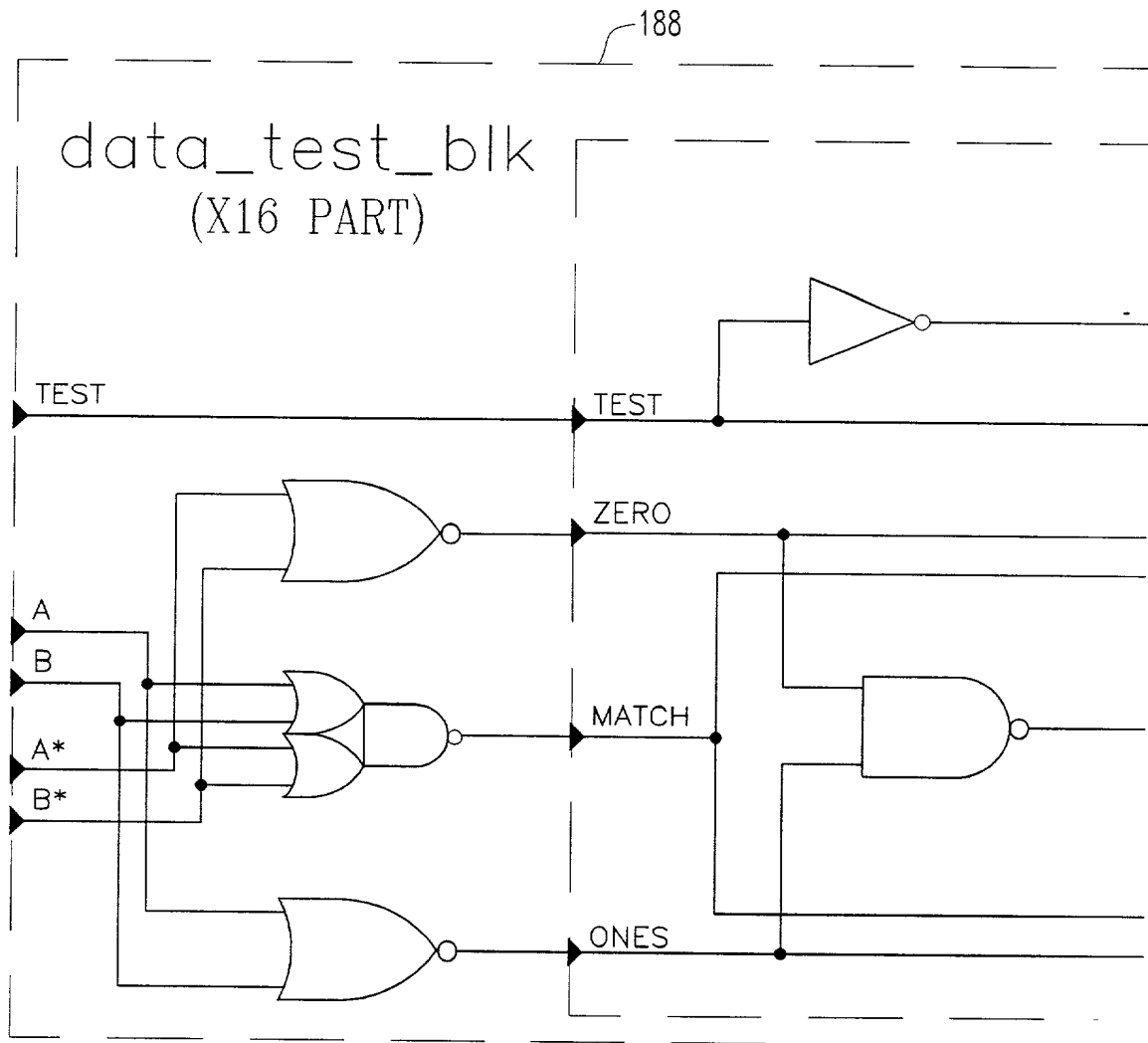


FIG. 29-1

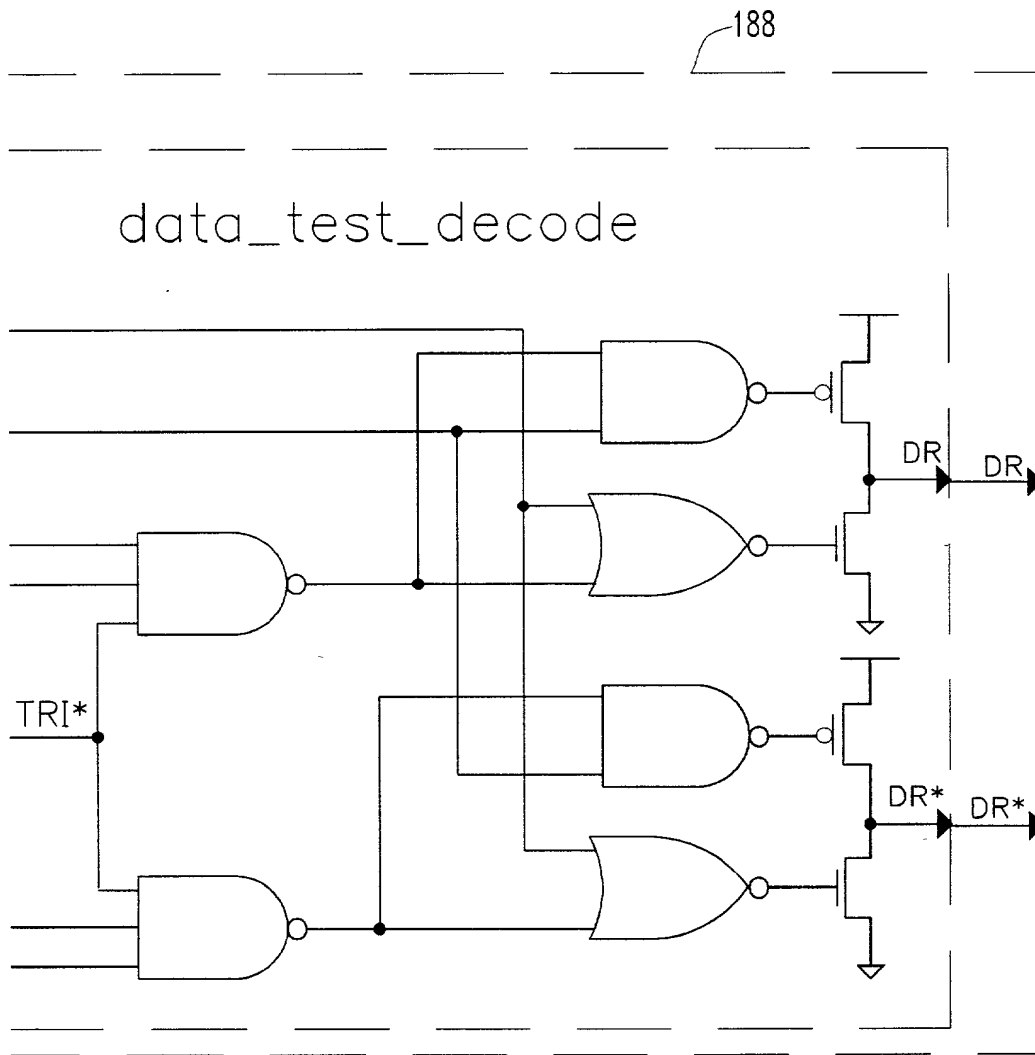
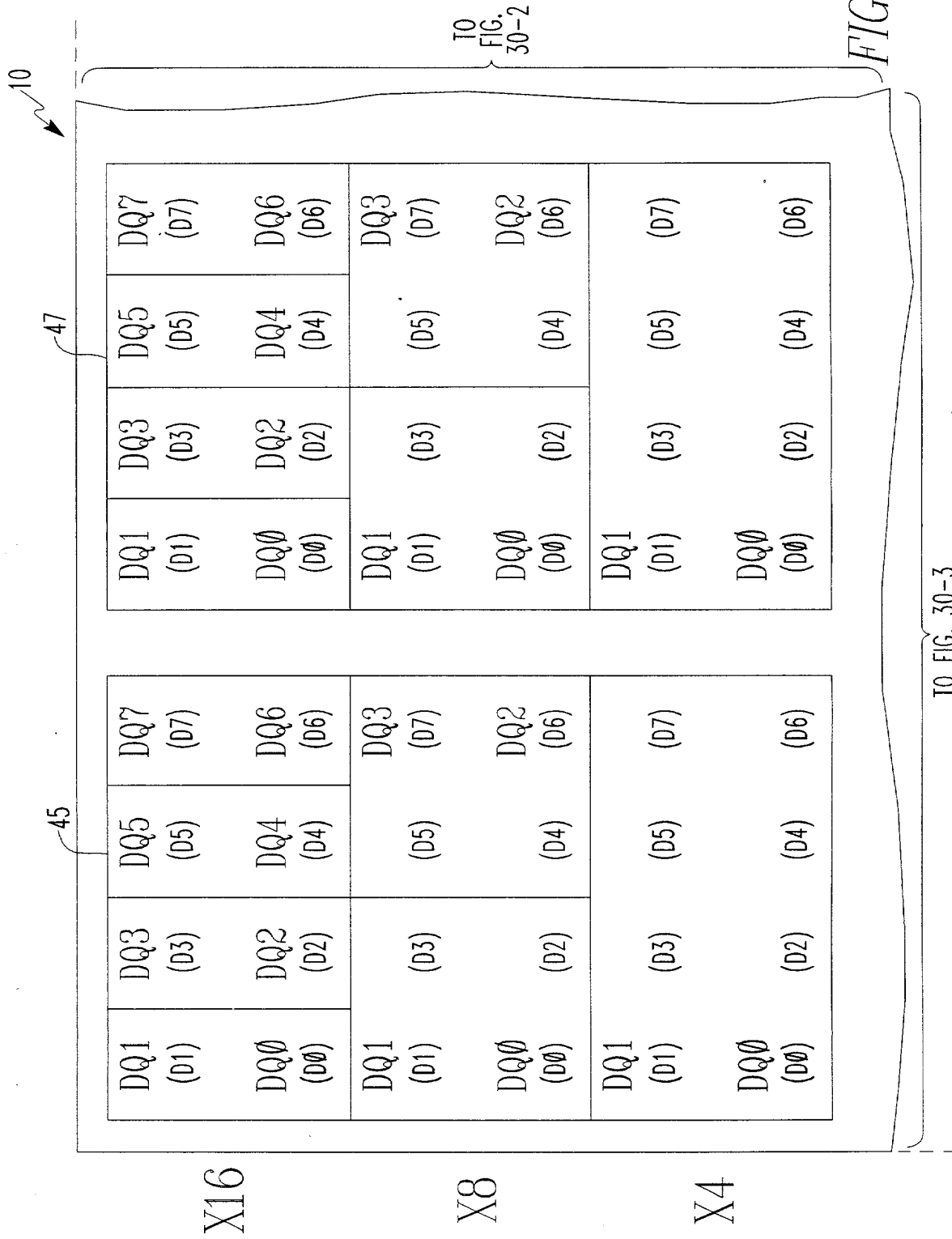
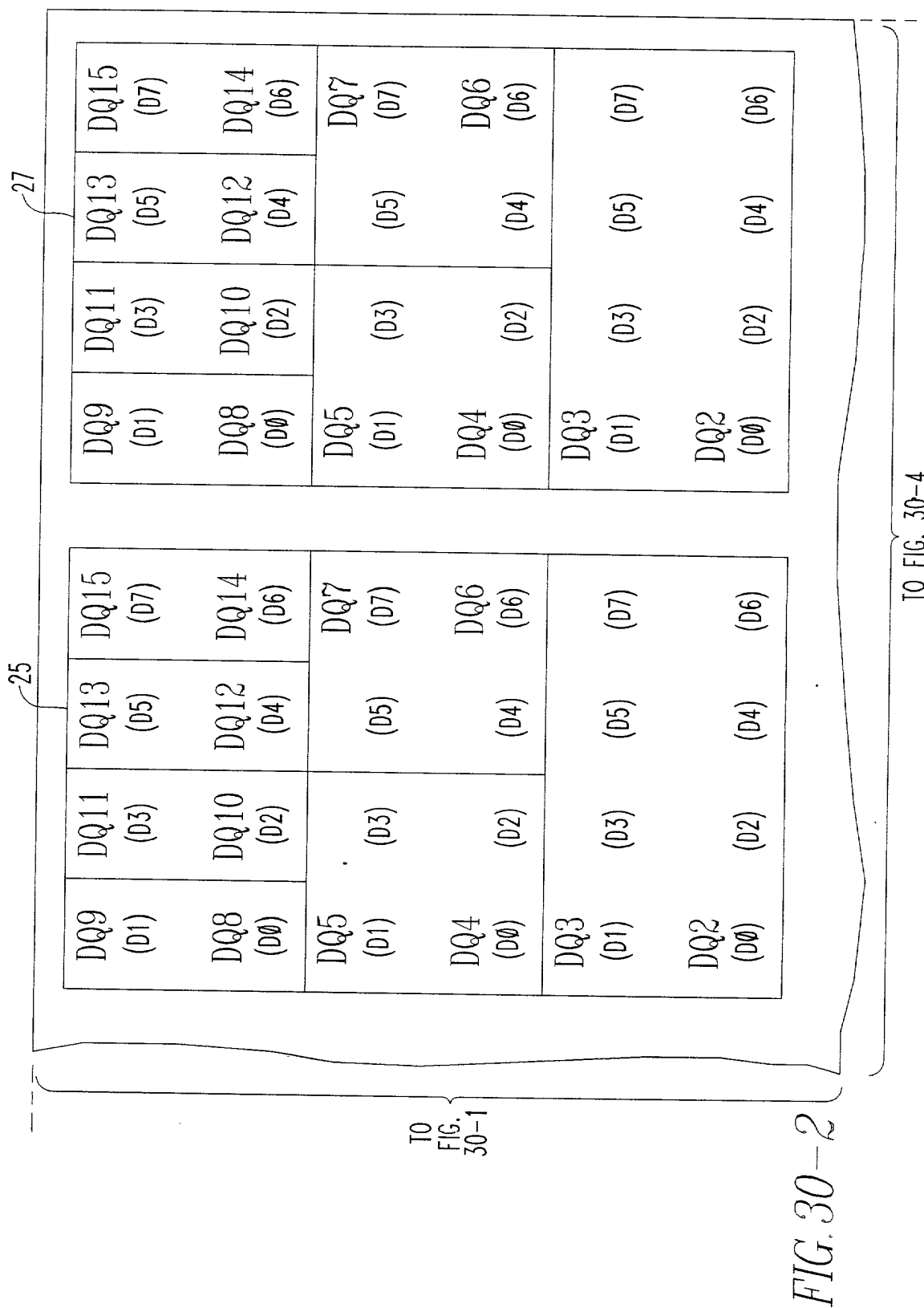


FIG. 29-2





TO FIG. 30-1

	38				40			
	(D0) DQ0	(D2) DQ2	(D4) DQ4	(D6) DQ6	(D0) DQ0	(D2) DQ2	(D4) DQ4	(D6) DQ6
X4	(D1) DQ1	(D3) DQ3	(D5) DQ5	(D7) DQ7	(D1) DQ1	(D3) DQ3	(D5) DQ5	(D7) DQ7
X8	(D0) DQ0	(D2) DQ2	(D4) DQ4	(D6) DQ6	(D0) DQ0	(D2) DQ2	(D4) DQ4	(D6) DQ6
X16	(D1) DQ1	(D3) DQ3	(D5) DQ5	(D7) DQ7	(D1) DQ1	(D3) DQ3	(D5) DQ5	(D7) DQ7

TO
FIG.
30-4

FIG. 30-3

TO FIG. 30-2

TO
FIG.
30-3

FIG. 30-1

X4	VSSQ	N/C	VSSQ	N/C	N/C	
X8	VSSQ	DQ3	VSSQ	DQ2	N/C	
X16	VSSQ	DQ7	VSSQ	DQ6	DQ5	
	1	2	3	4	5	6
X16	VCCQ	DQ0	VCCQ	DQ1	DQ2	VCCQ
X8	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C
X4	VCCQ	DQ0	VCCQ	DQ1	N/C	N/C

TO FIG. 31A2

FIG. 31A1

TO FIG. 31A1

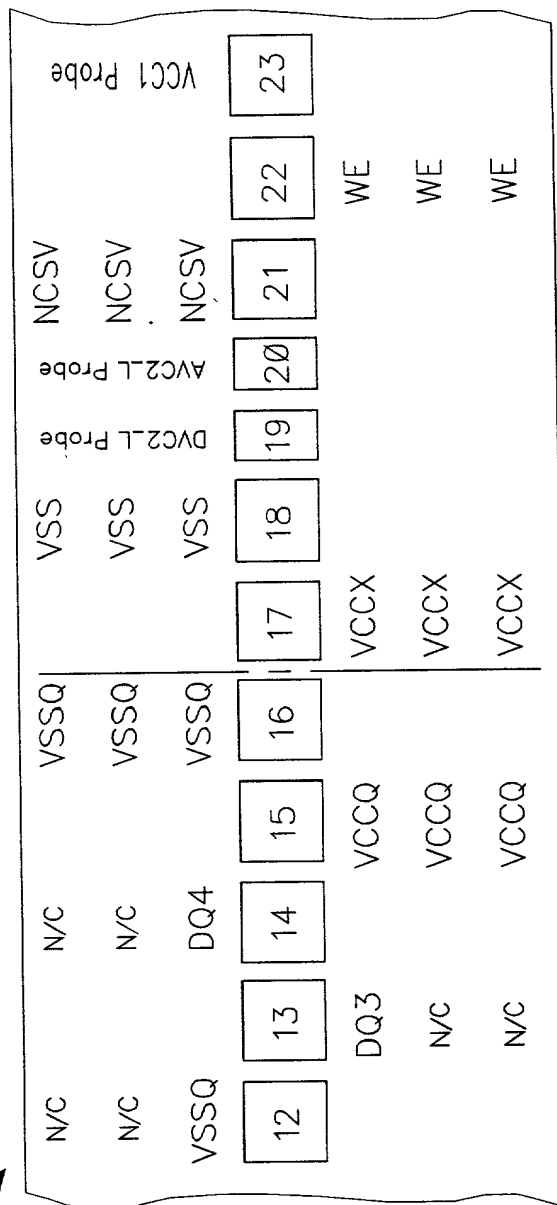
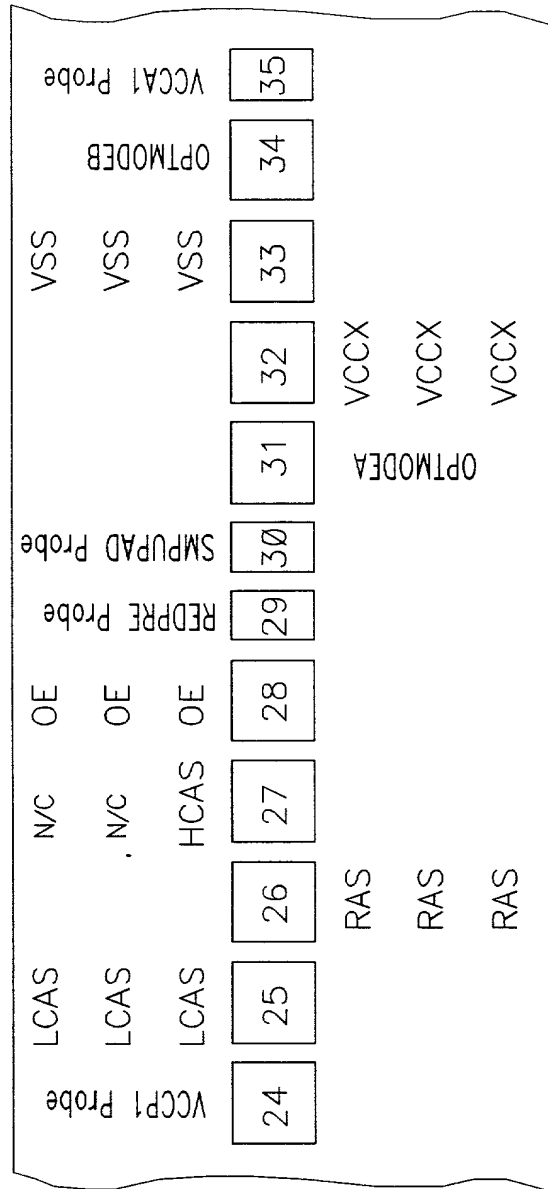


FIG. 31A2



TO FIG. 31B2

FIG. 31B1

T0 FIG. 31B1
→

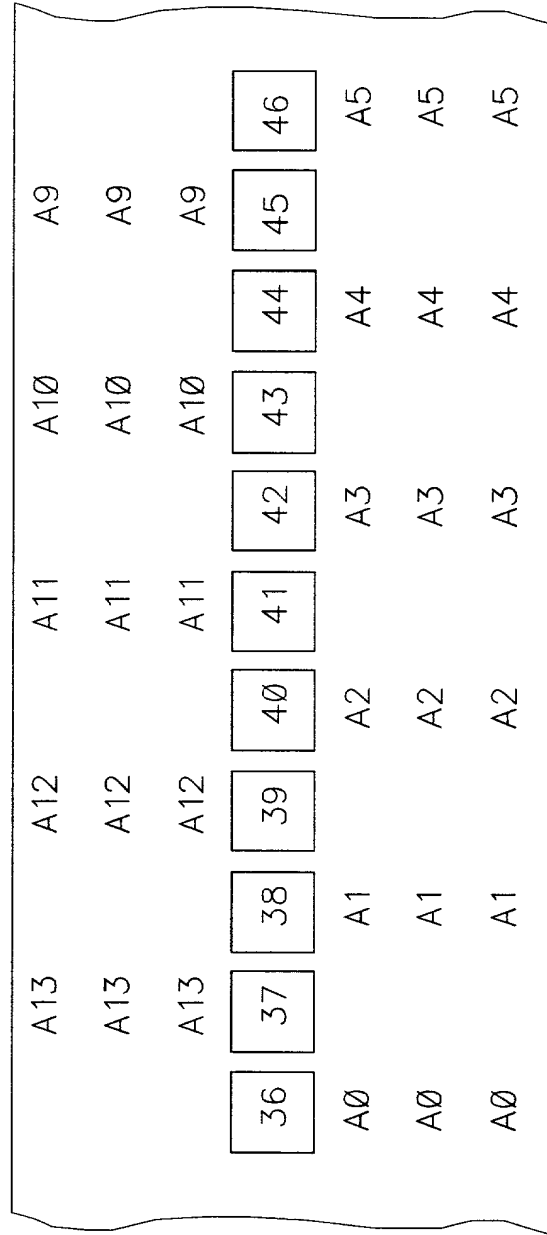


FIG. 31B2

FIG. 31B1

TO FIG. 31C1

N/C	N/C	N/C	VSSQ	N/C	VSSQ	N/C	VSSQ	VBB
N/C	DQ6	N/C	VSSQ	N/C	VSSQ	N/C	VSSQ	VBB
VSSQ	DQ14	DQ13	VSSQ	DQ12	VSSQ	VSSQ	VSSQ	VBB
60	61	62	63	64	65	66	67	68
								69
DQ9	DQ10	VCCQ	DQ11	VCCQ	VCCQ	VCCQ	VCCQ	VBB
DQ5	N/C	VCCQ	N/C	VCCQ	VCCQ	VCCQ	VCCQ	VBB
DQ3	N/C	VCCQ	N/C	VCCQ	VCCQ	VCCQ	VCCQ	VBB
								70
								71

FIG. 31C2

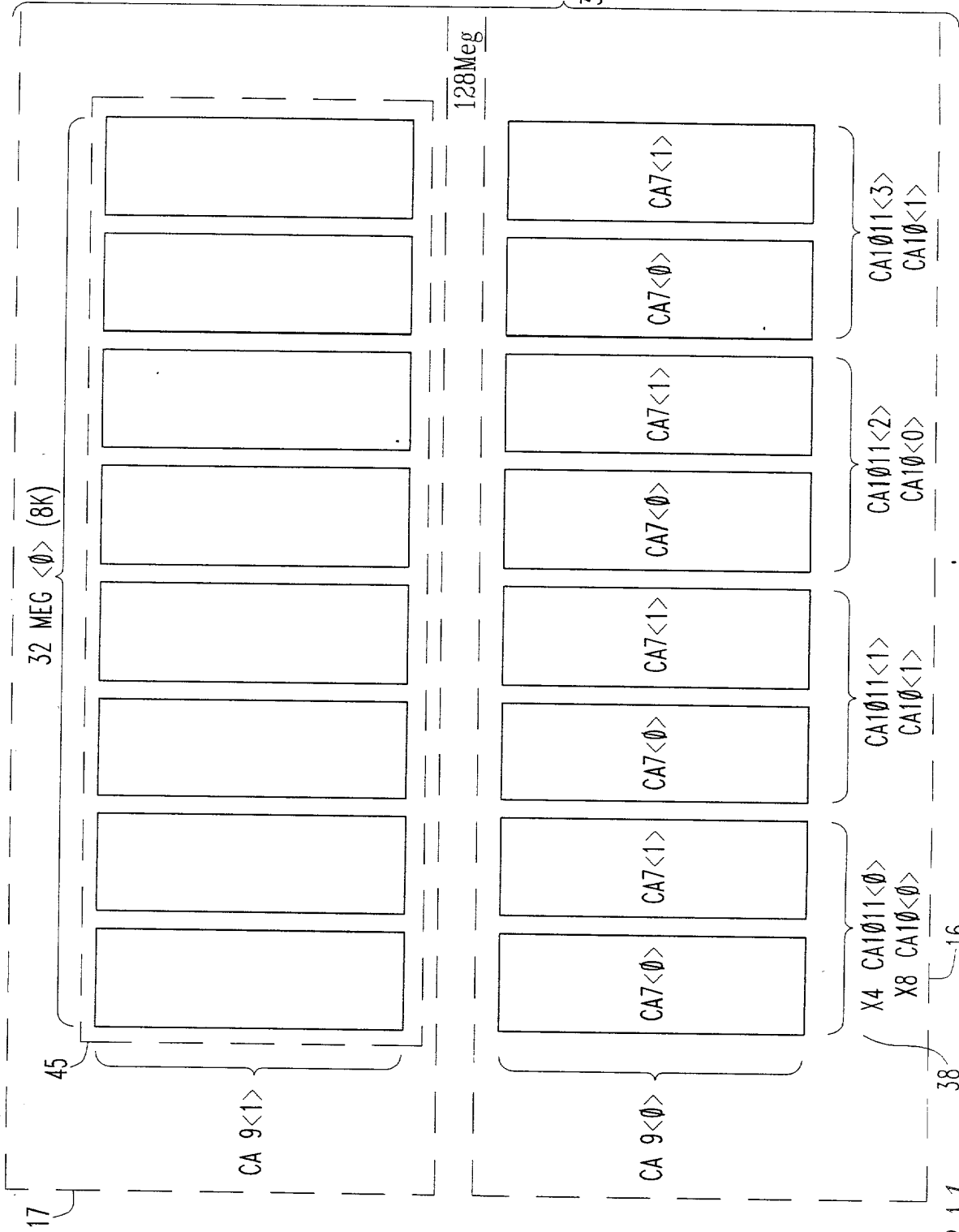
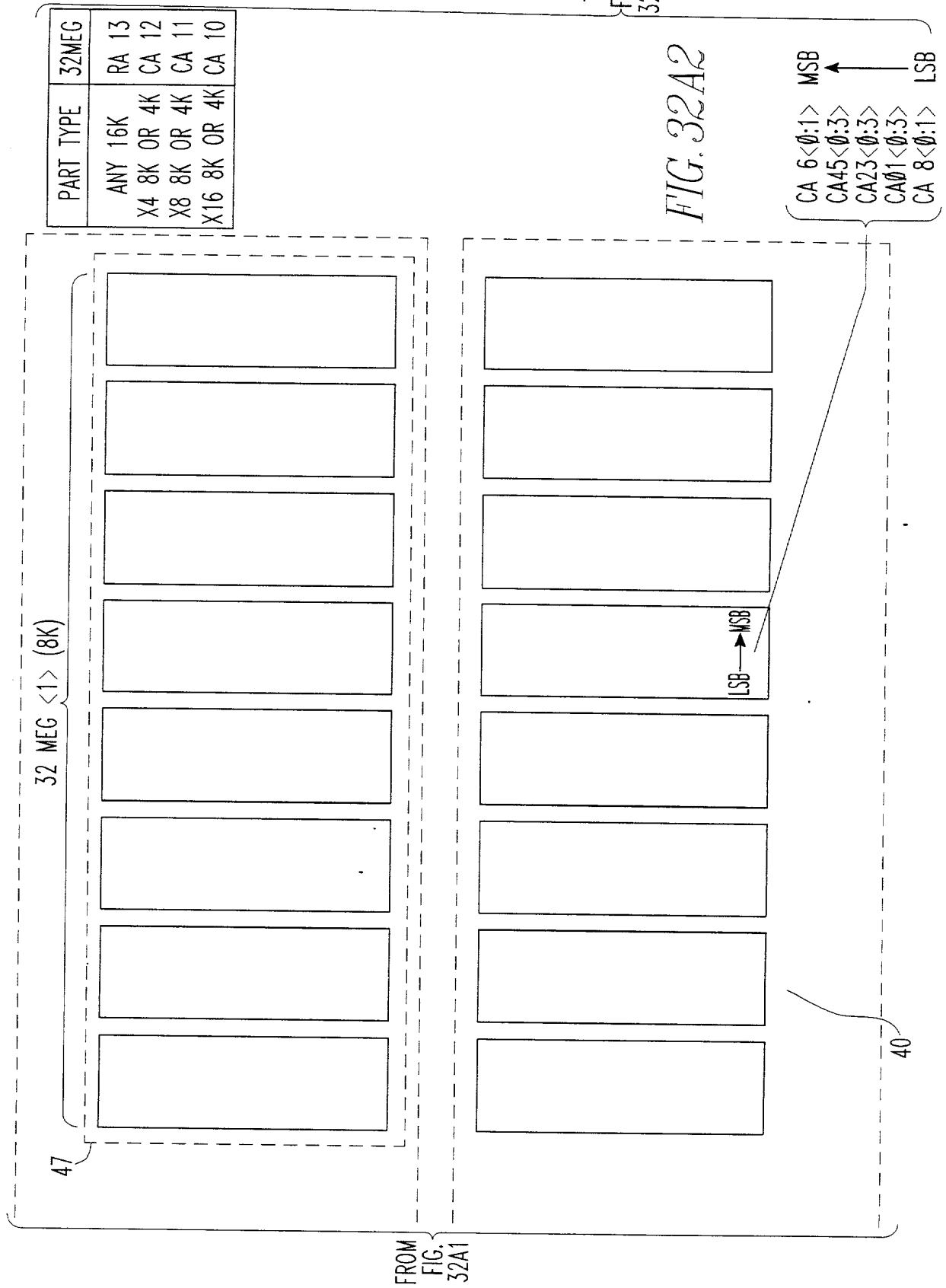
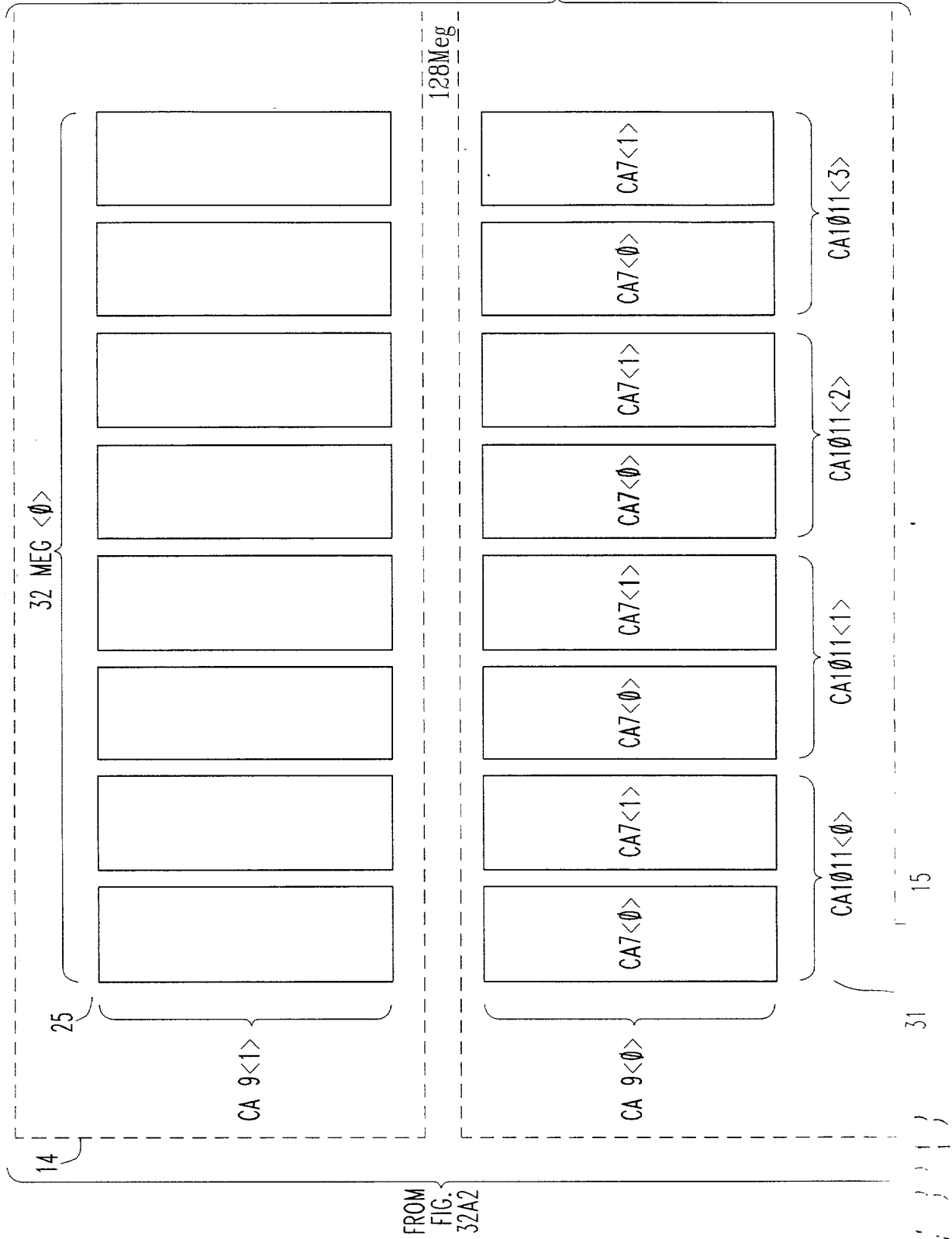


FIG 32A1

TO
FIG.
32A3





FROM
FIG.
32A2

FIG. 32A

FIG. 32A3

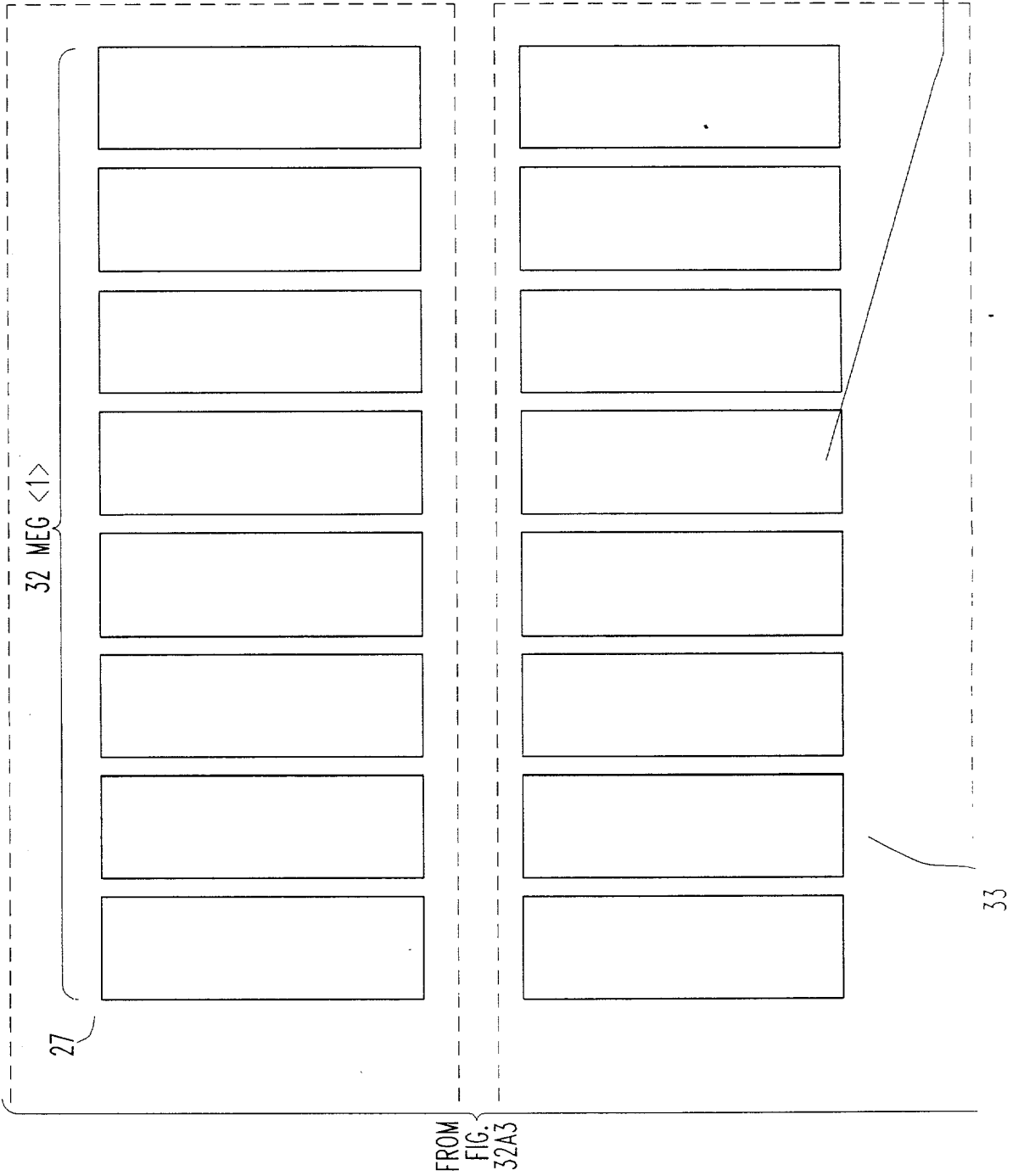


FIG. 32A4

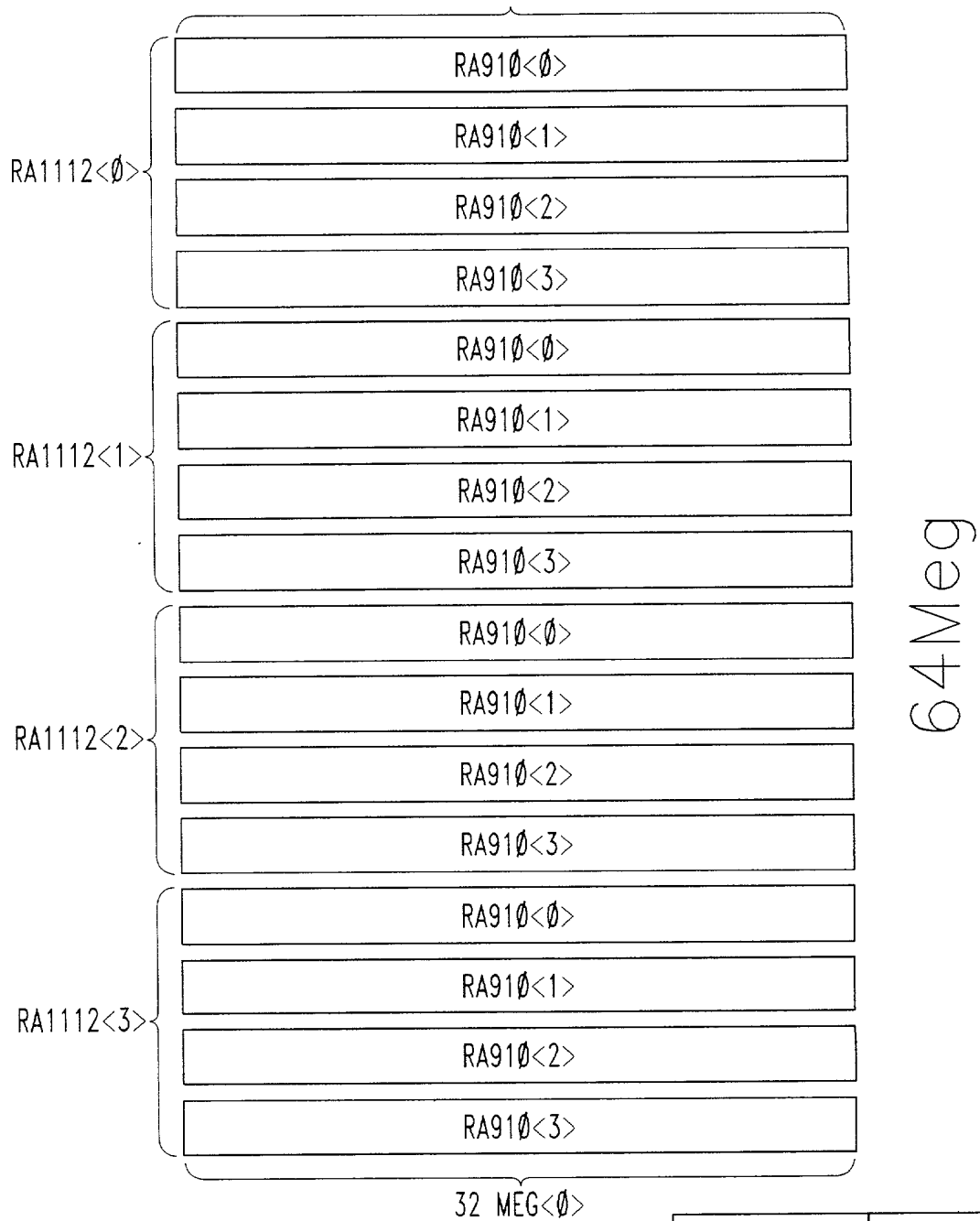


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

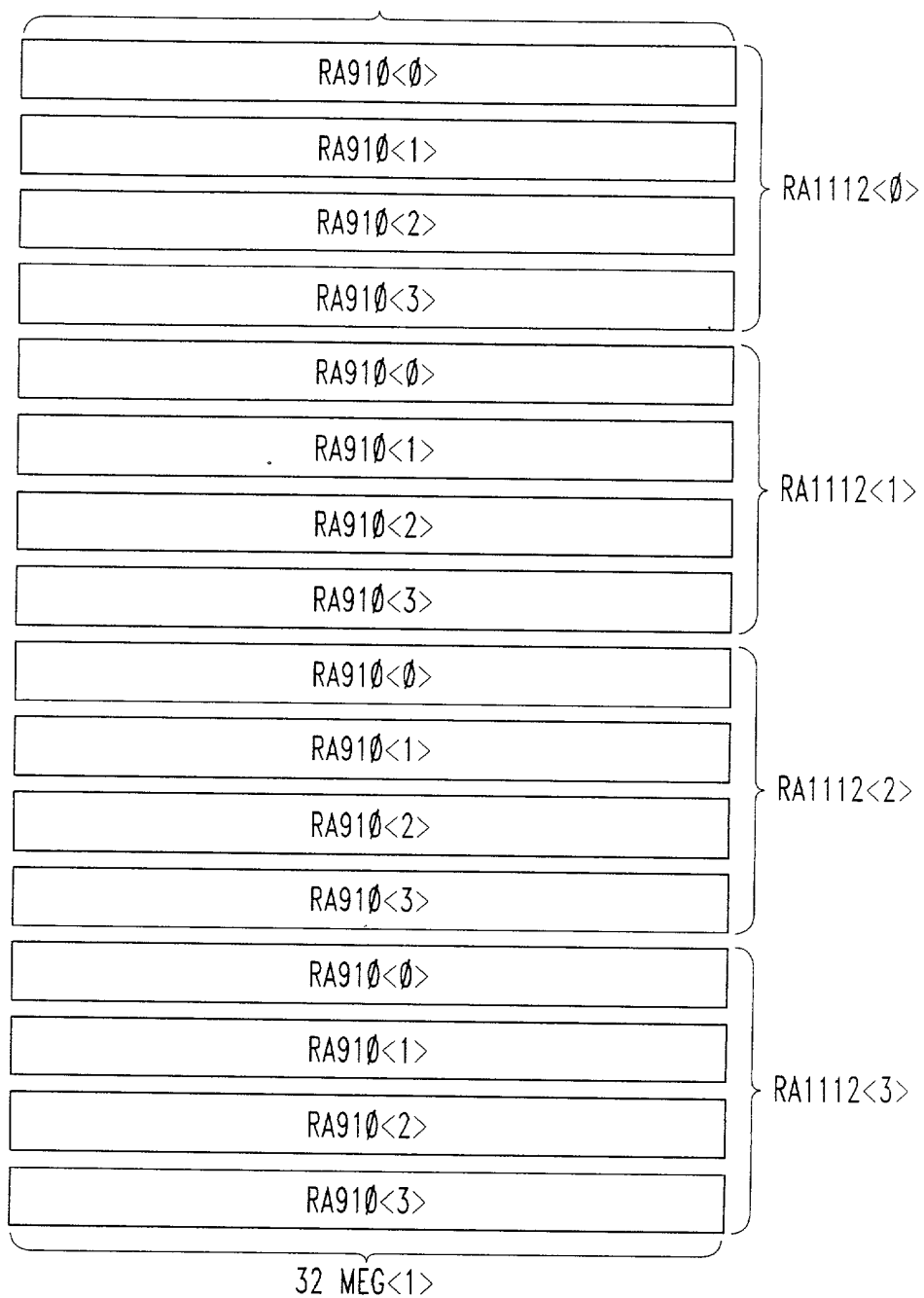
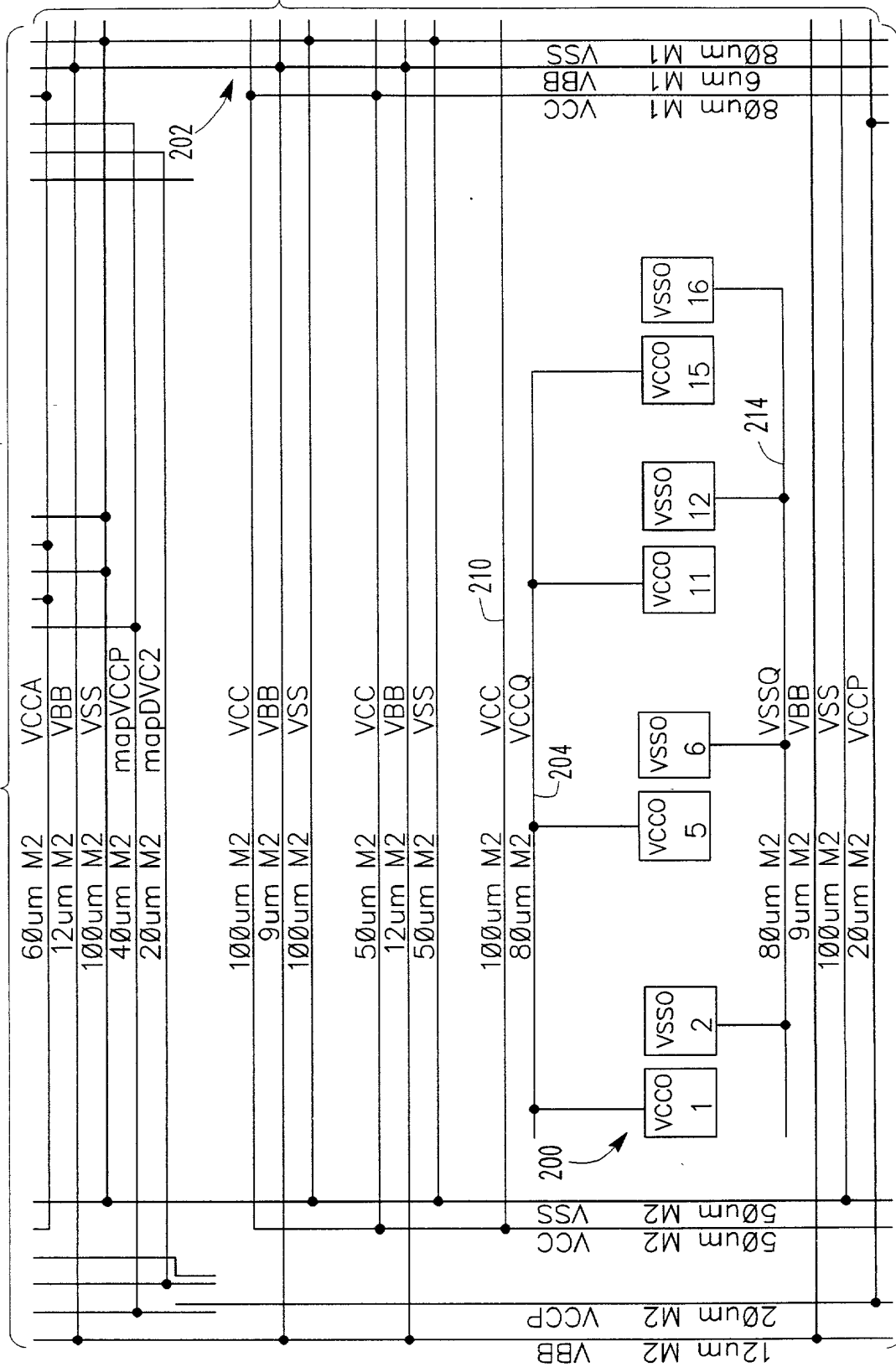


FIG. 32B2



FIG. 33A1

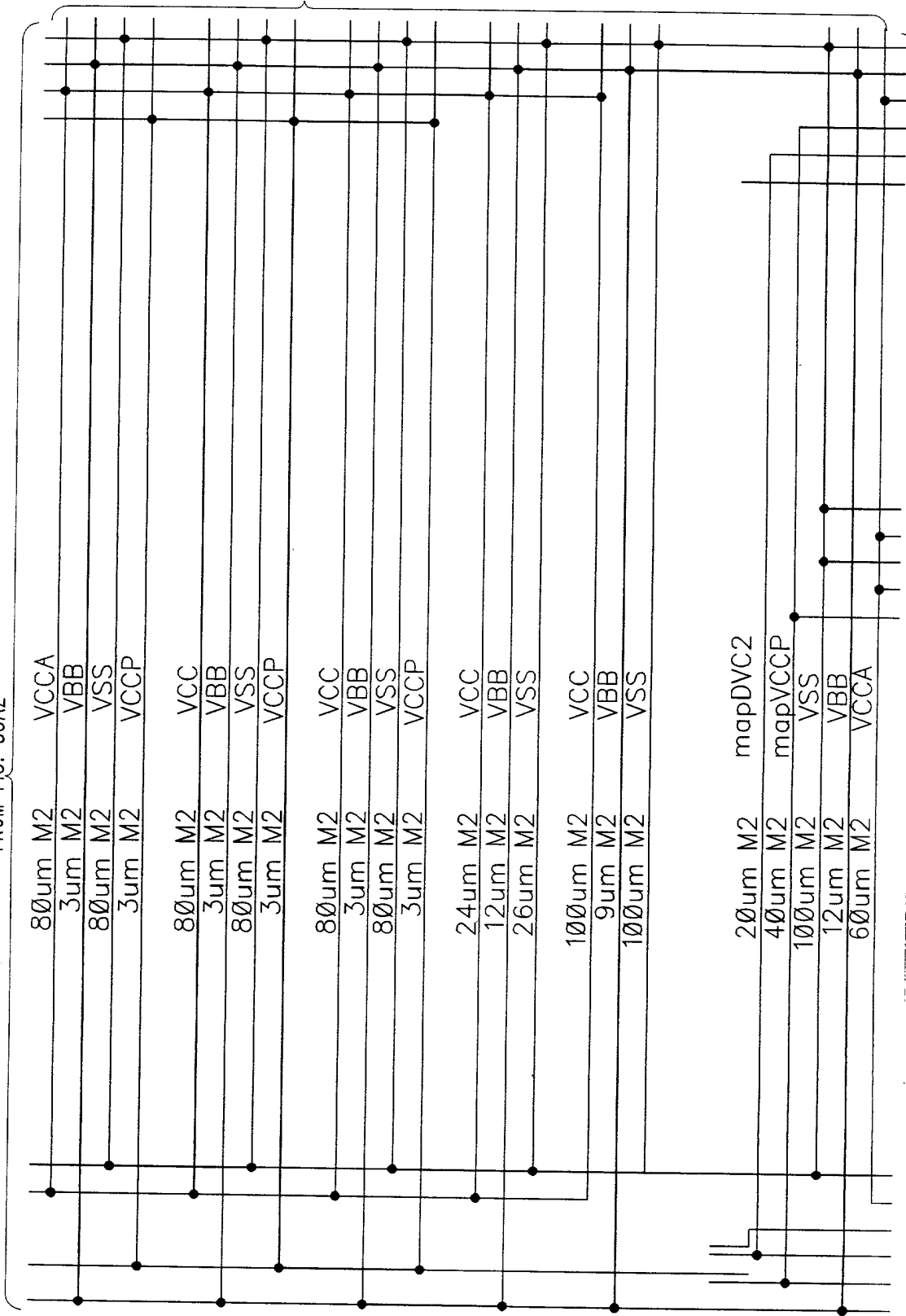
FROM FIG. 33A1



TO FIG. 33A3

FIG. 33A2

FROM FIG. 33A2



TO
FIG.
33B5

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TO FIG. 33A4

FIG. 33A3

FROM FIG. 33A3

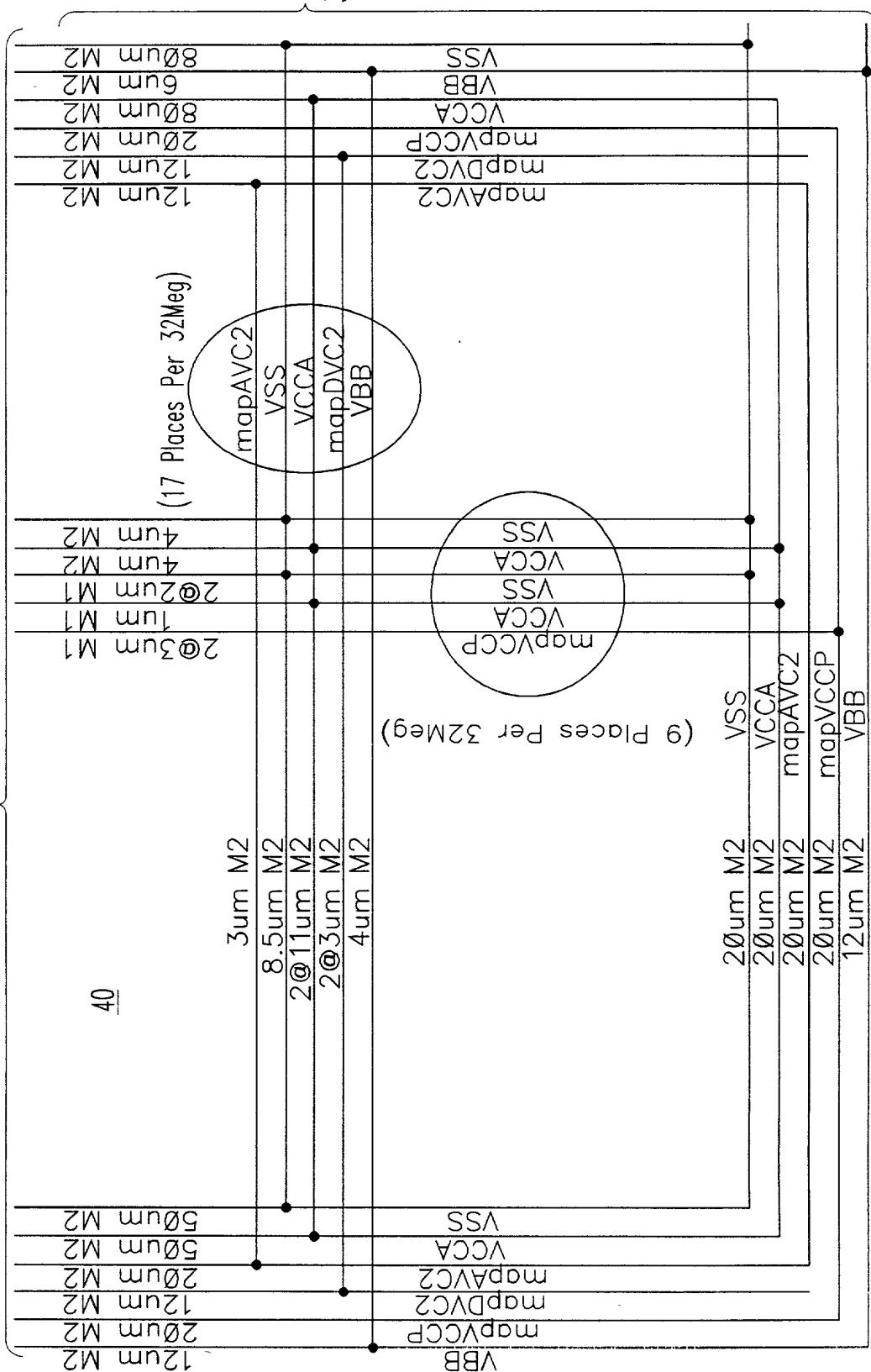
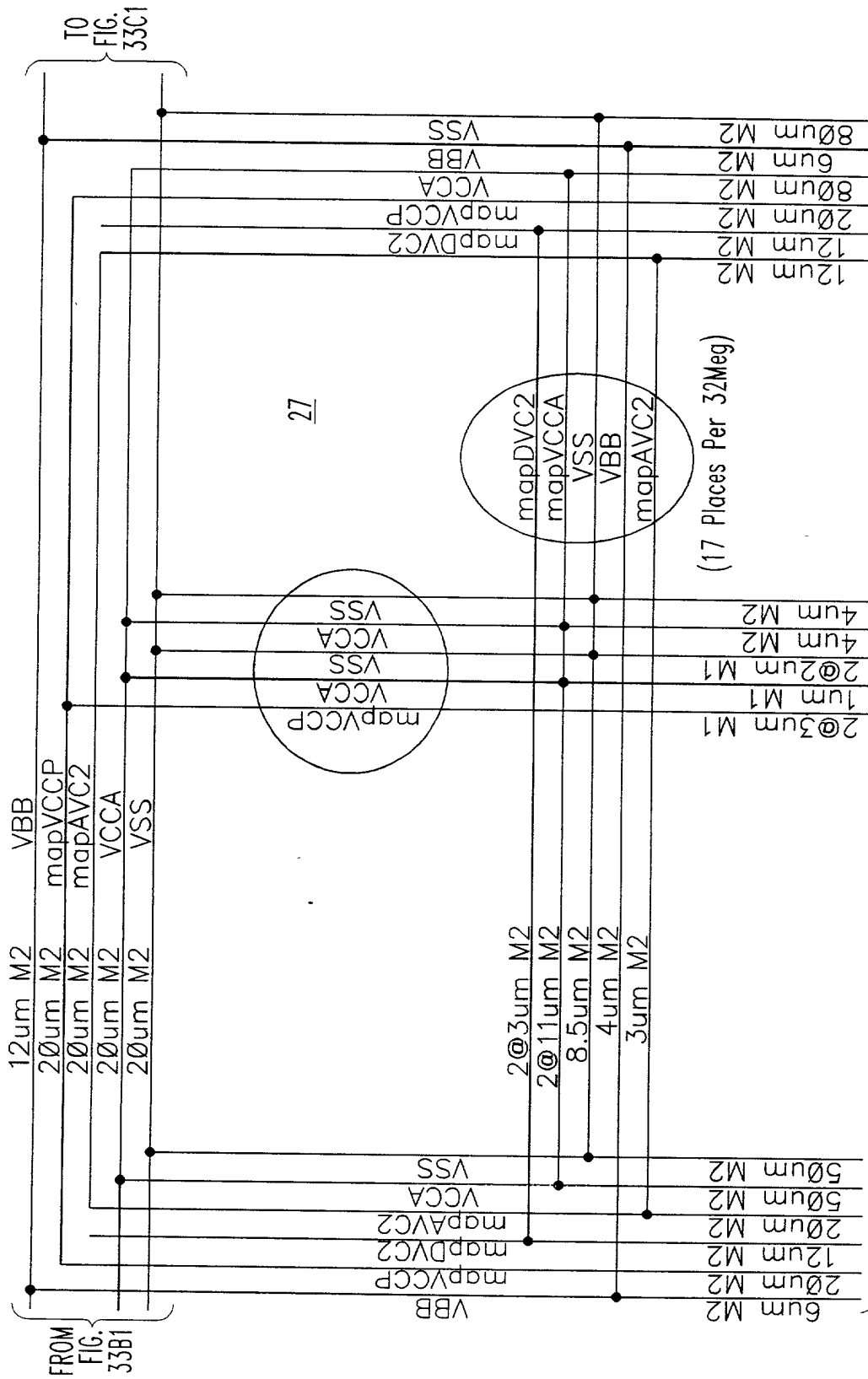


FIG. 33A4

TO FIG. 33B3

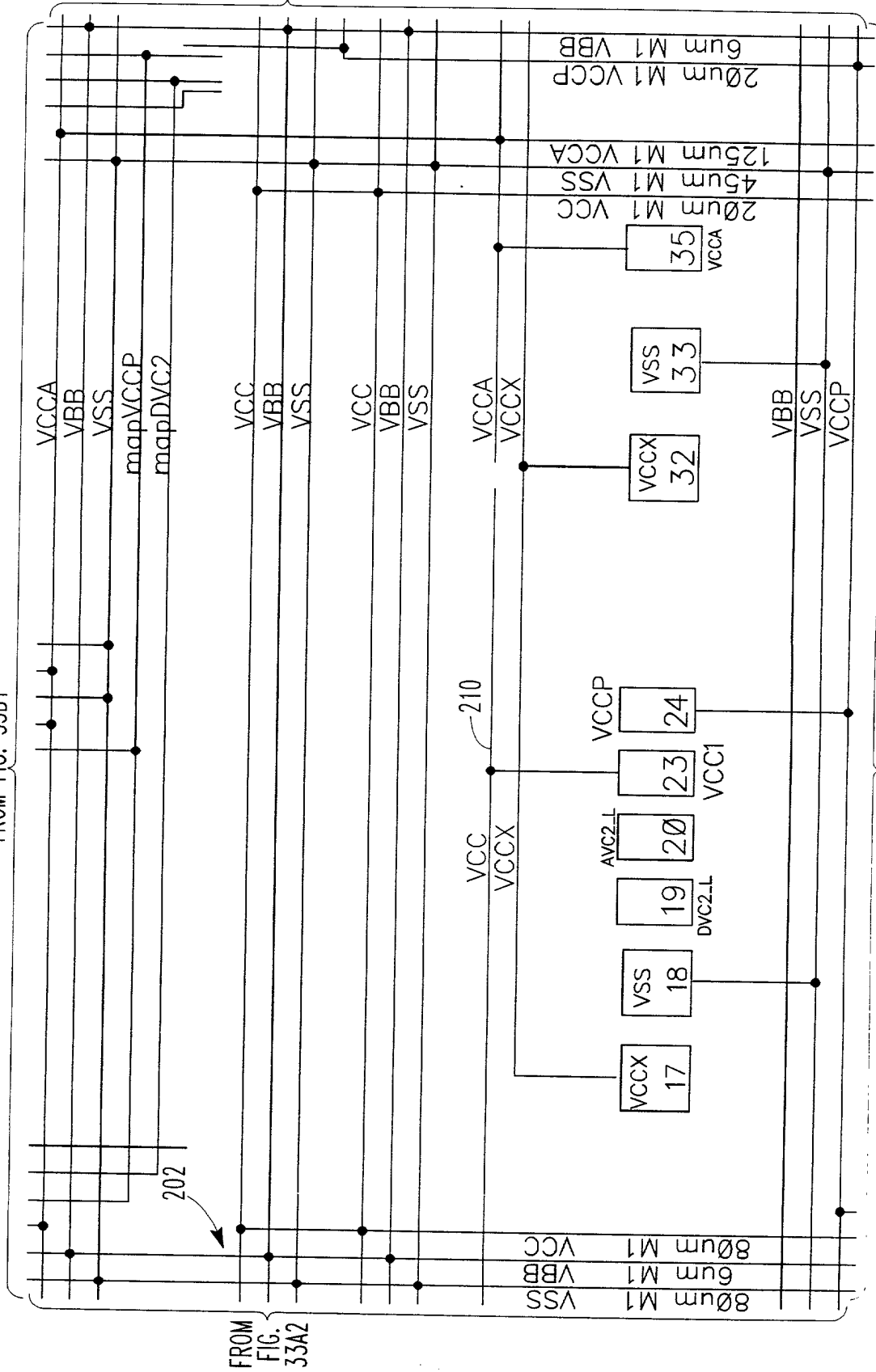
FIG. 33B1



TO FIG. 33B4

FIG. 33B2

FROM FIG. 33B1



FROM
FIG.
33A2

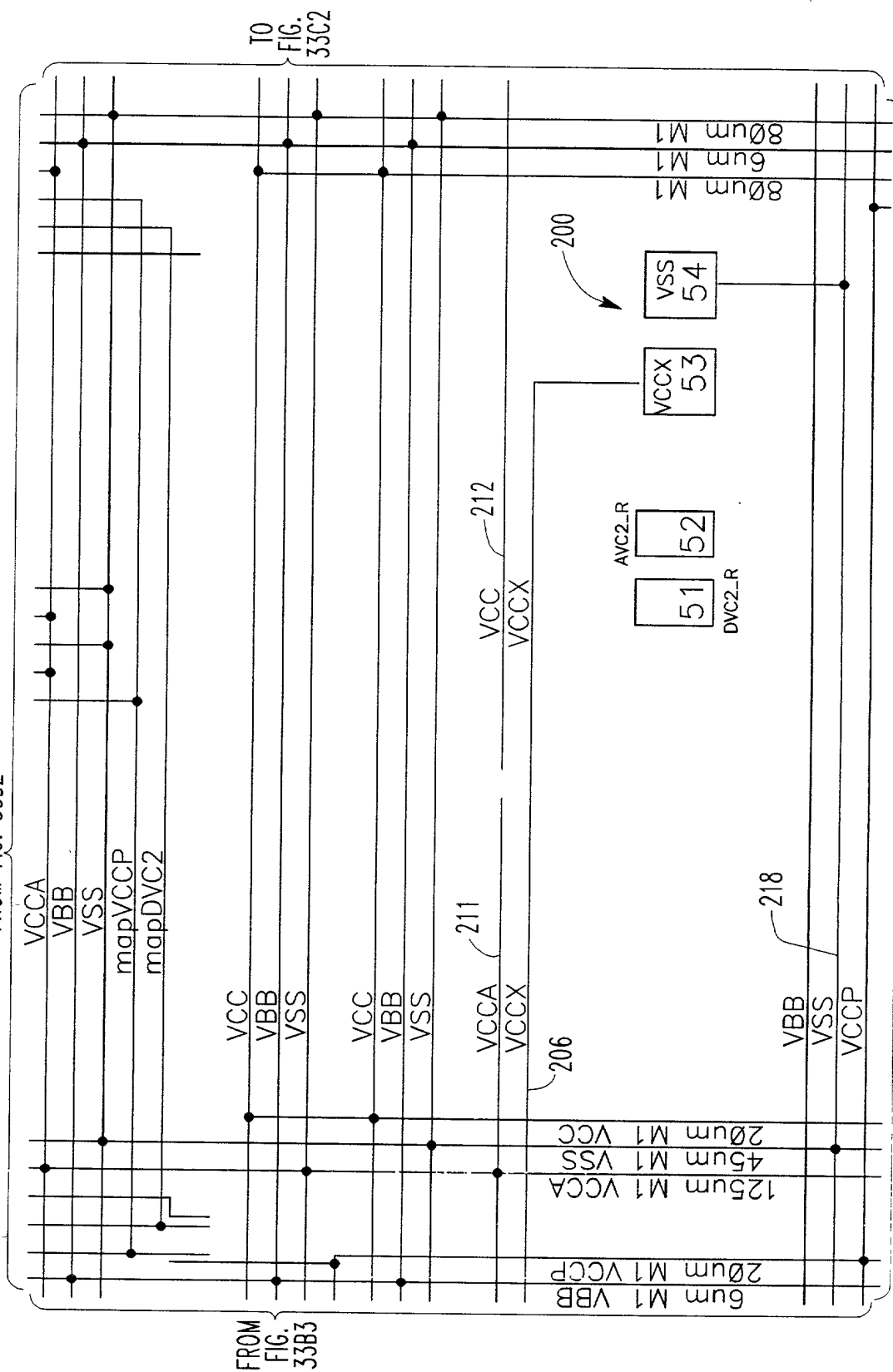
TO
FIG.
33B4

TO FIG. 33B3

FIG. 33B3

FIG. 33B4

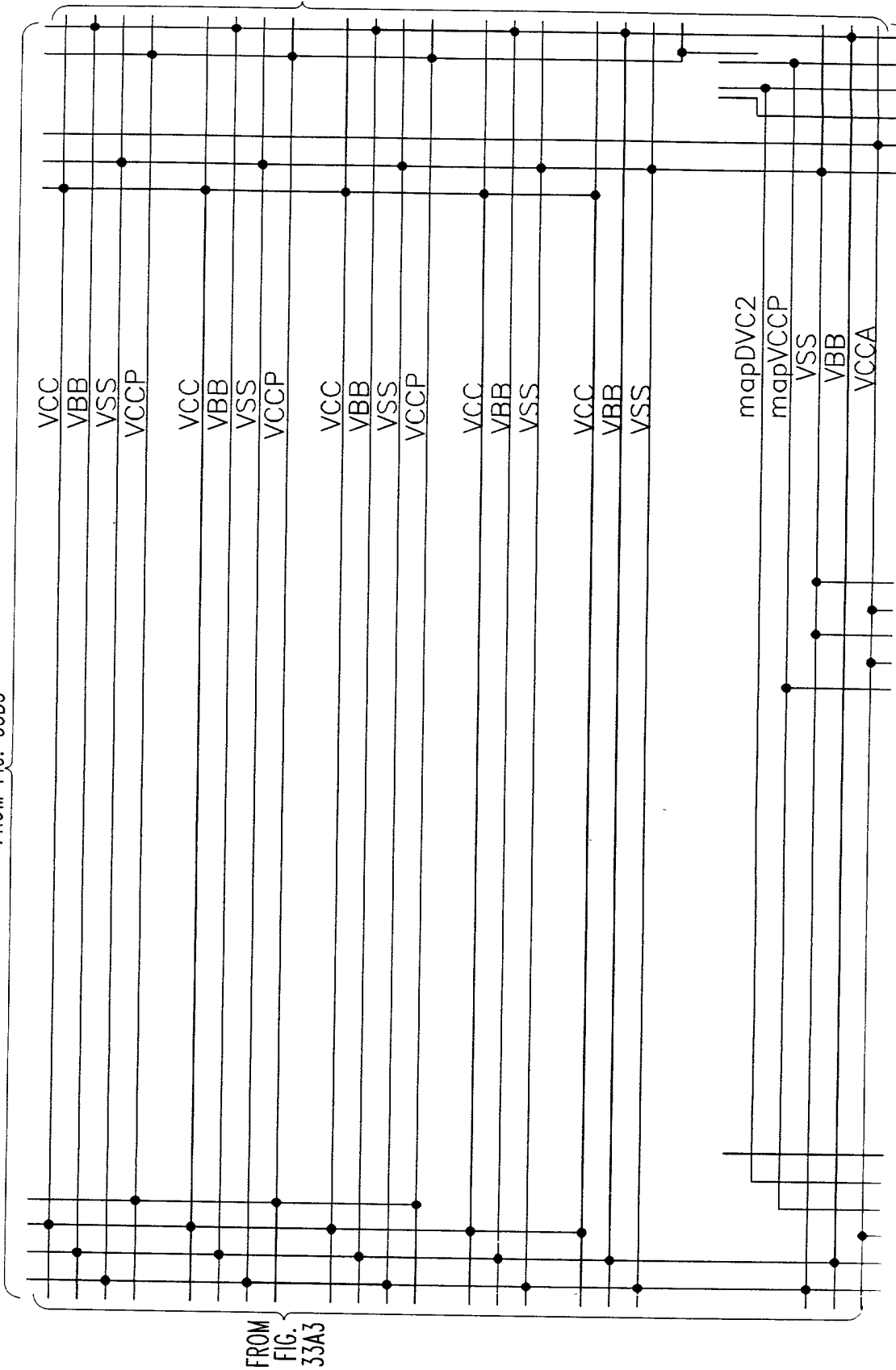
FROM FIG. 33B2



TO FIG. 33B6

FIG. 33B4

FROM FIG. 33B3

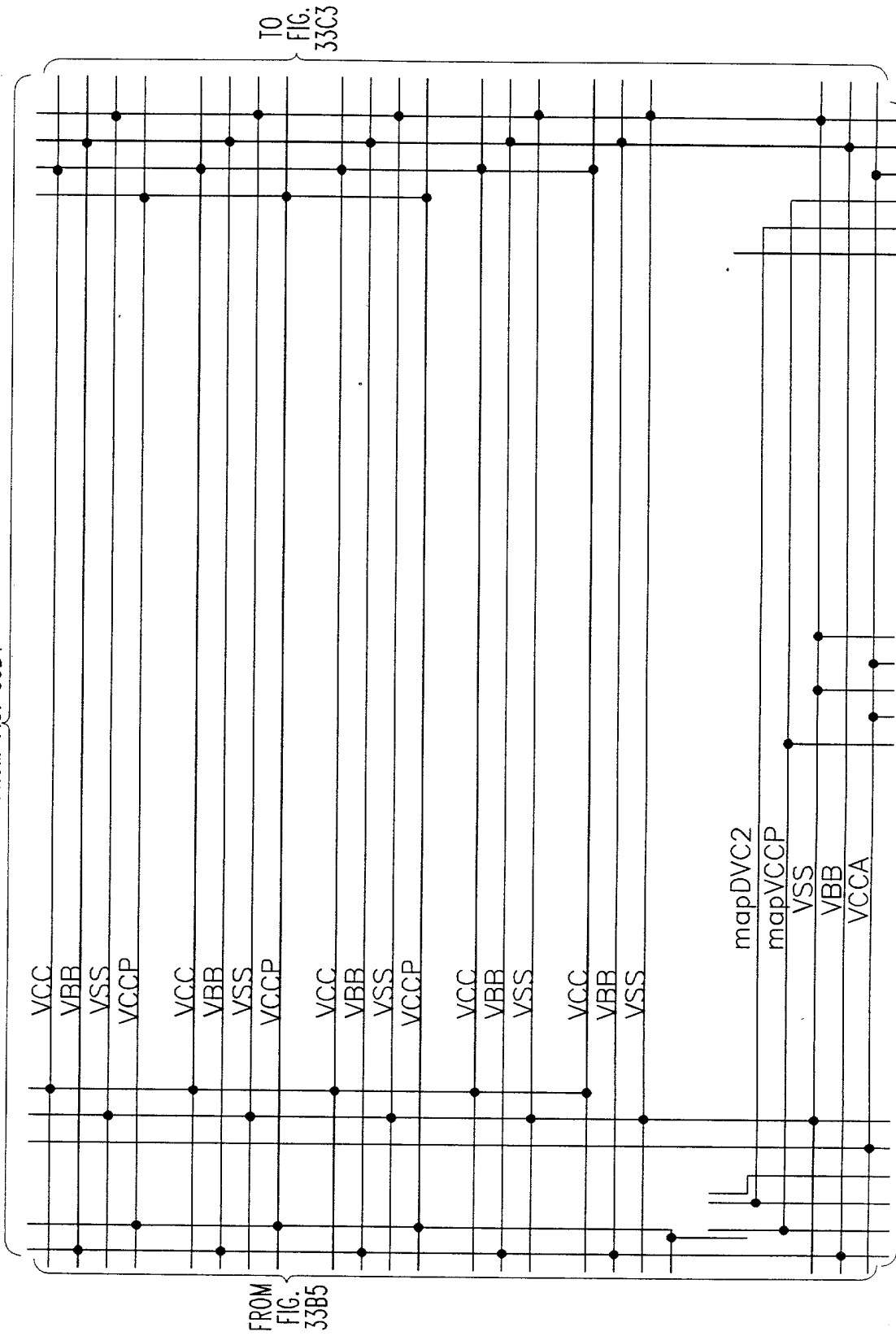


TO FIG. 33B7

FIG. 33B5

FIG. 33B6

FROM FIG. 33B4



TO FIG. 33B8

FIG. 33B6

38

(17 Places Per 32Meg)

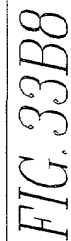
(9 Places Per 32Meg)

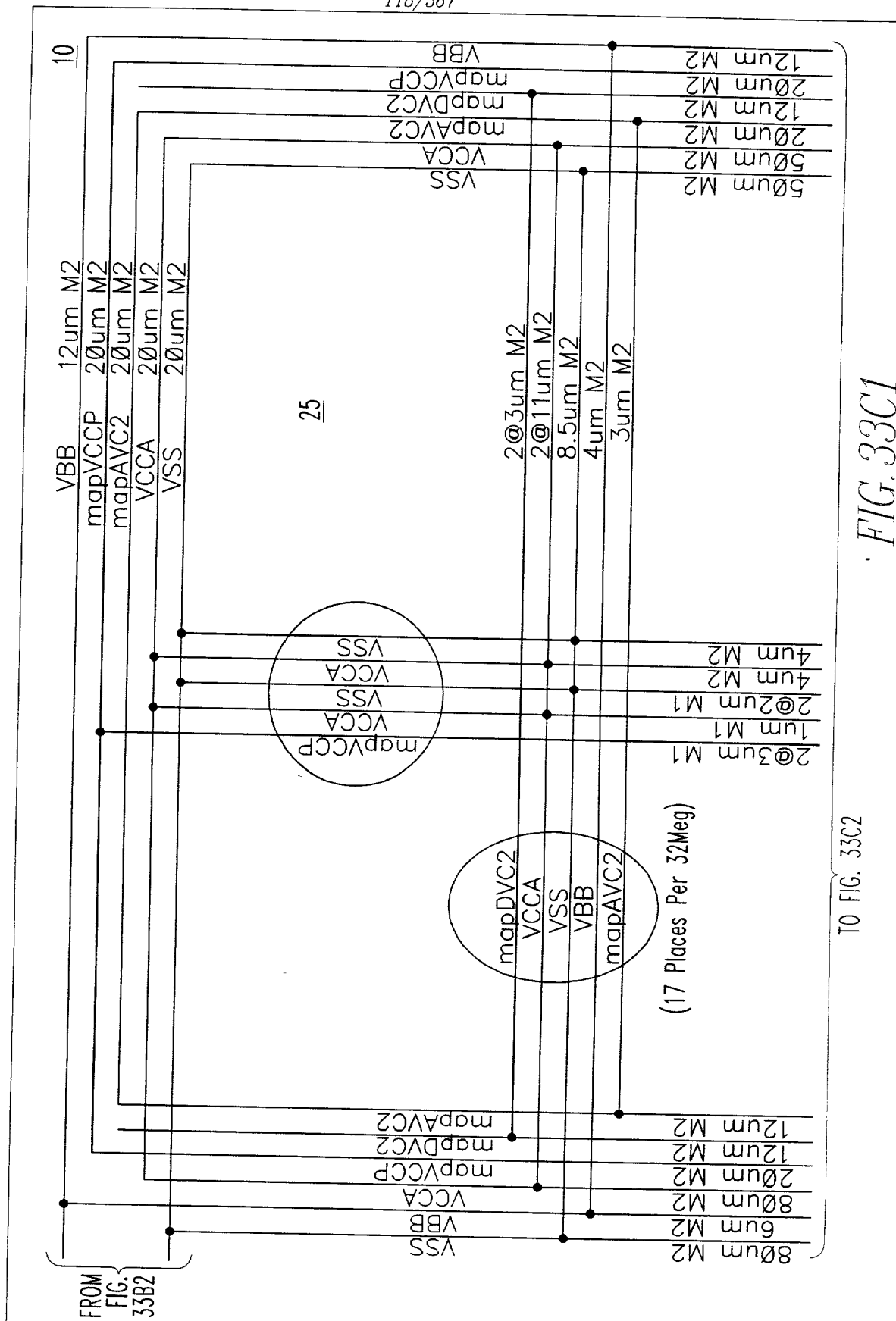
Figure 1 illustrates a 32Mbit memory array layout. The diagram shows a grid of memory cells with various control lines and labels. Labels include mapAVC2, VSS, VCCA, mapDVC2, VBB, mapVCCP, and VBB. Dimensions are given in micrometers (um) and millimeters (mm).

FROM
FIG.
33A4

FIG. 33B8

FIG. 33B7

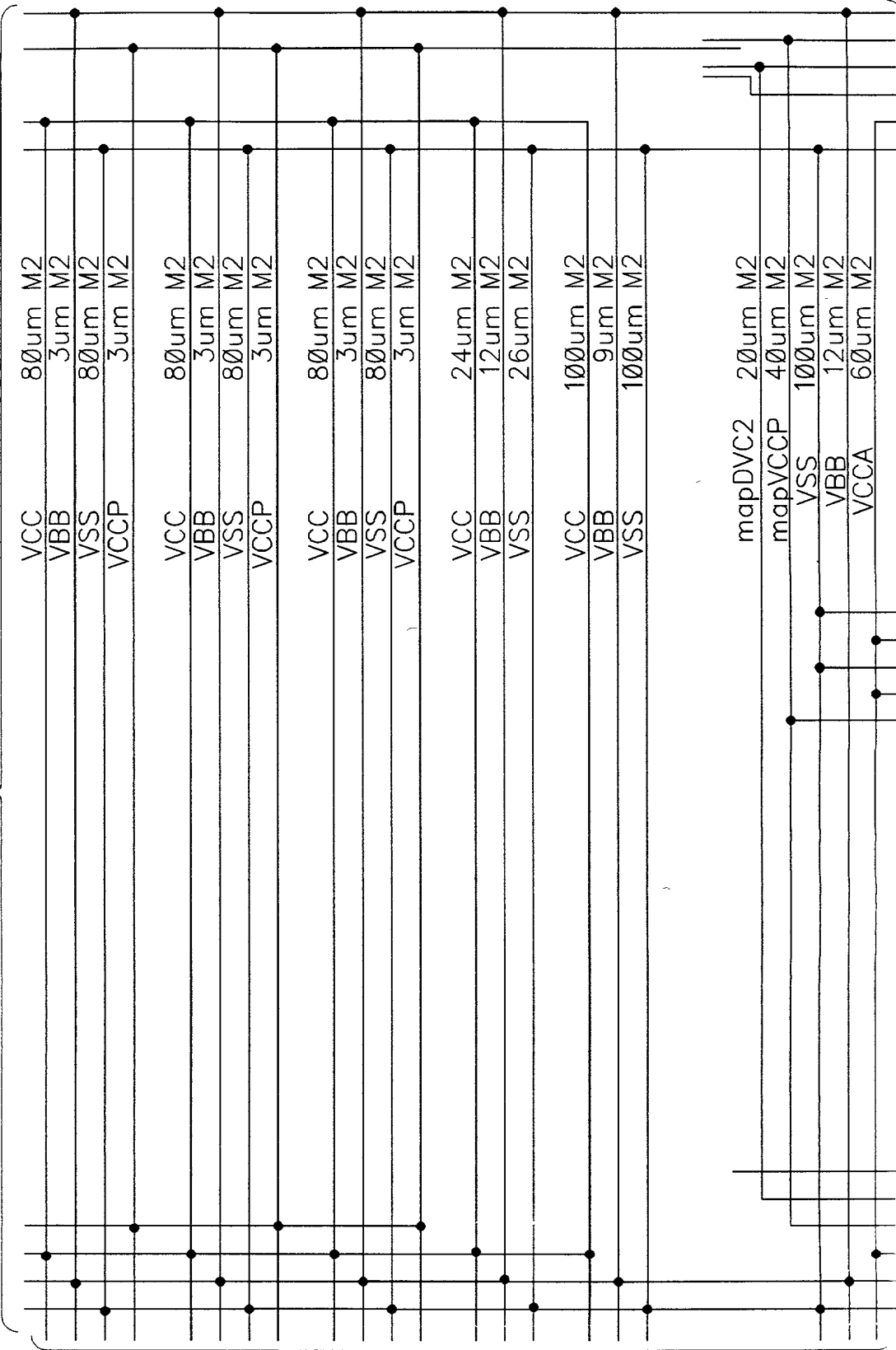




[illegible]

TO FIG. 33C3

FROM FIG. 33C2



FROM
FIG.
33B6

TO FIG. 33C4

FIG. 33C3

FROM FIG. 33C3

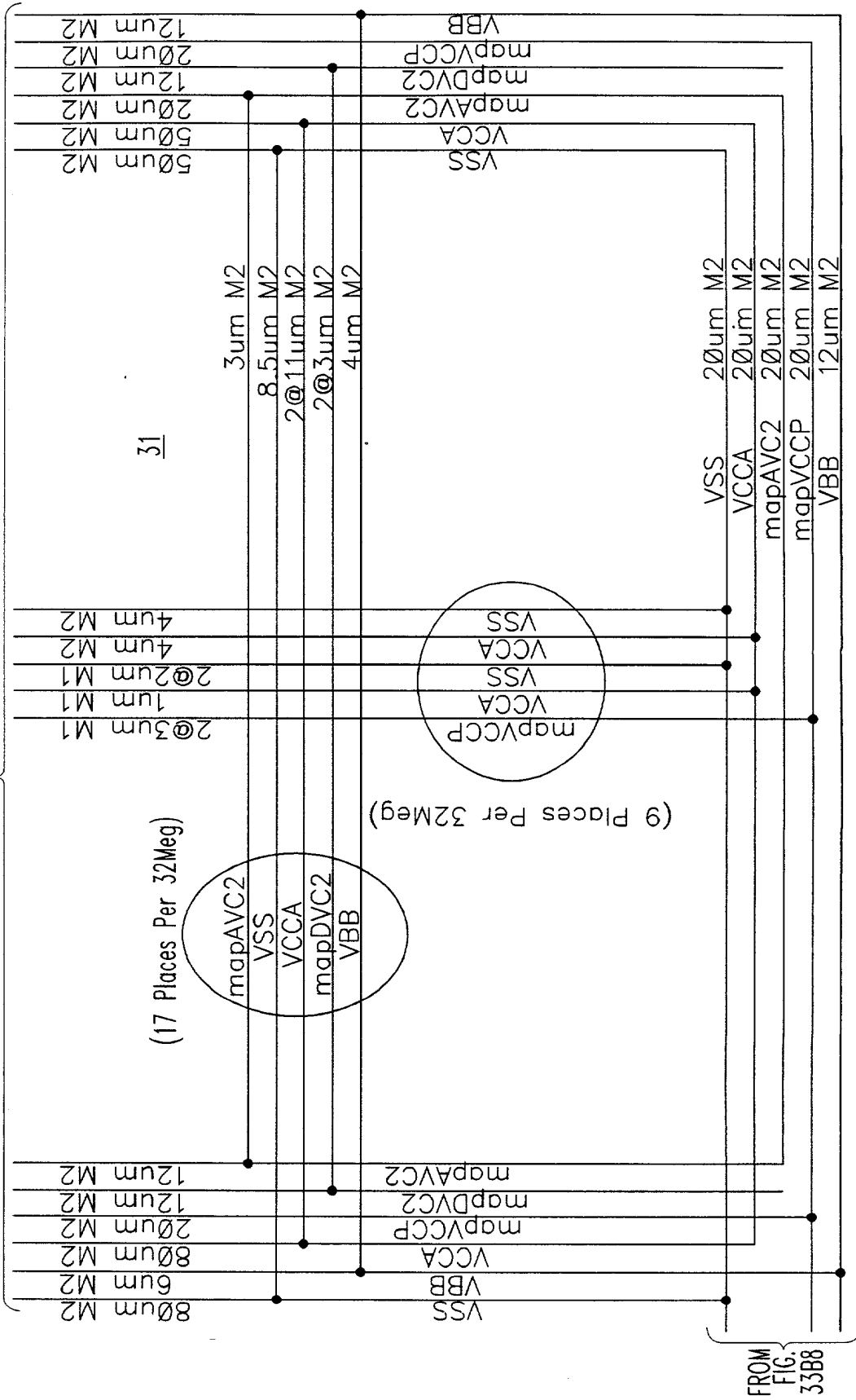


FIG. 33C4

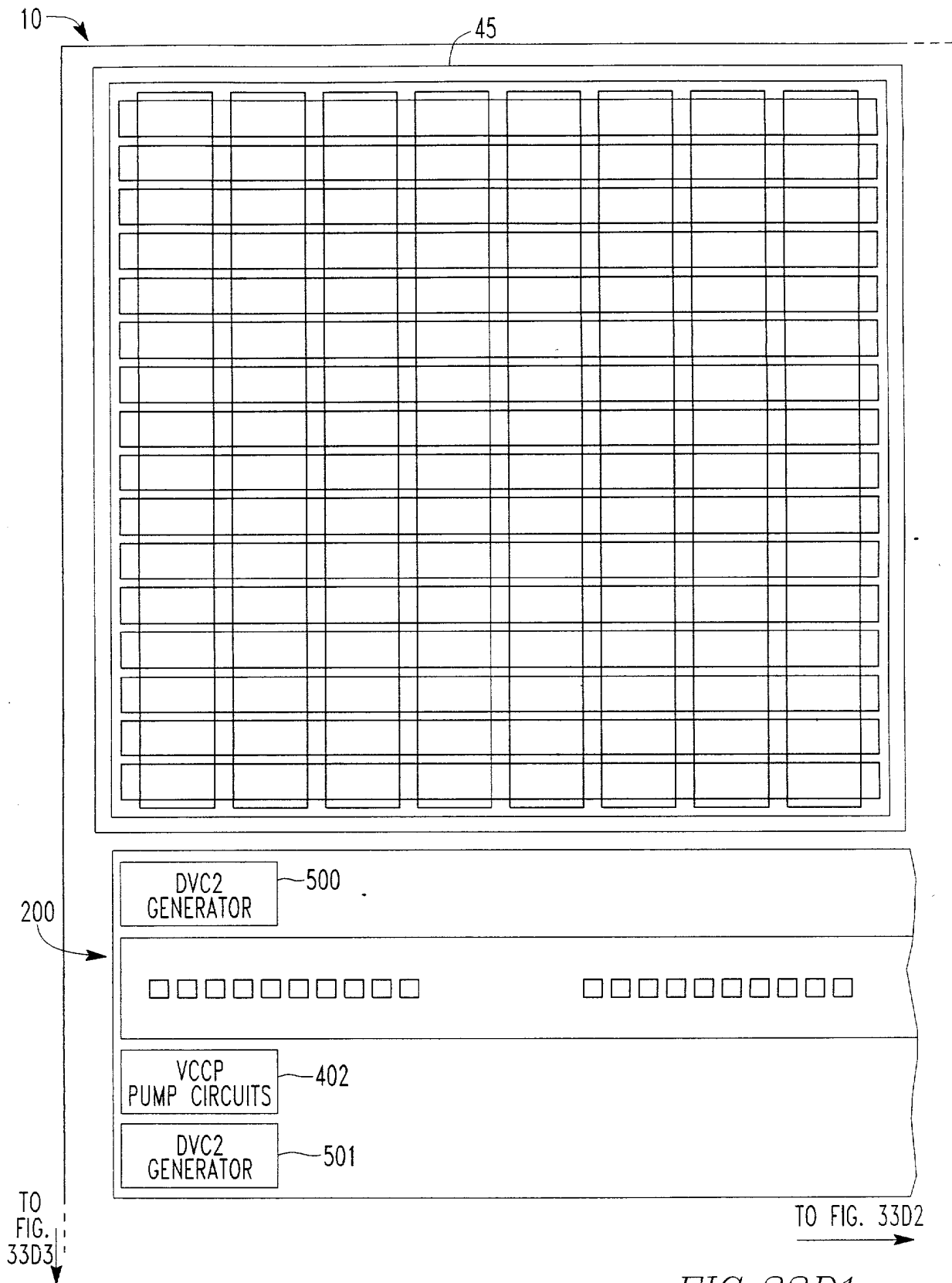


FIG. 33D1

TO FIG. 33D1

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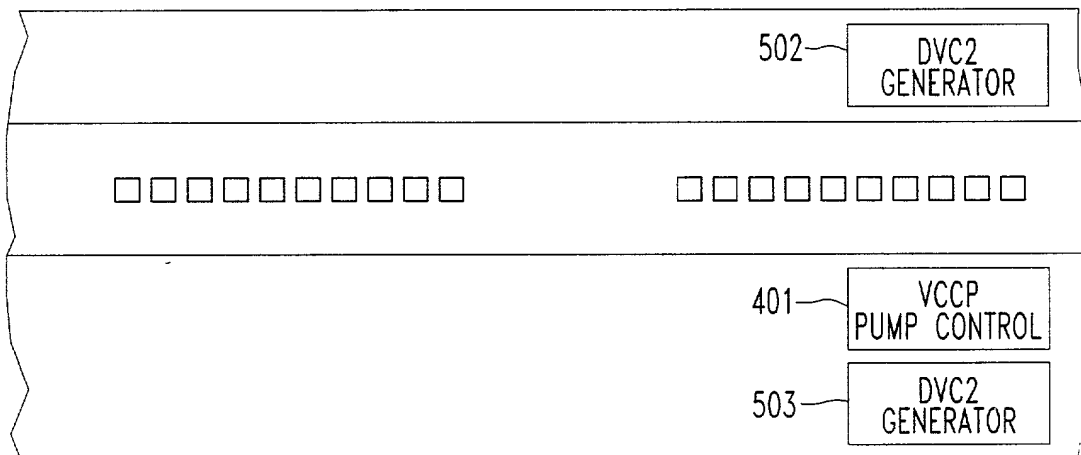
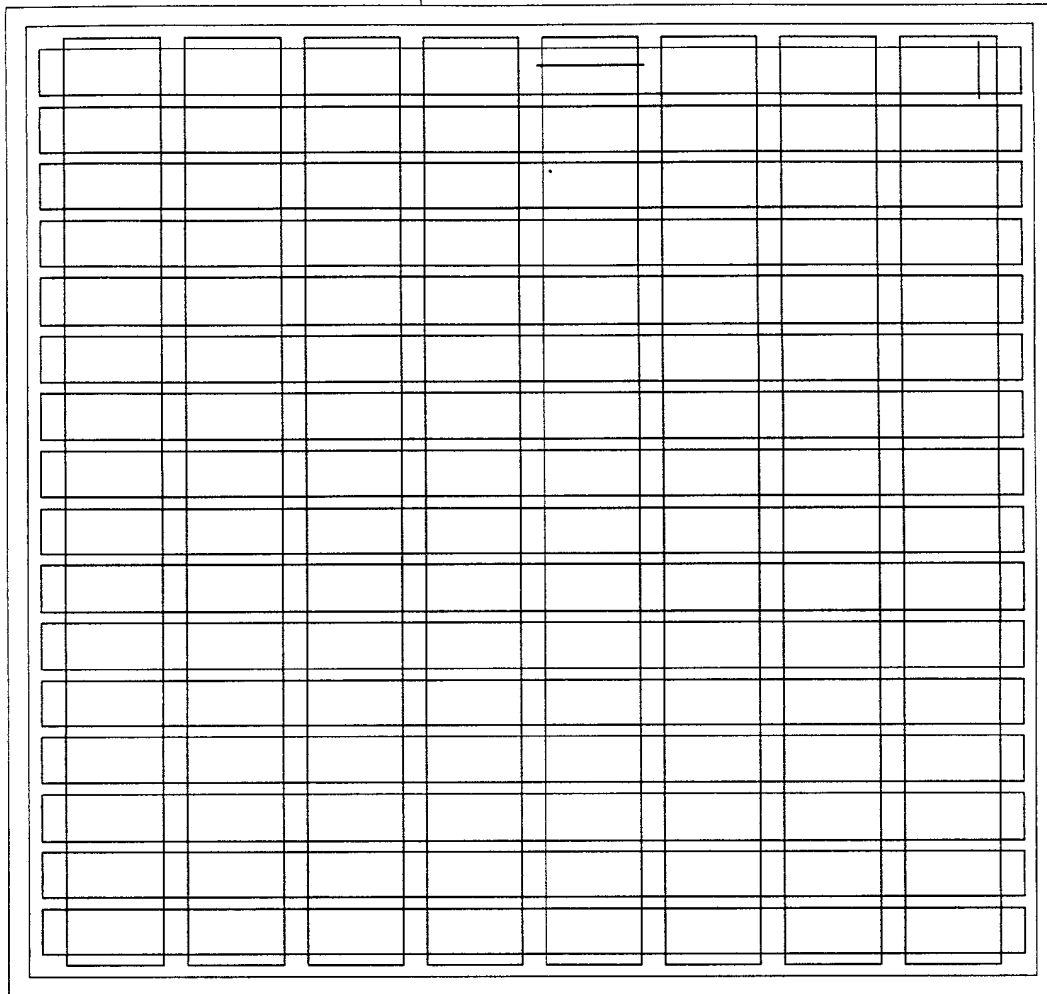


FIG. 33D2

TO
FIG.
33D4

TO
FIG. 33D1

(SEE FIG. 33E1)

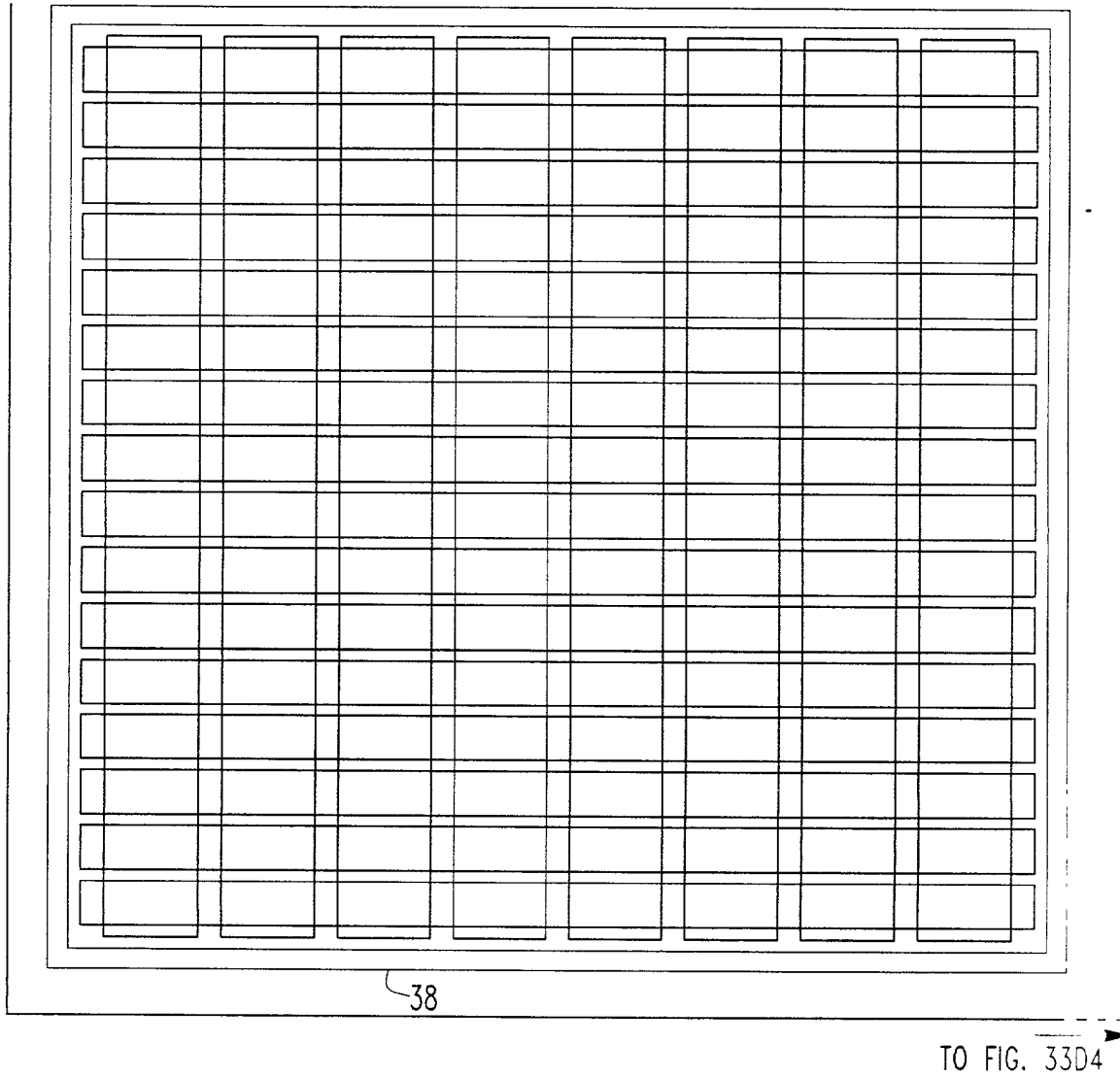
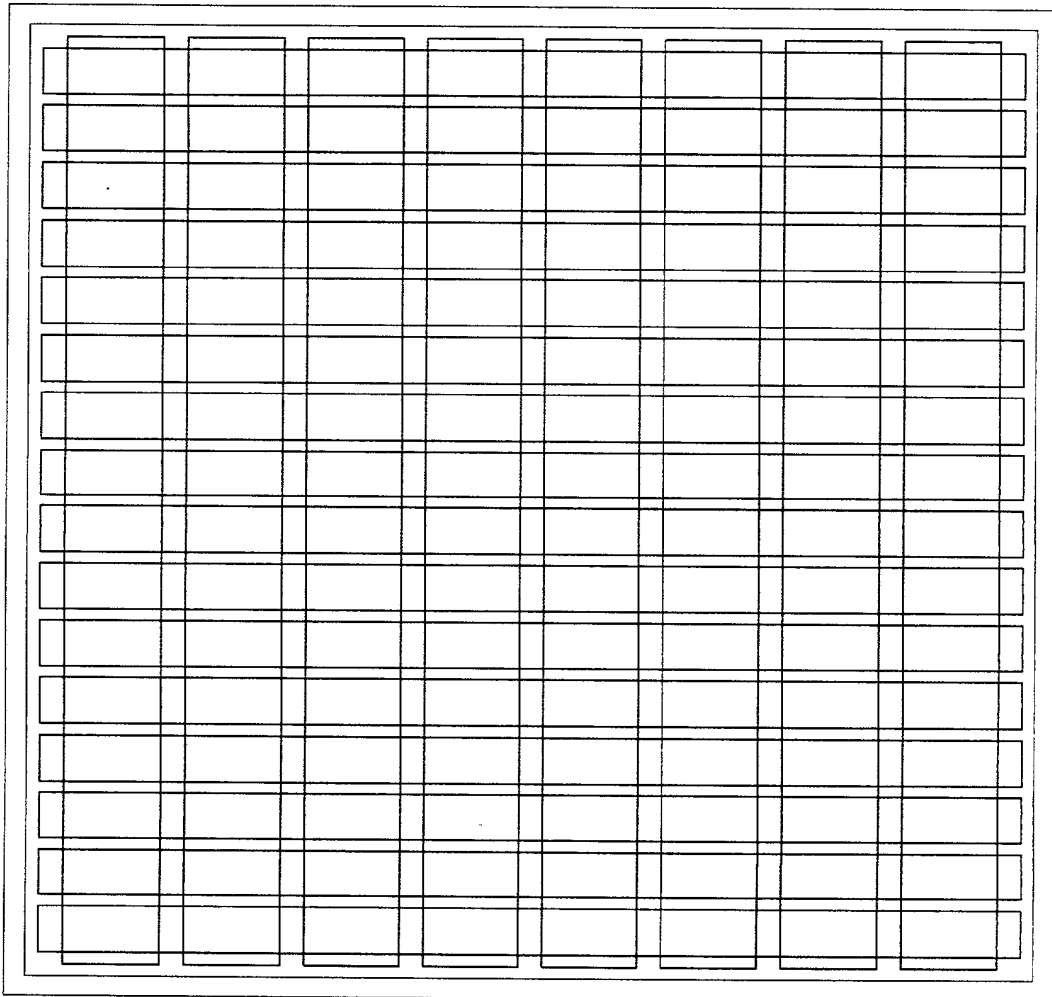


FIG. 33D3

TO
FIG.
33D2



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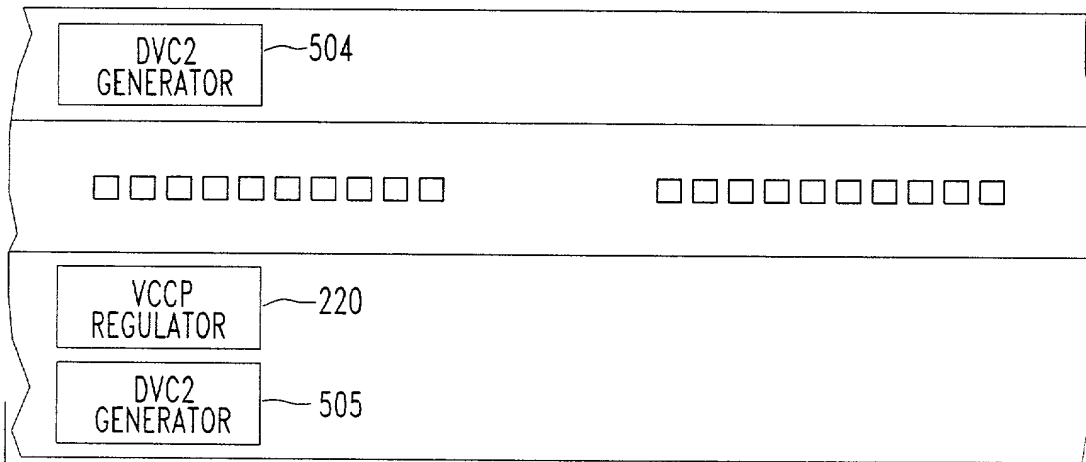
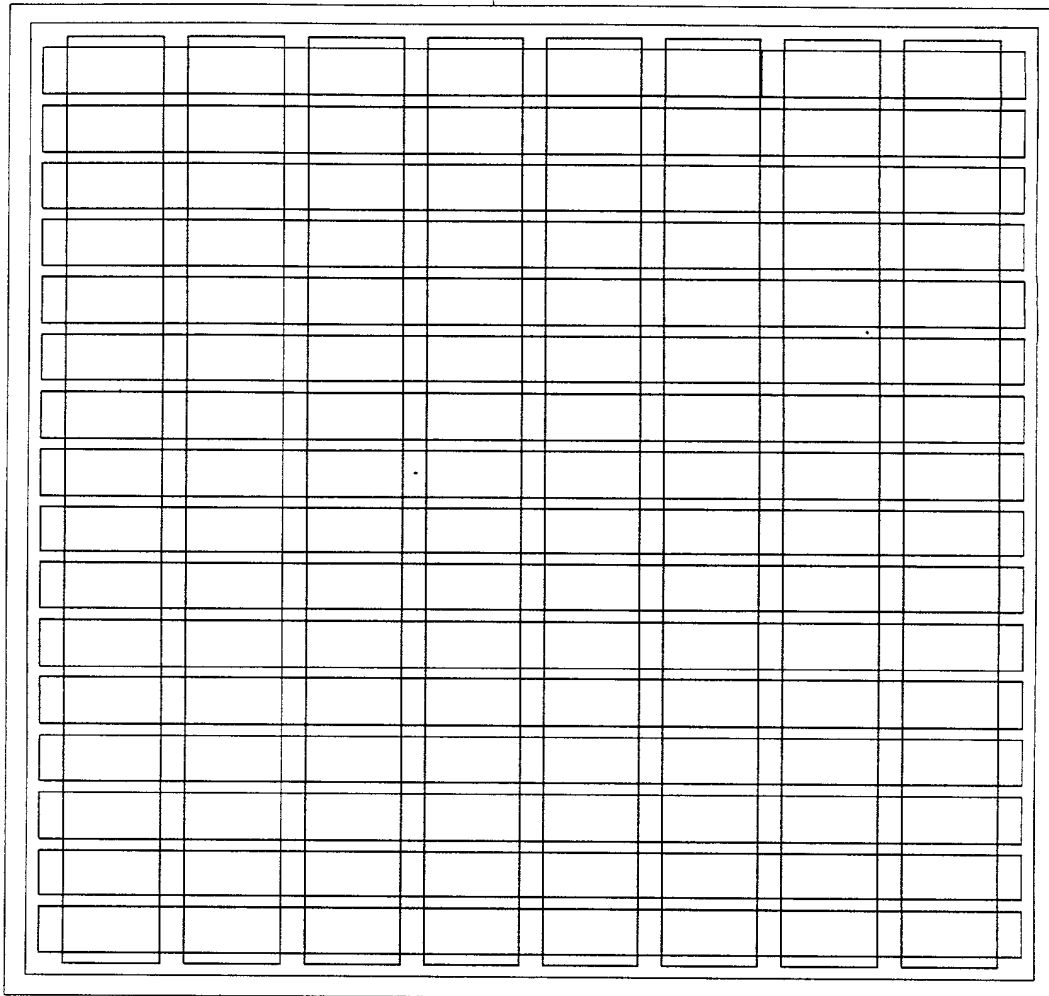
TO FIG. 33D3

FIG. 33D4

(SEE FIG. 33D2)

25

TO FIG. 33E2



TO
FIG.
33E3

FIG. 33E1

TO FIG. 33E1

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27

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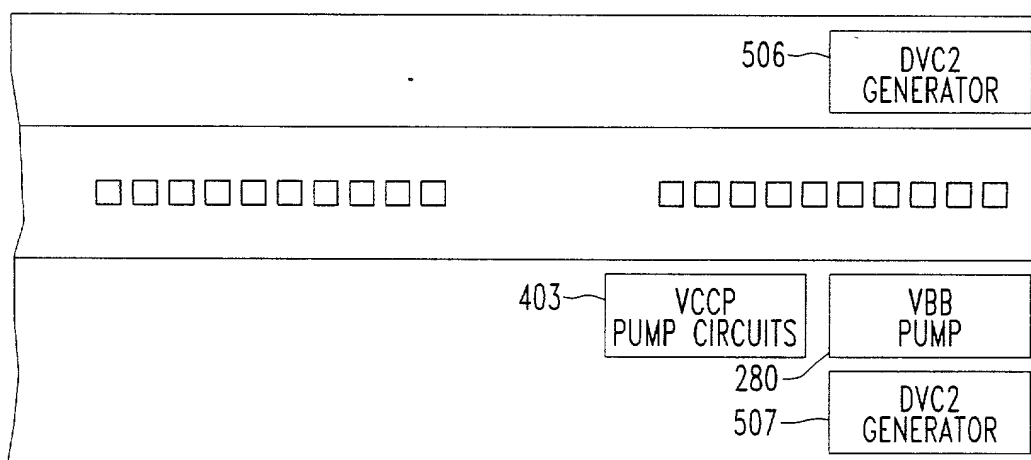
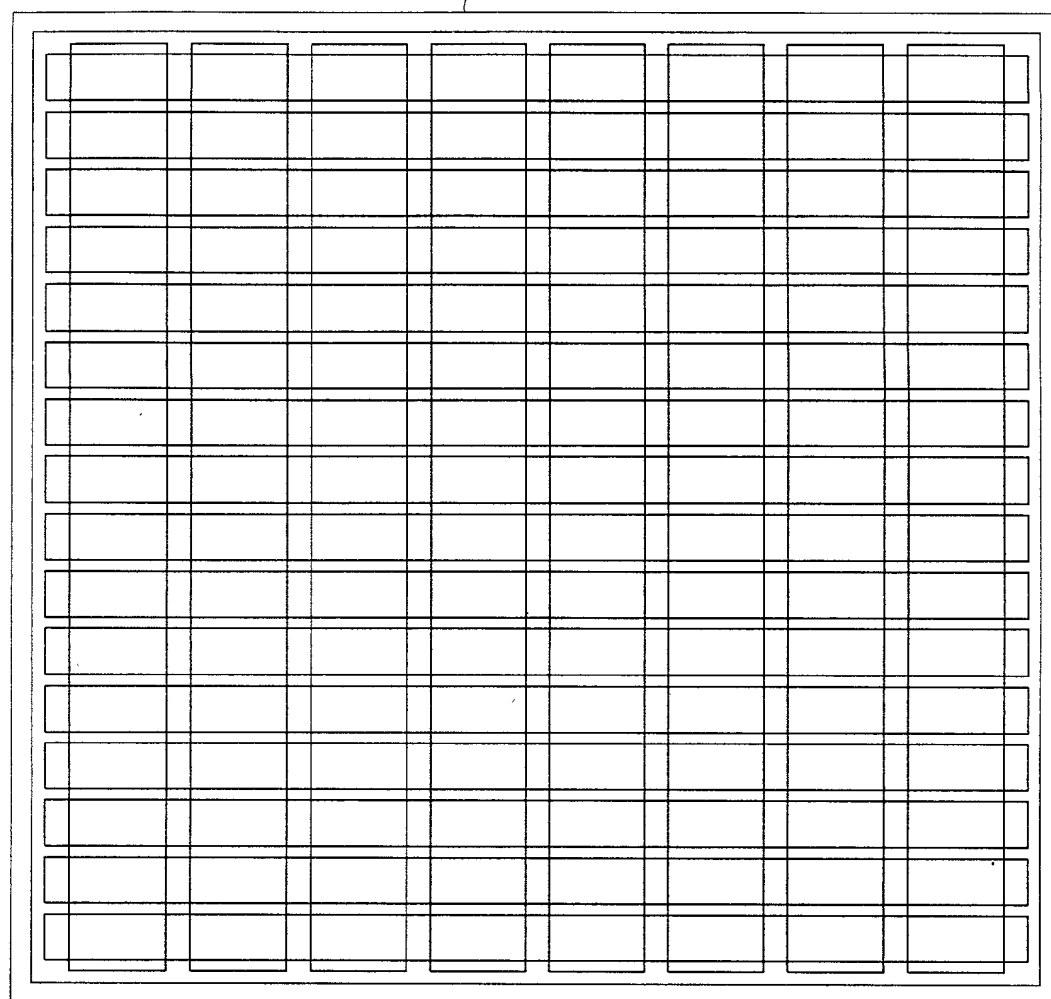
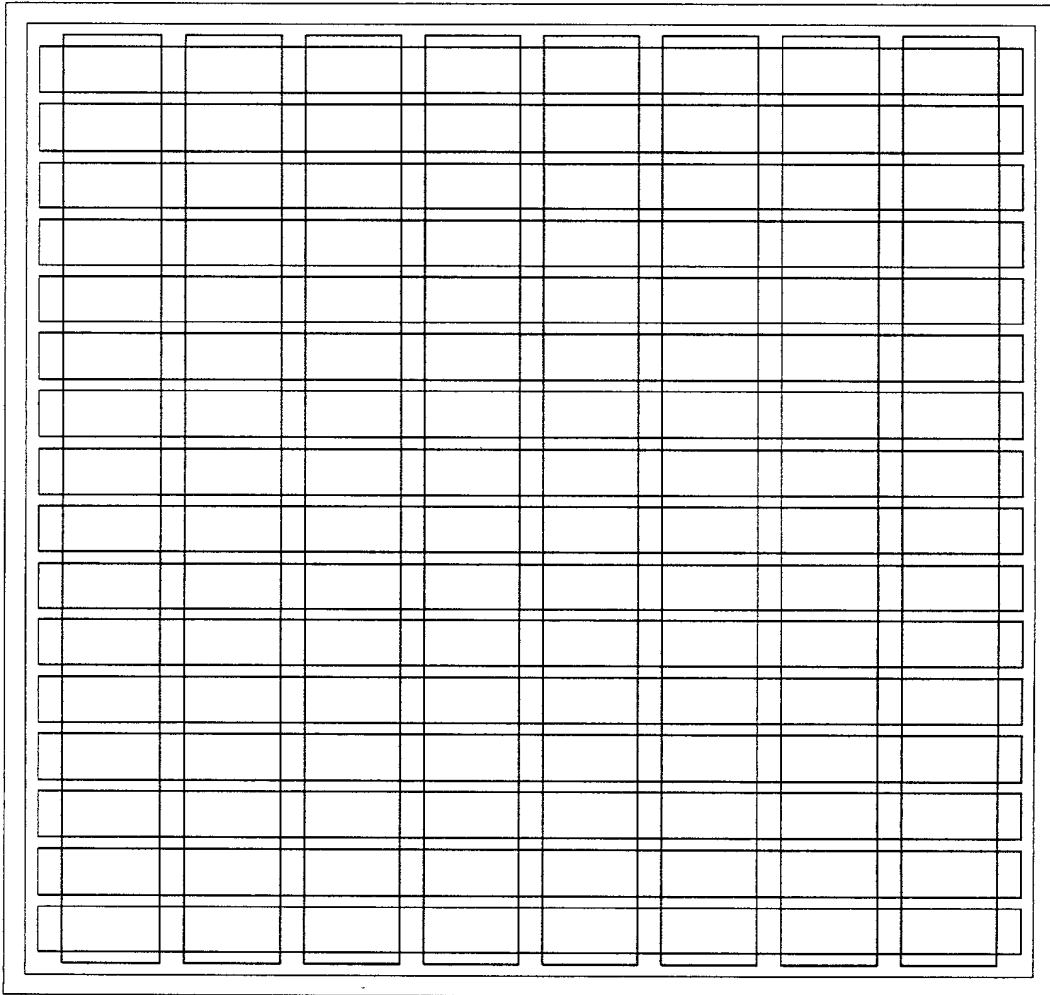


FIG. 33E2

TO
FIG.
33E4

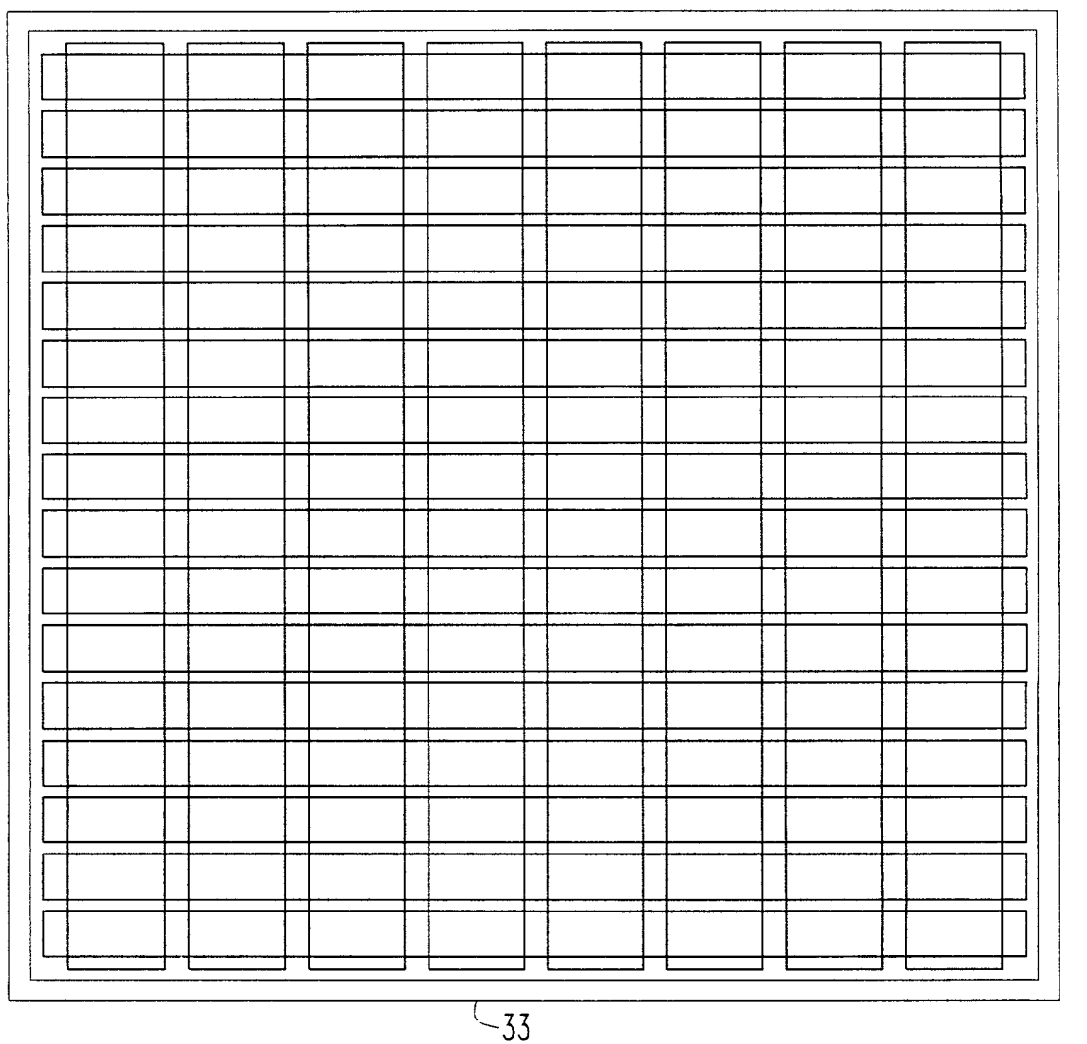
TO
FIG.
33E1



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FIG. 33E3

TO FIG. 33E4



TO FIG. 33E3

FIG. 33E4

TO
FIG.
33E2

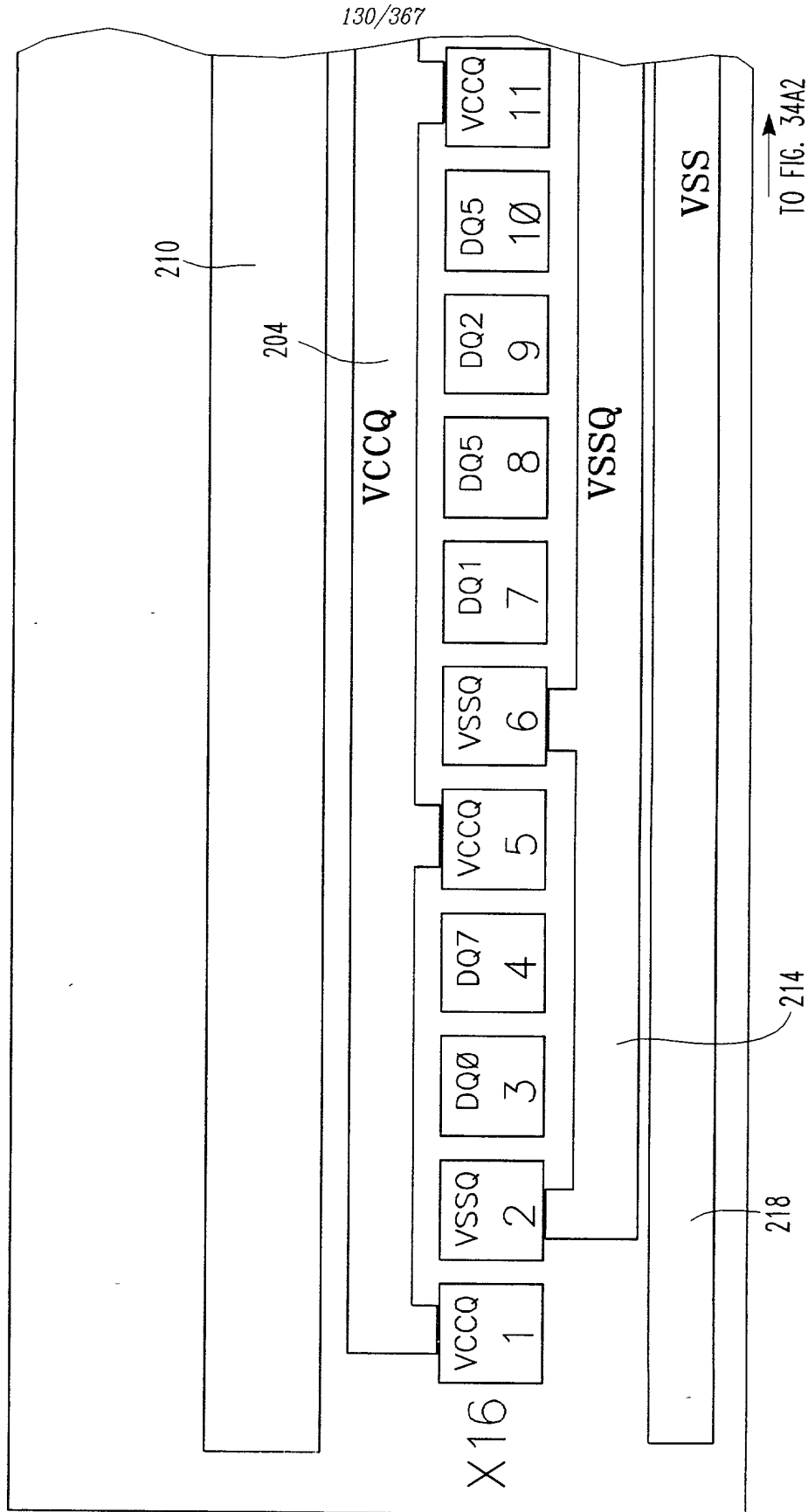
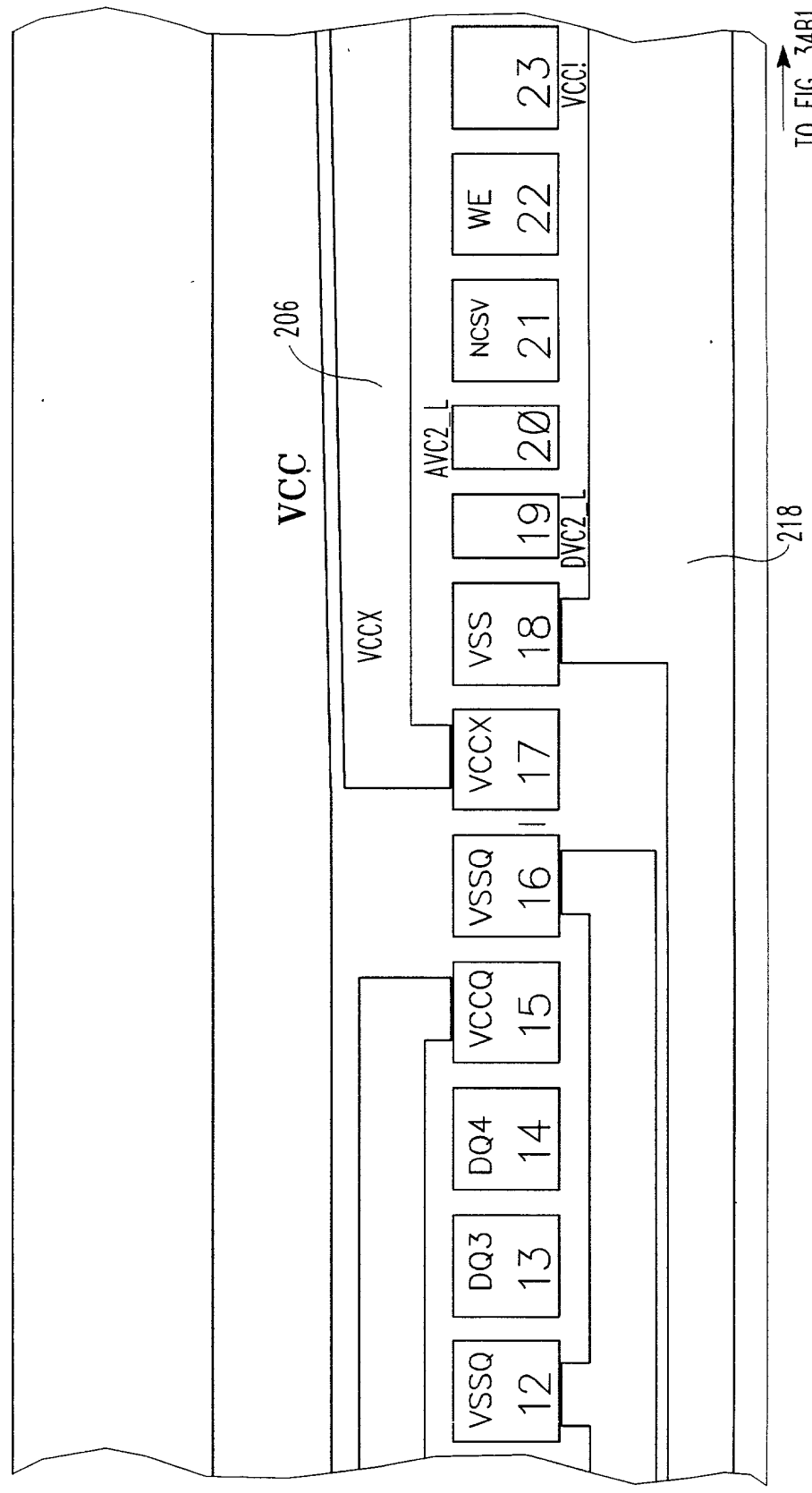


FIG. 34A1

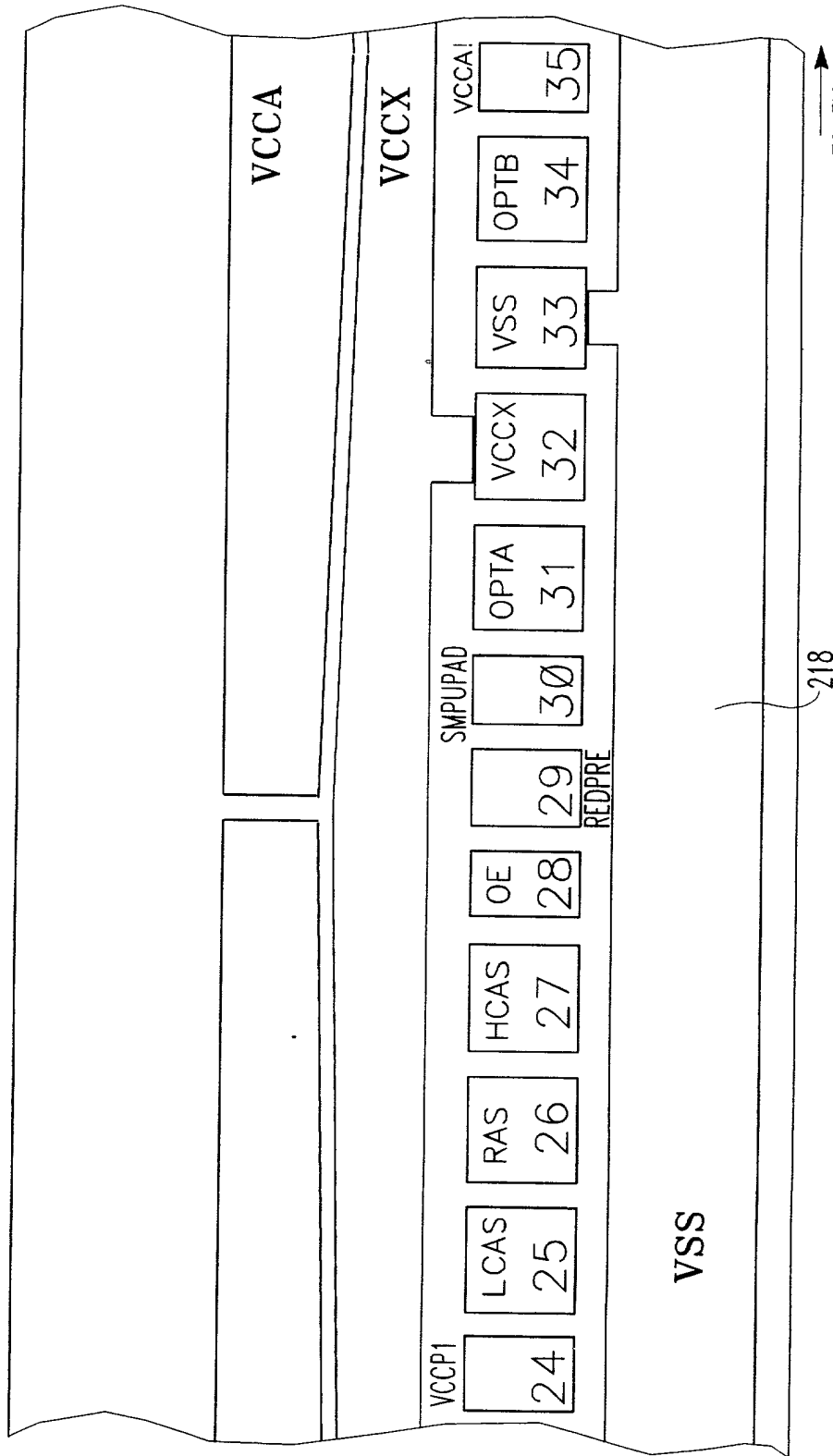
TO FIG. 34A1
←



TO FIG. 34B1
→

FIG. 34A2

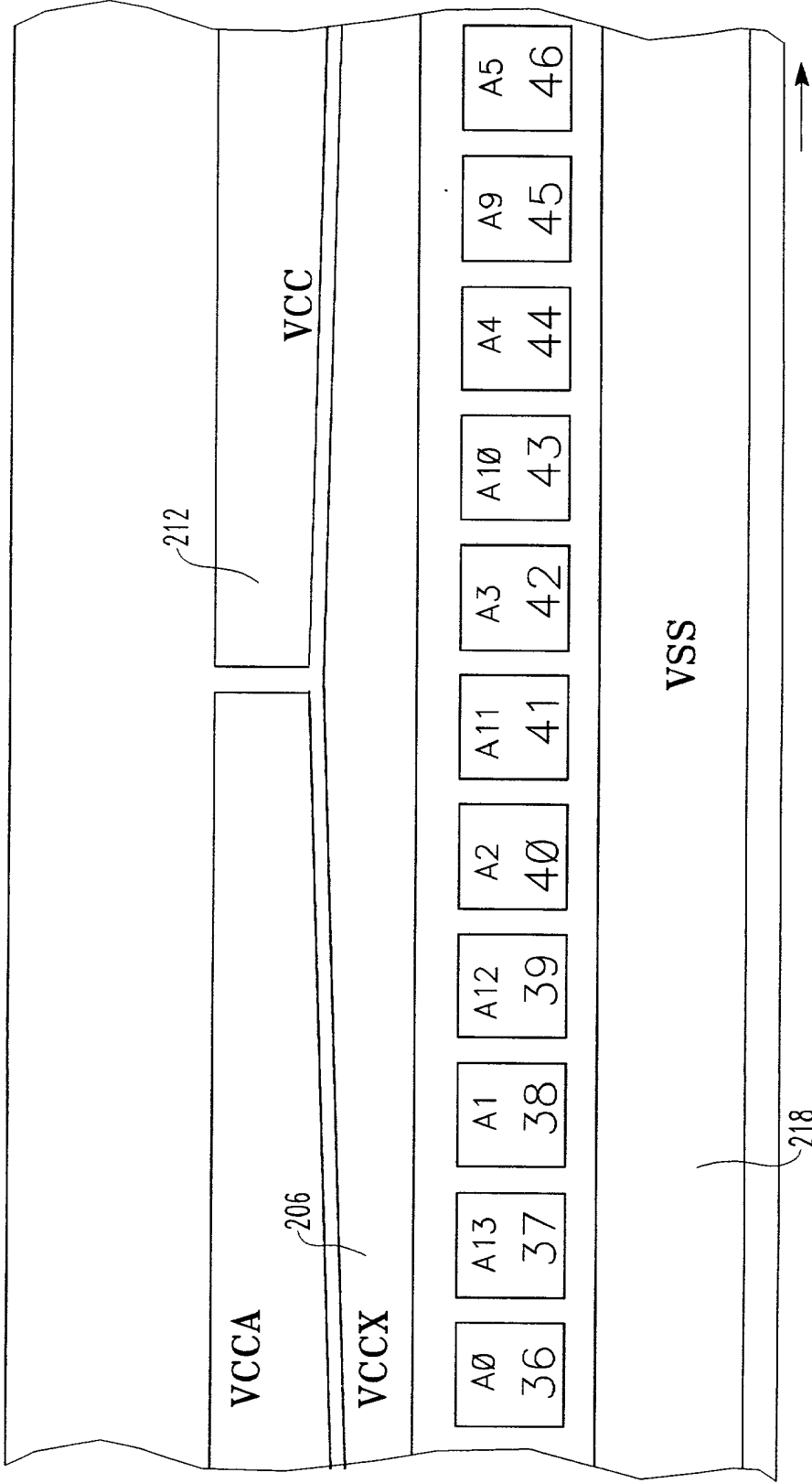
TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

TO FIG. 34B1



TO FIG. 34C1

FIG. 34B2

TO FIG. 34B2

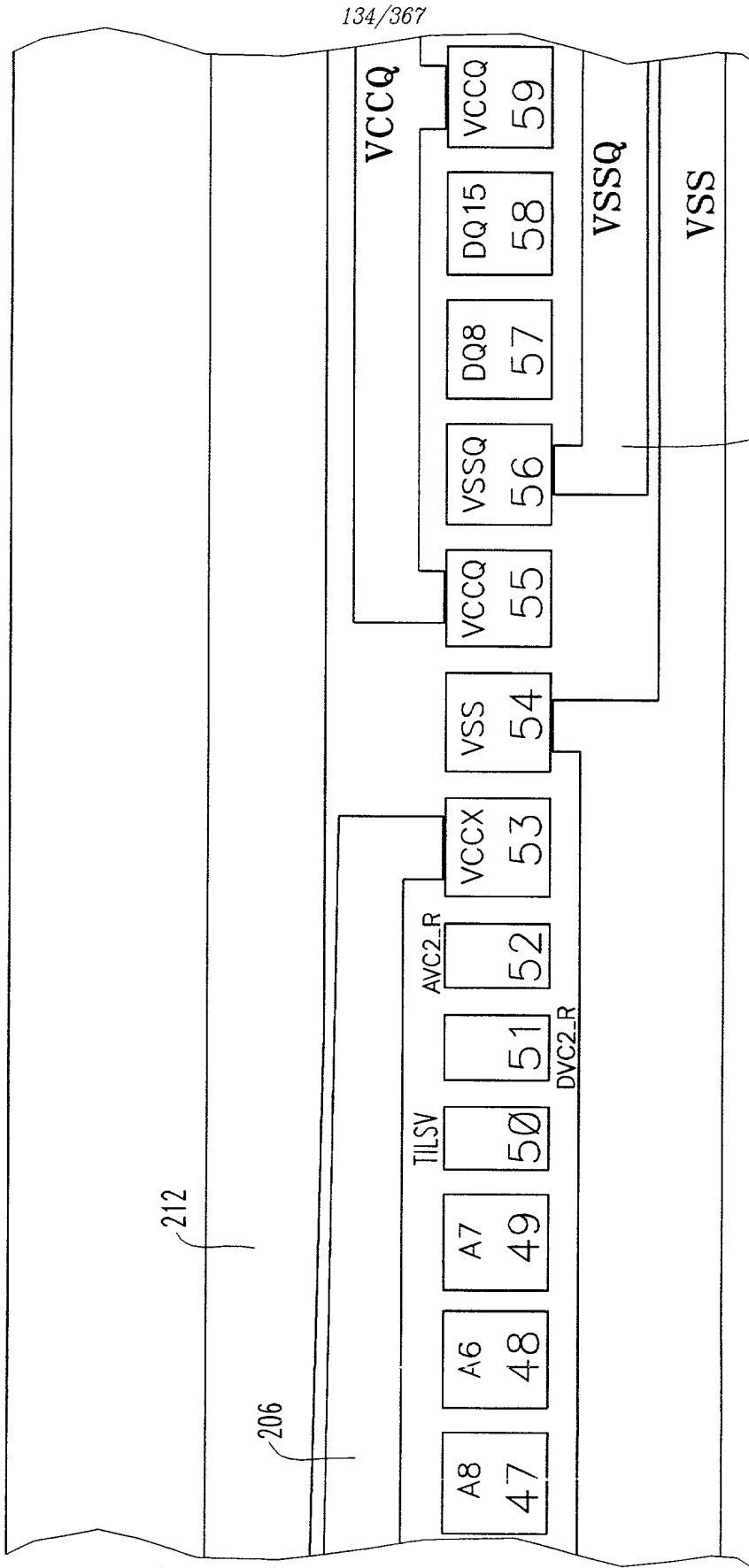


FIG. 34C1

TO FIG. 34C1

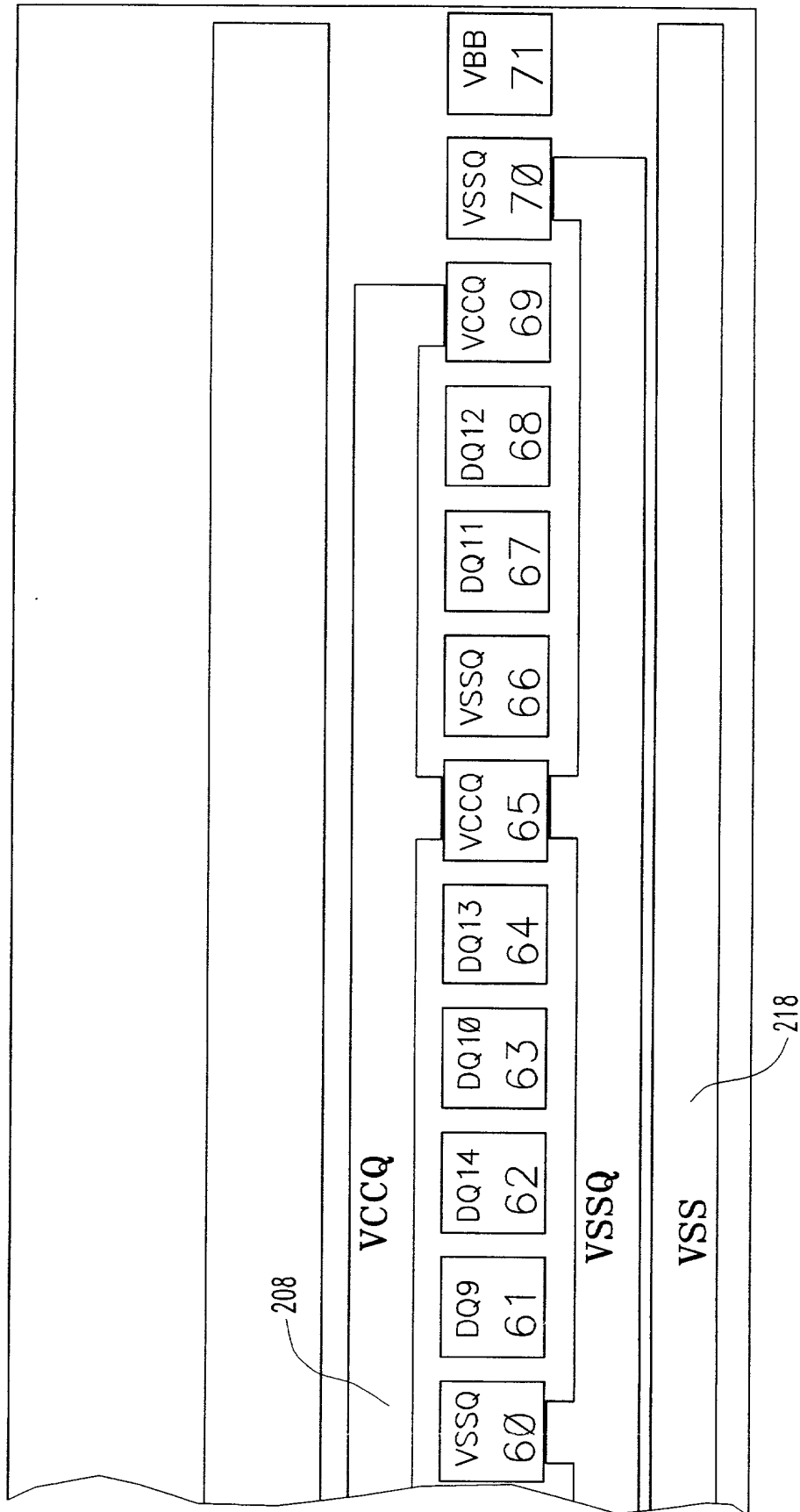


FIG. 34C2

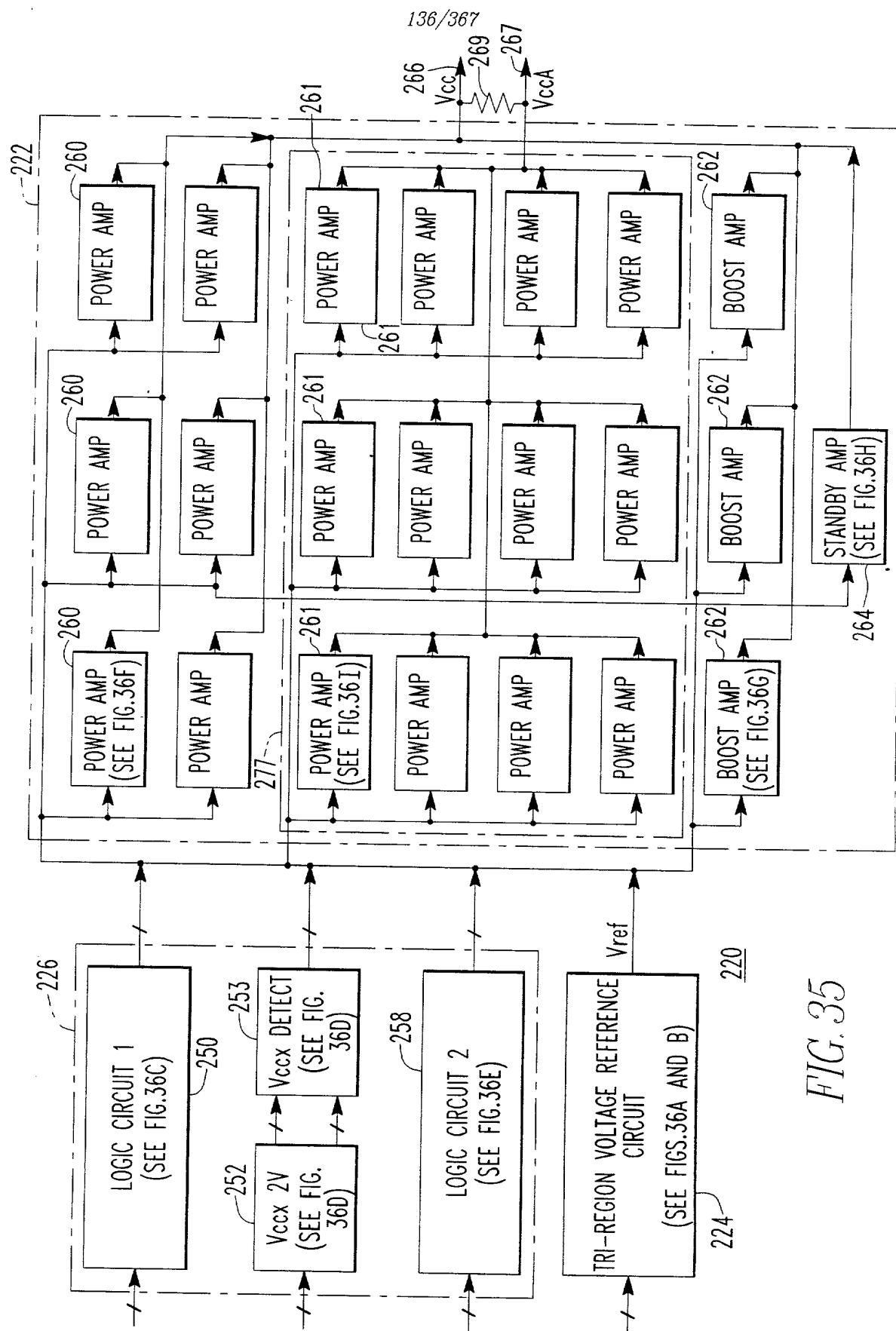


FIG. 35

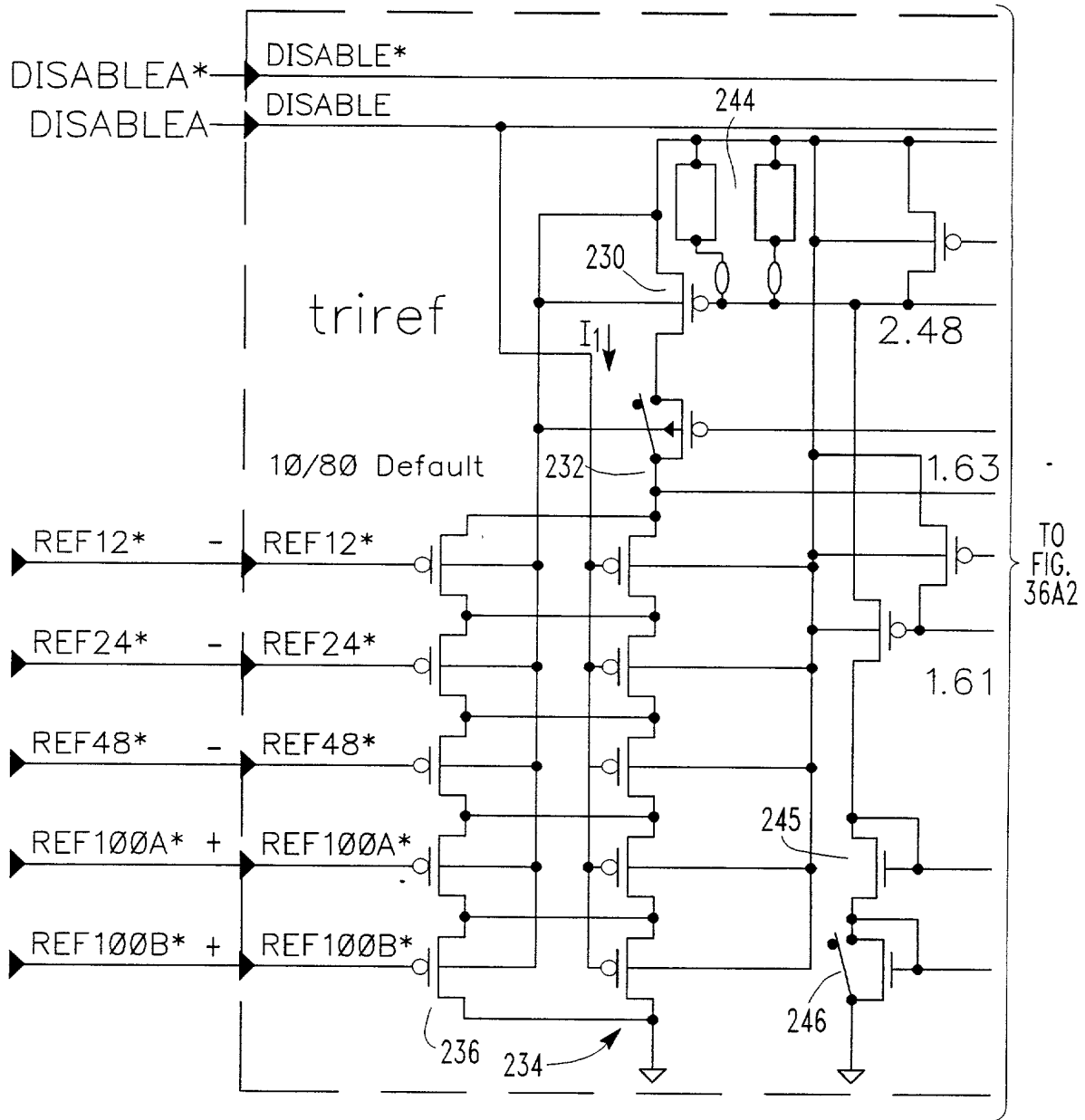


FIG. 36A1

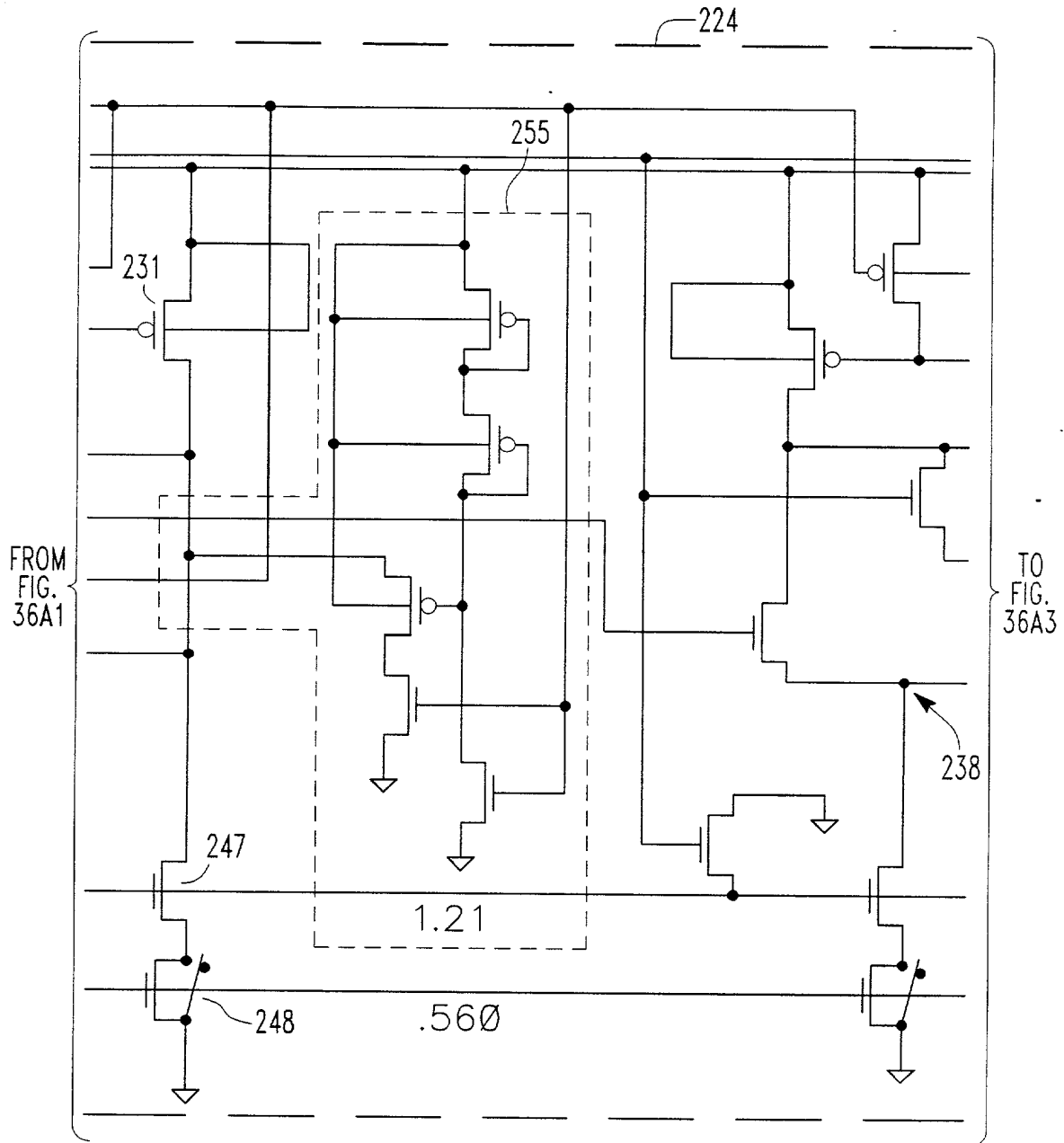
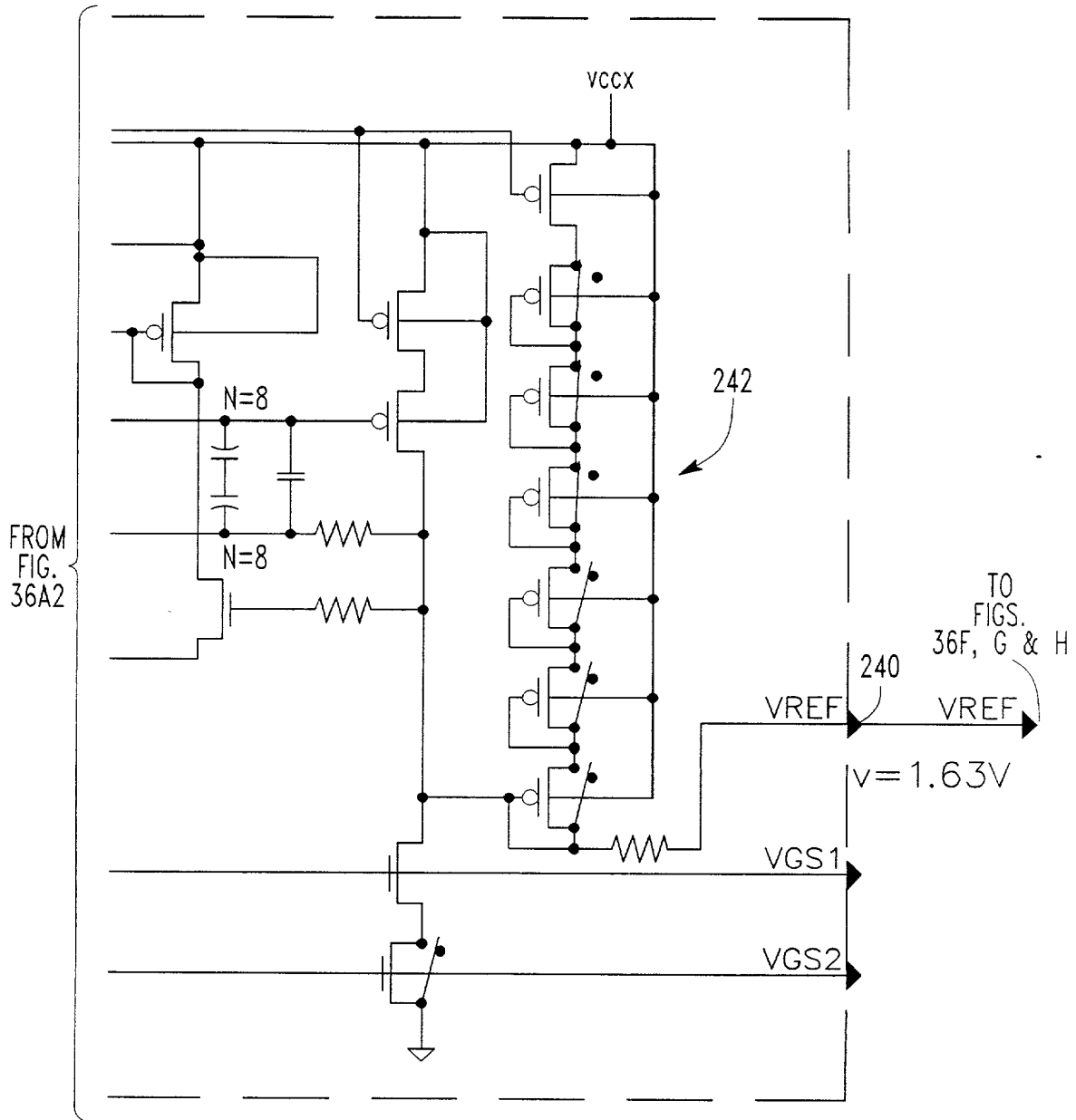


FIG. 36A2



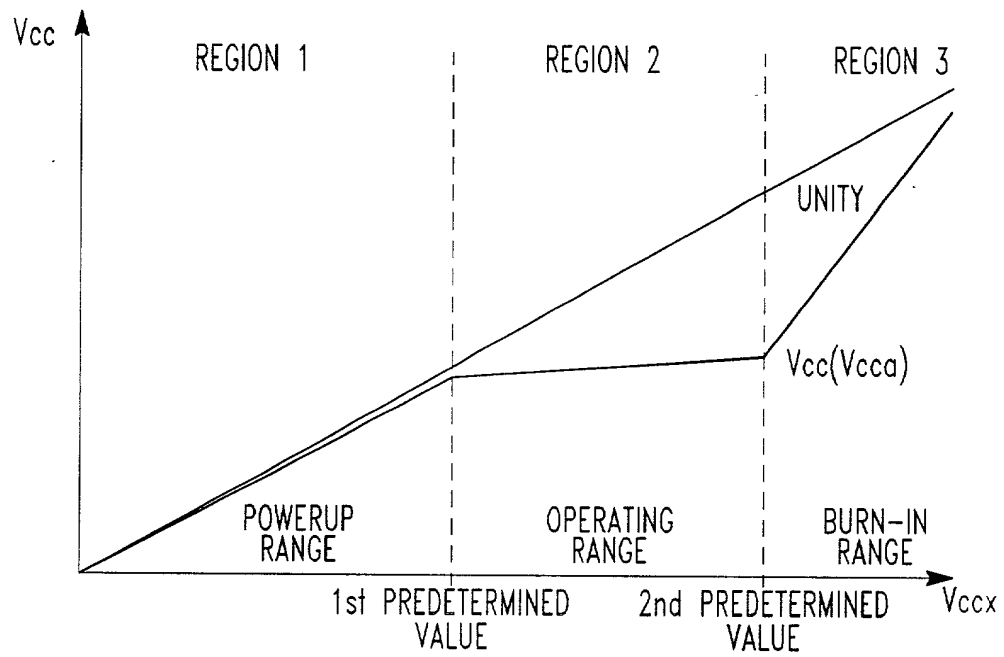


FIG. 36B

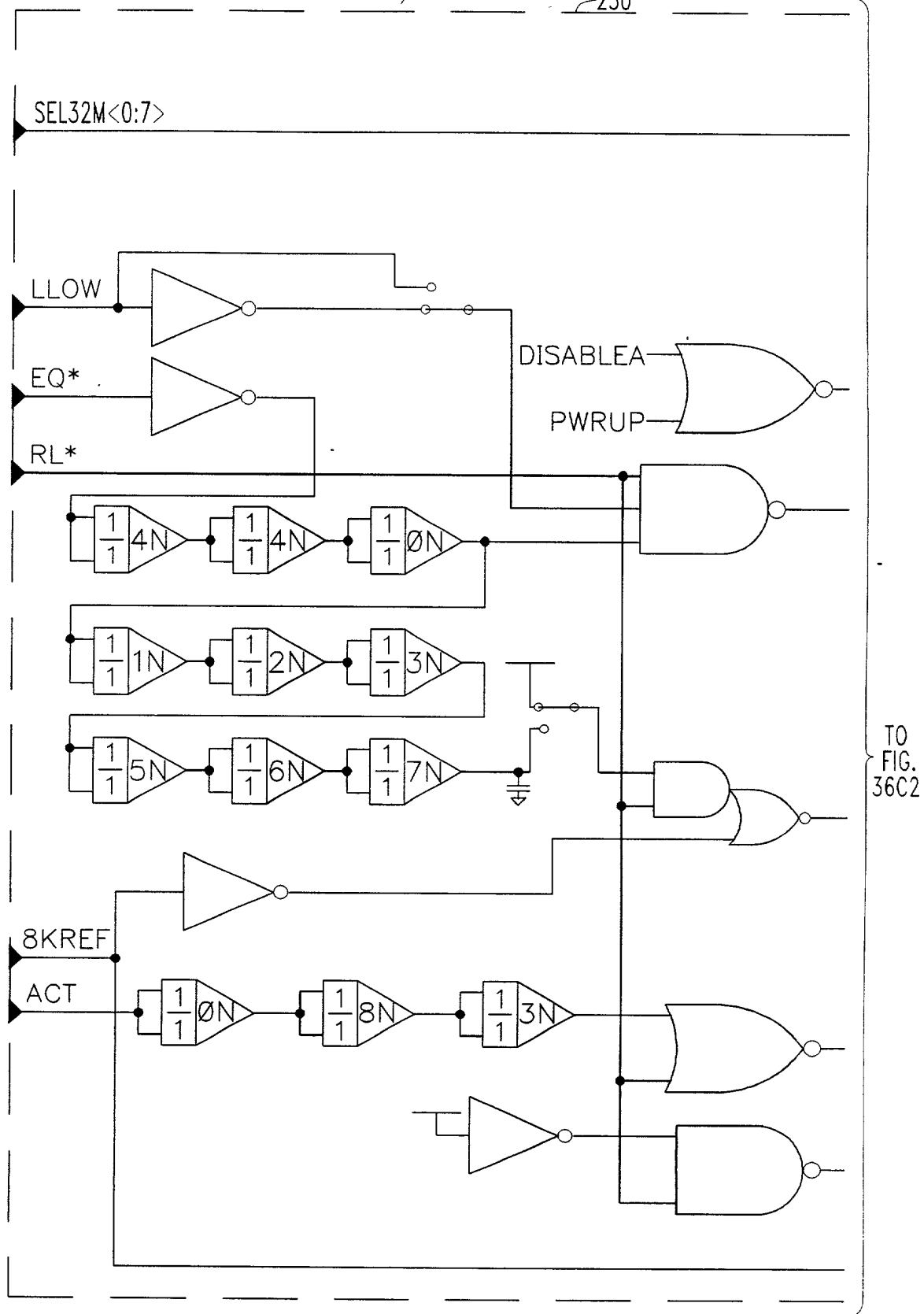


FIG. 36C1

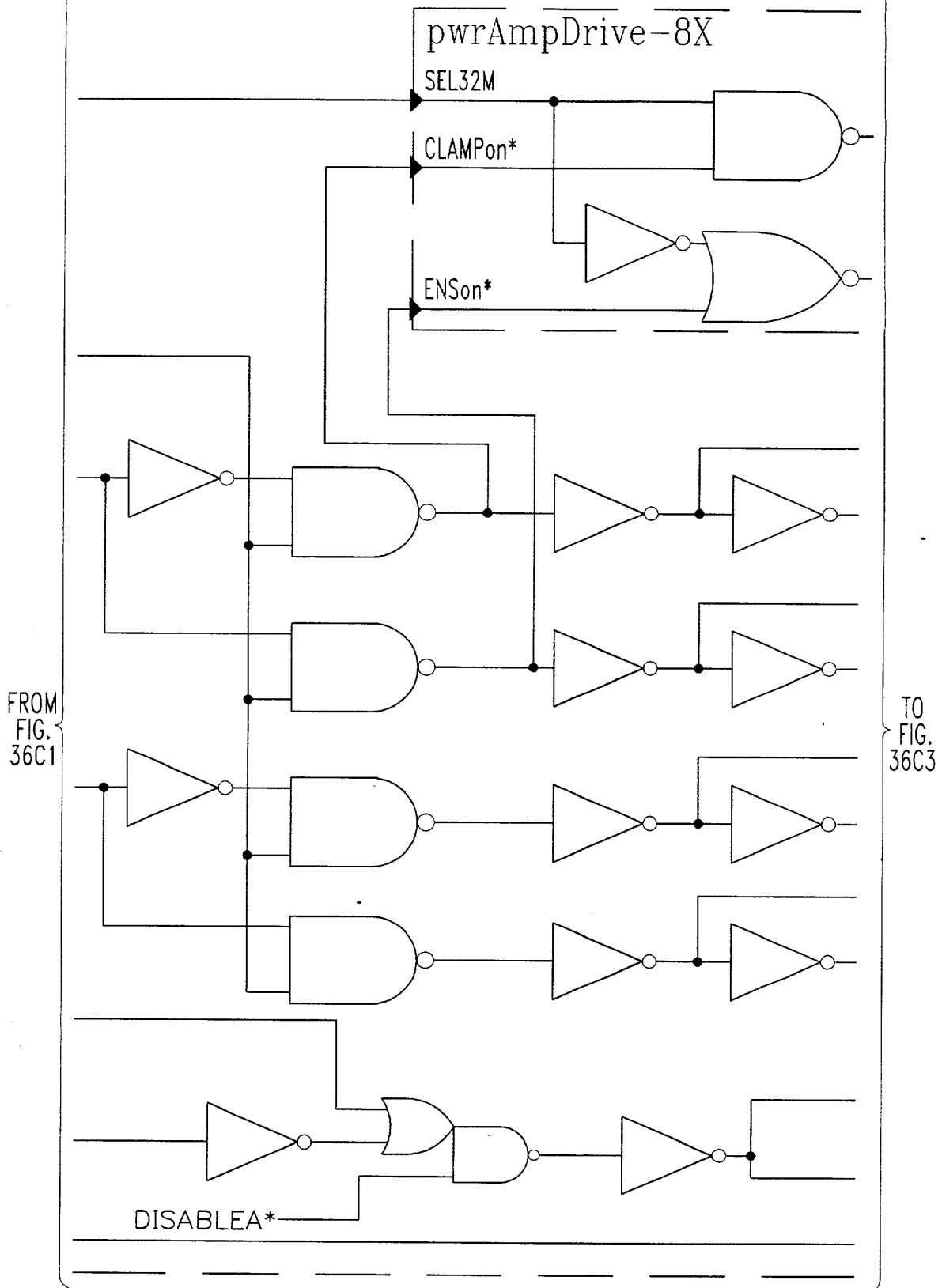


FIG. 36C2

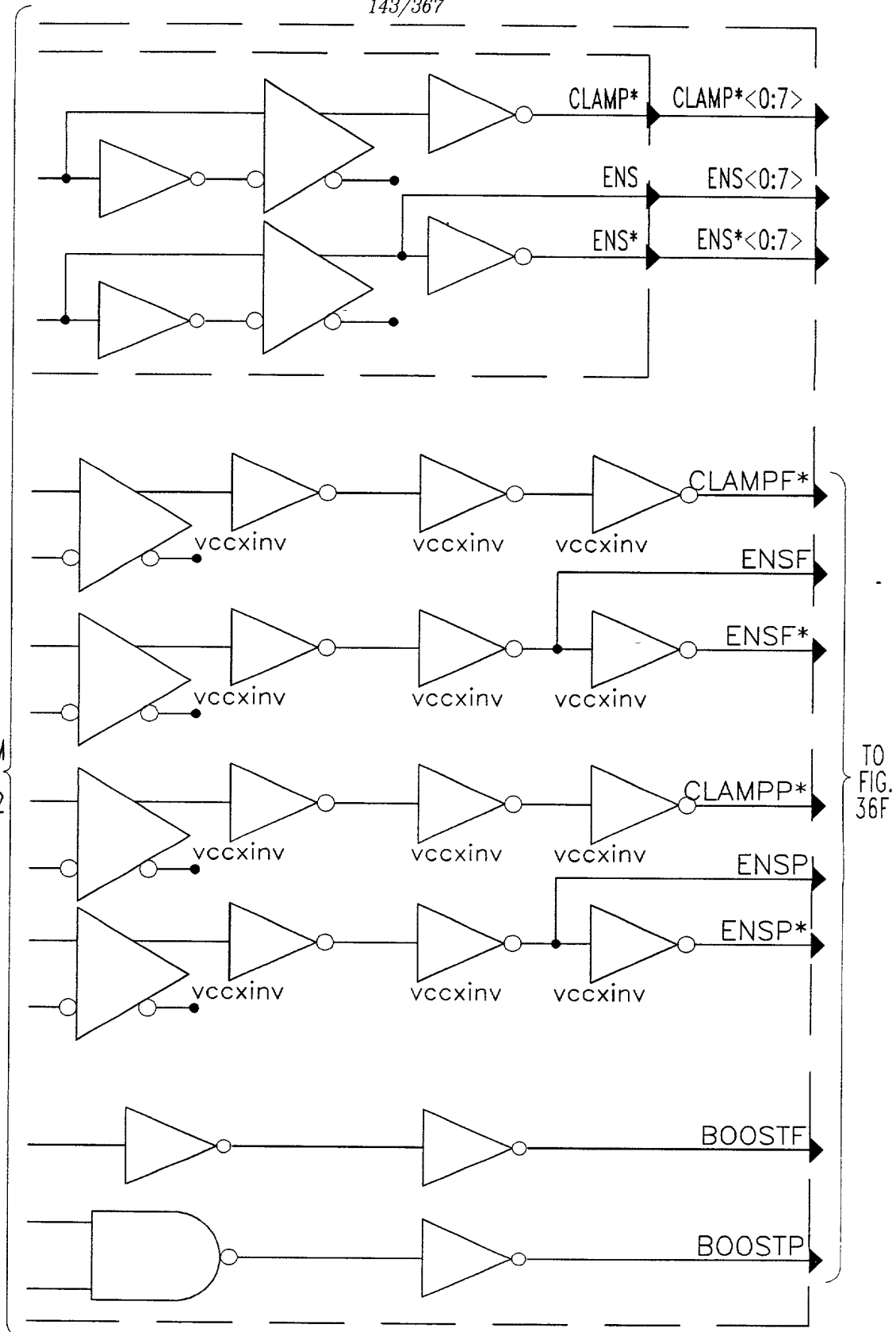


FIG. 36C3



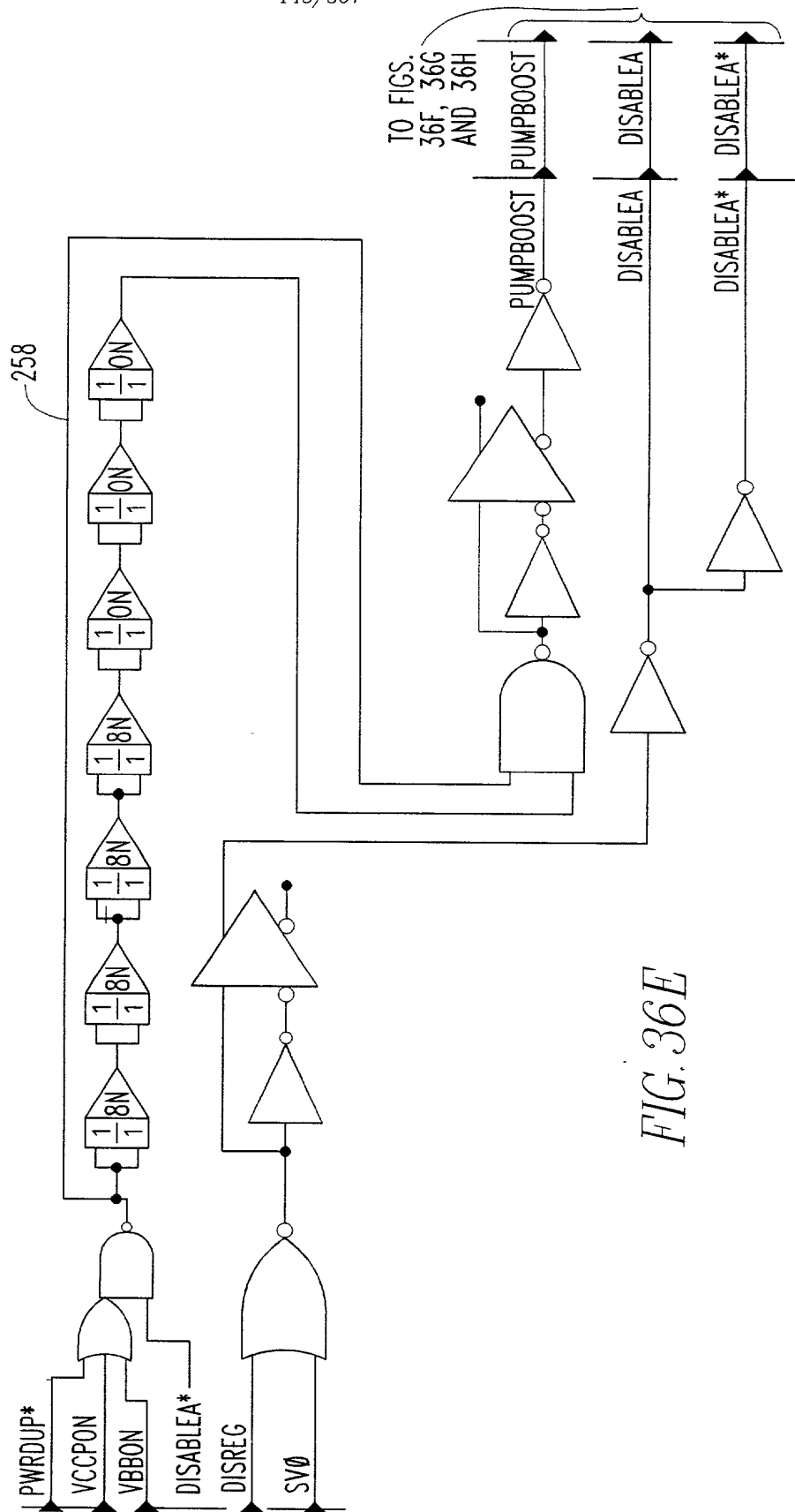


FIG. 36E

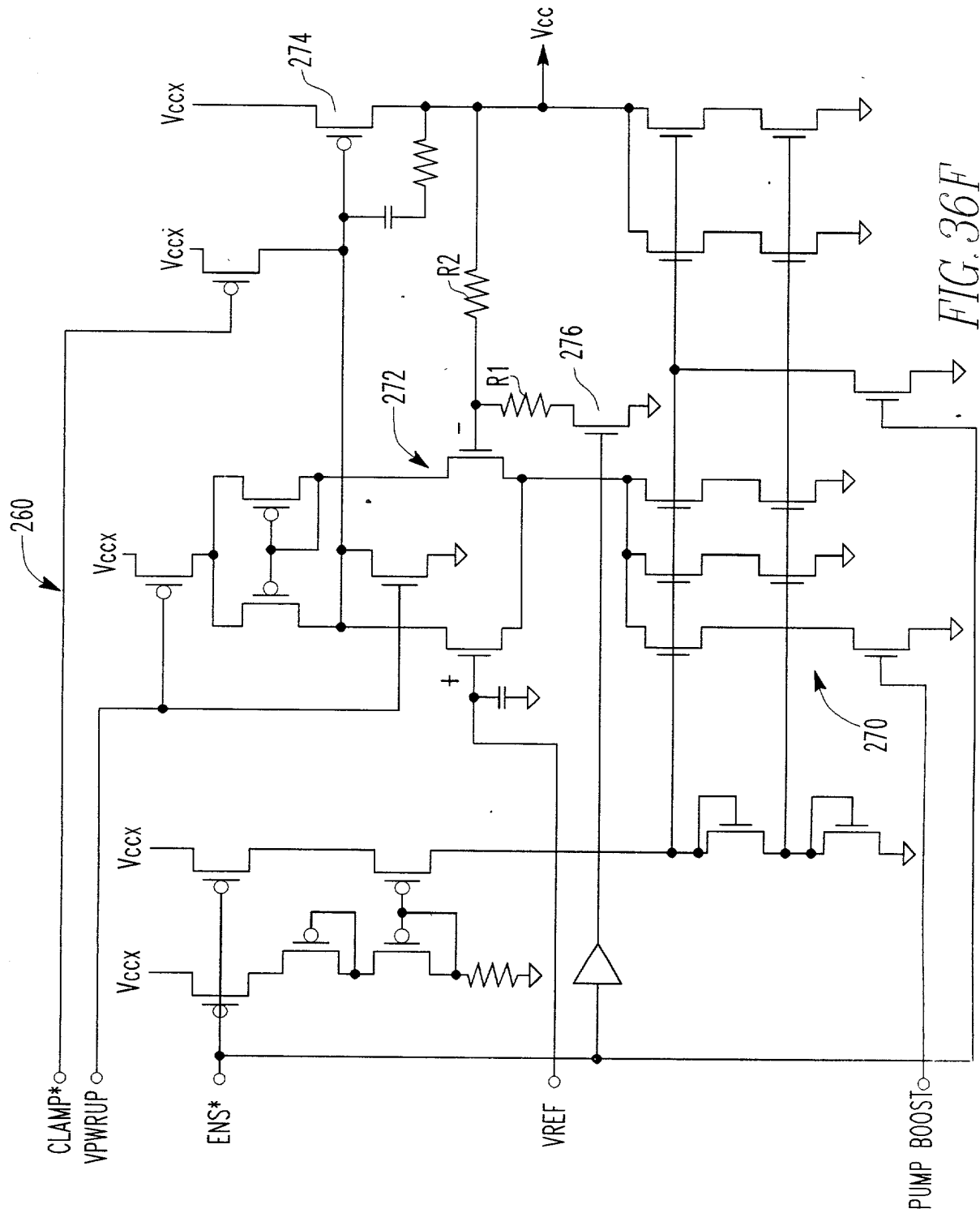
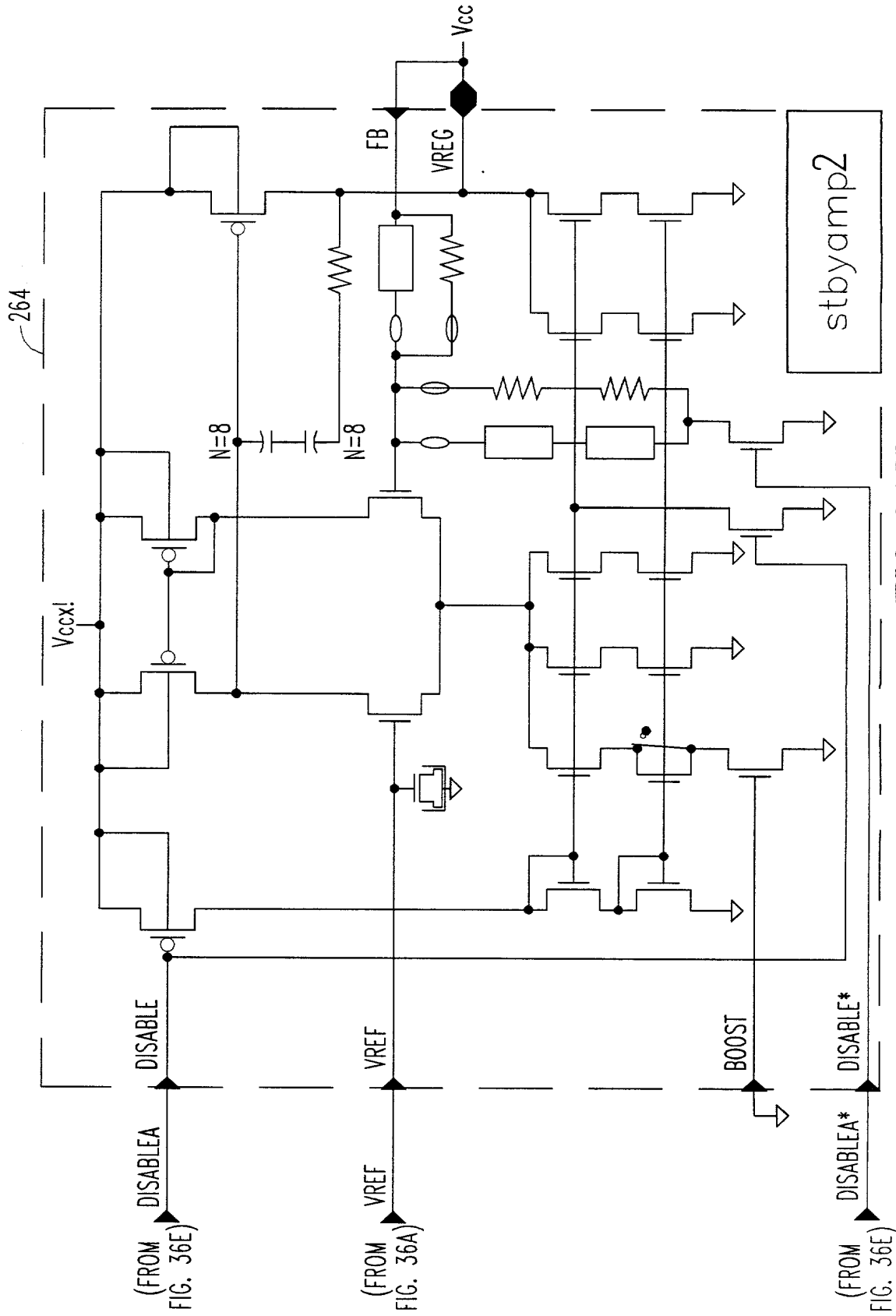


FIG. 36F





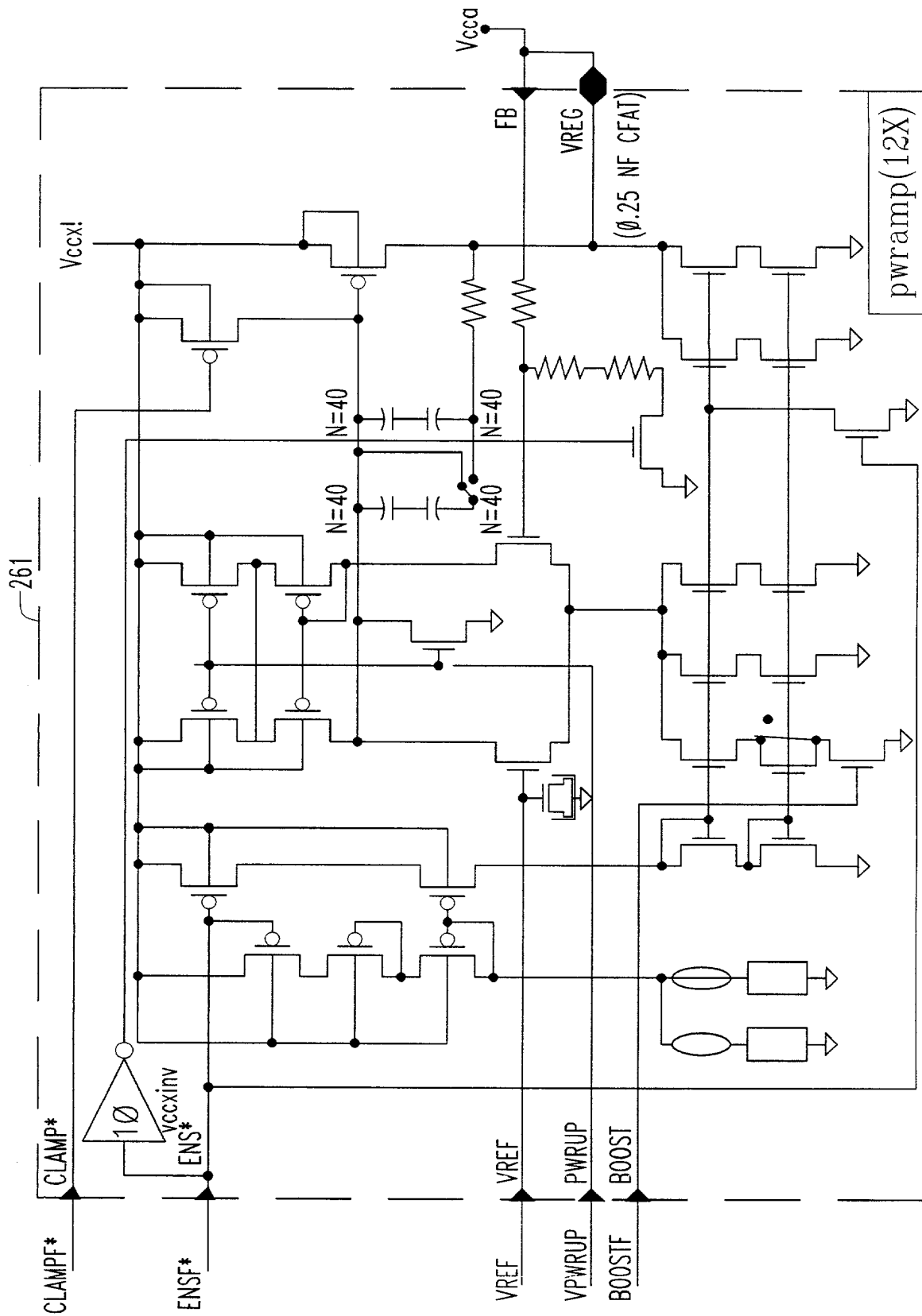


FIG. 361

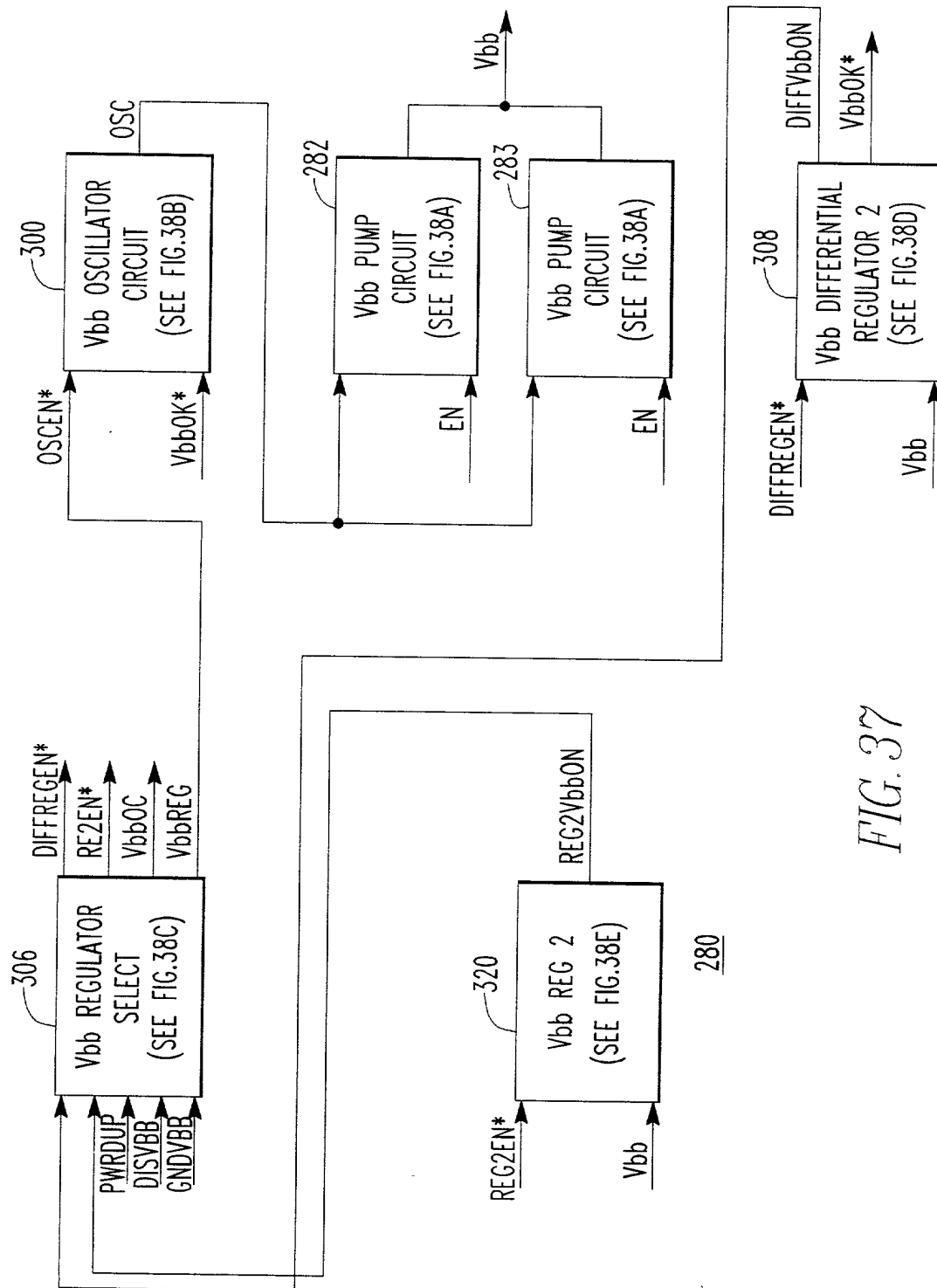


FIG. 37

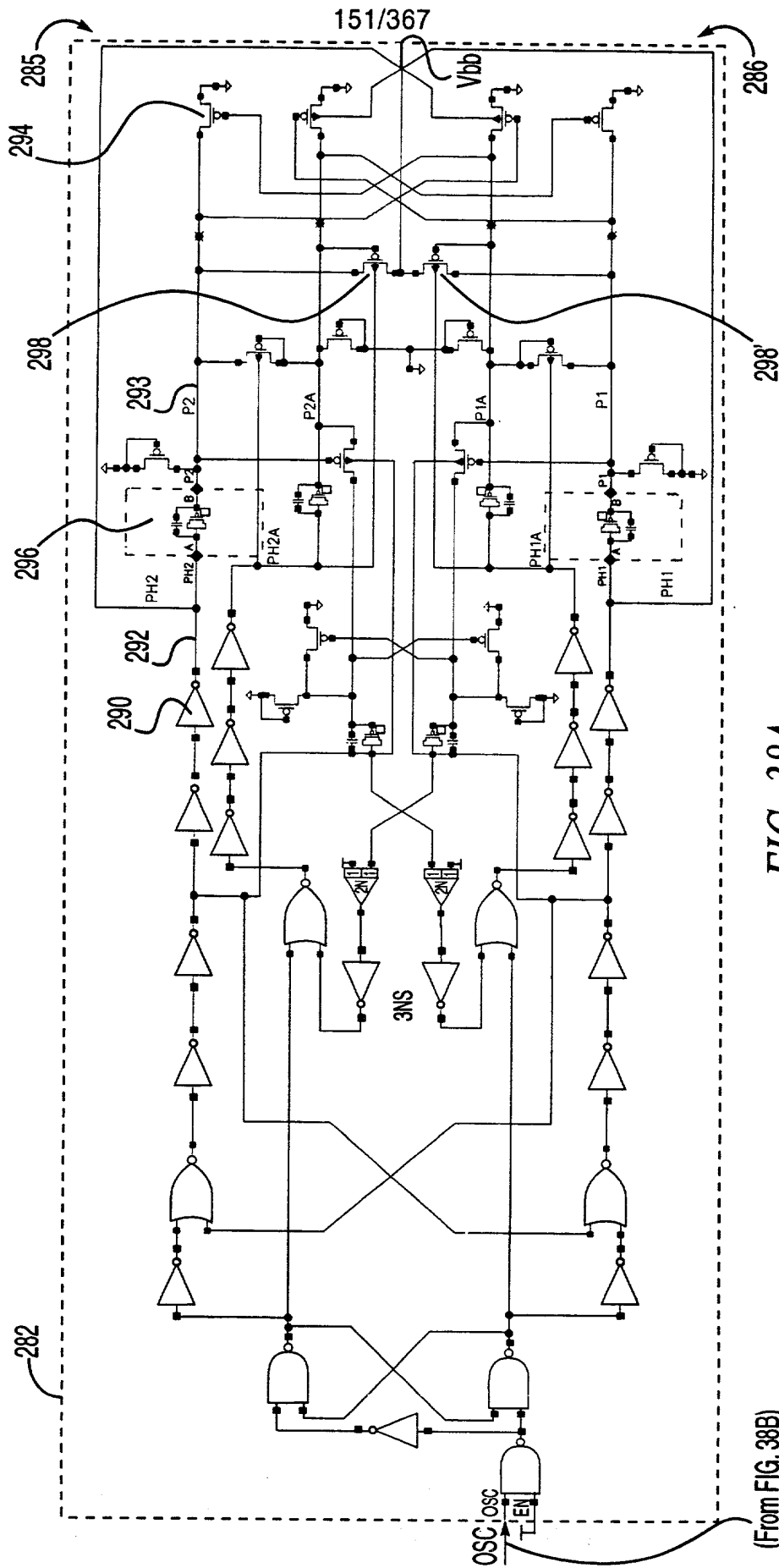
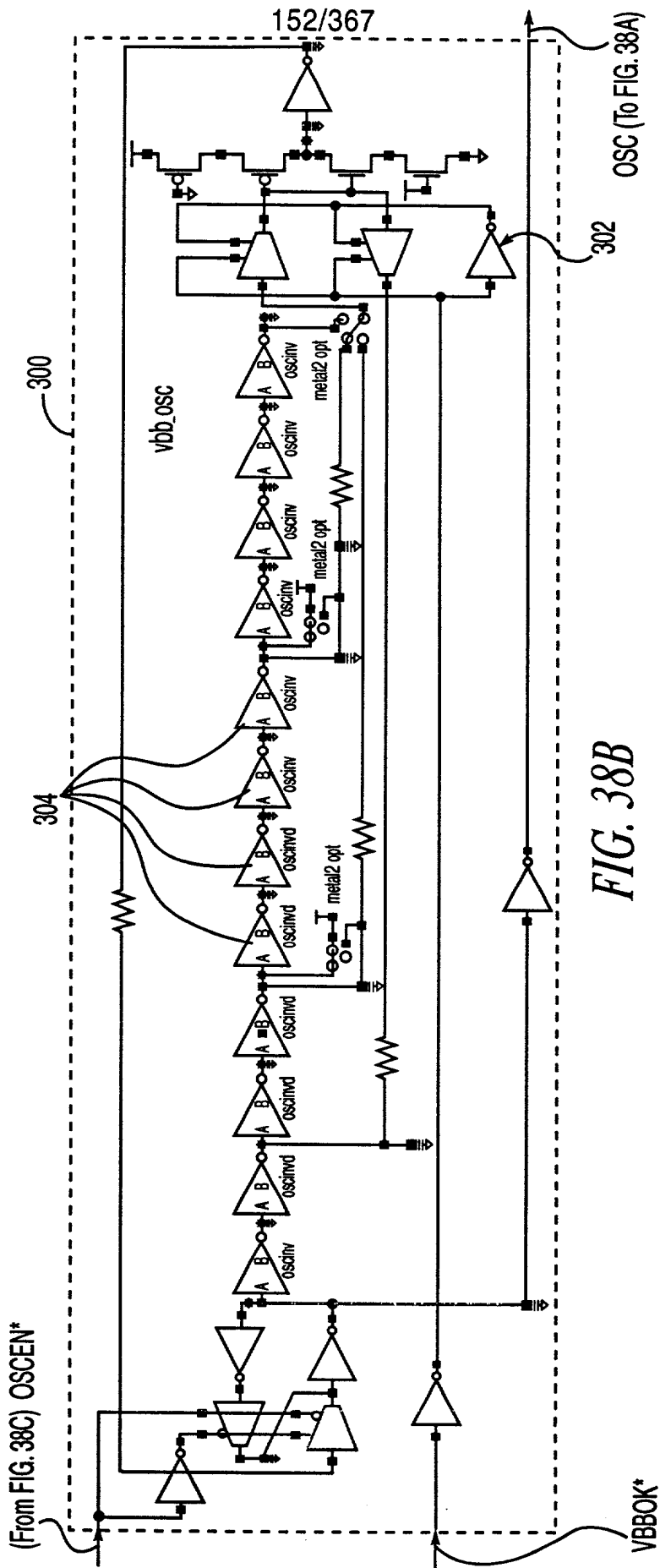


FIG. 38A

(From FIG. 38B)



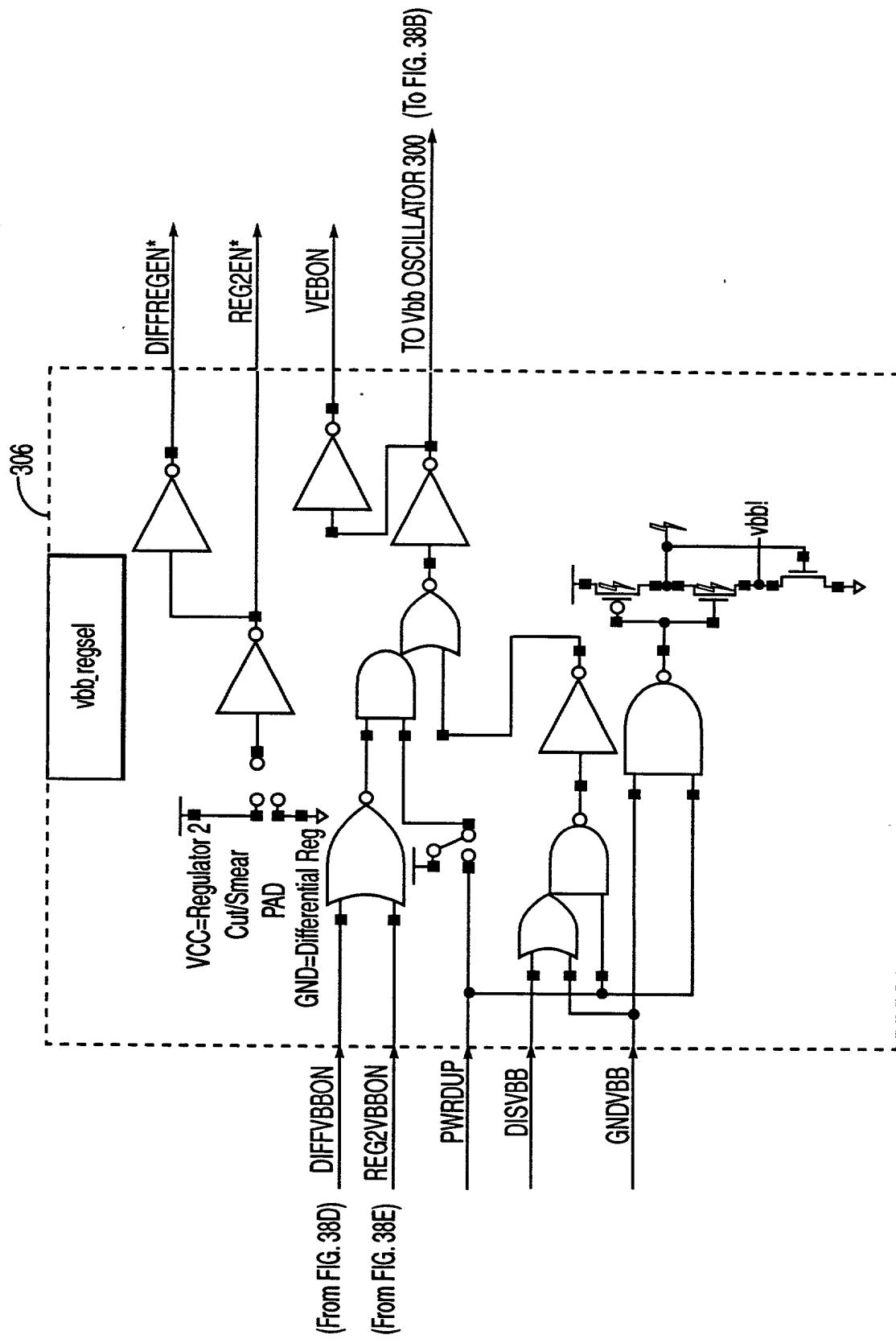
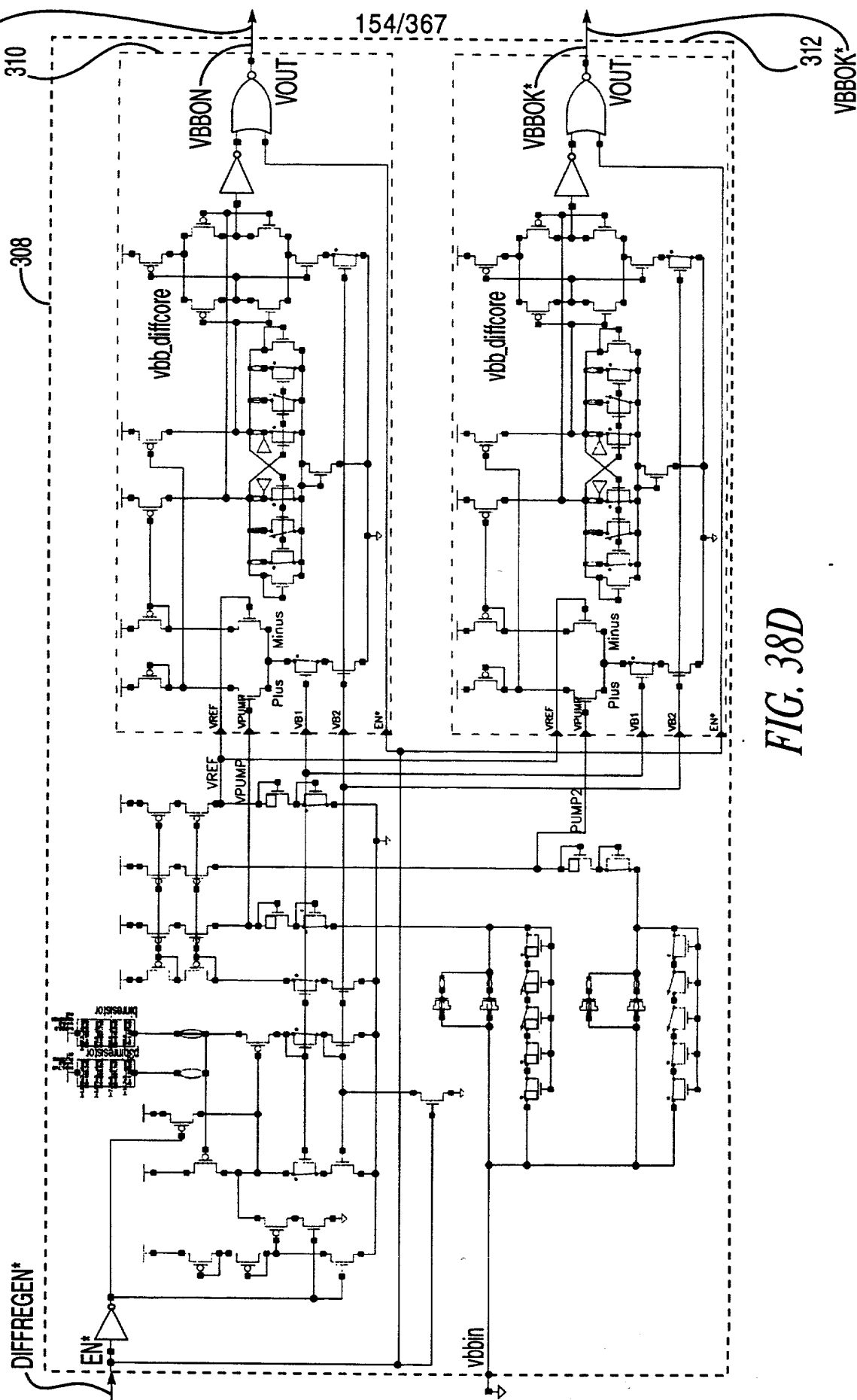


FIG. 38C



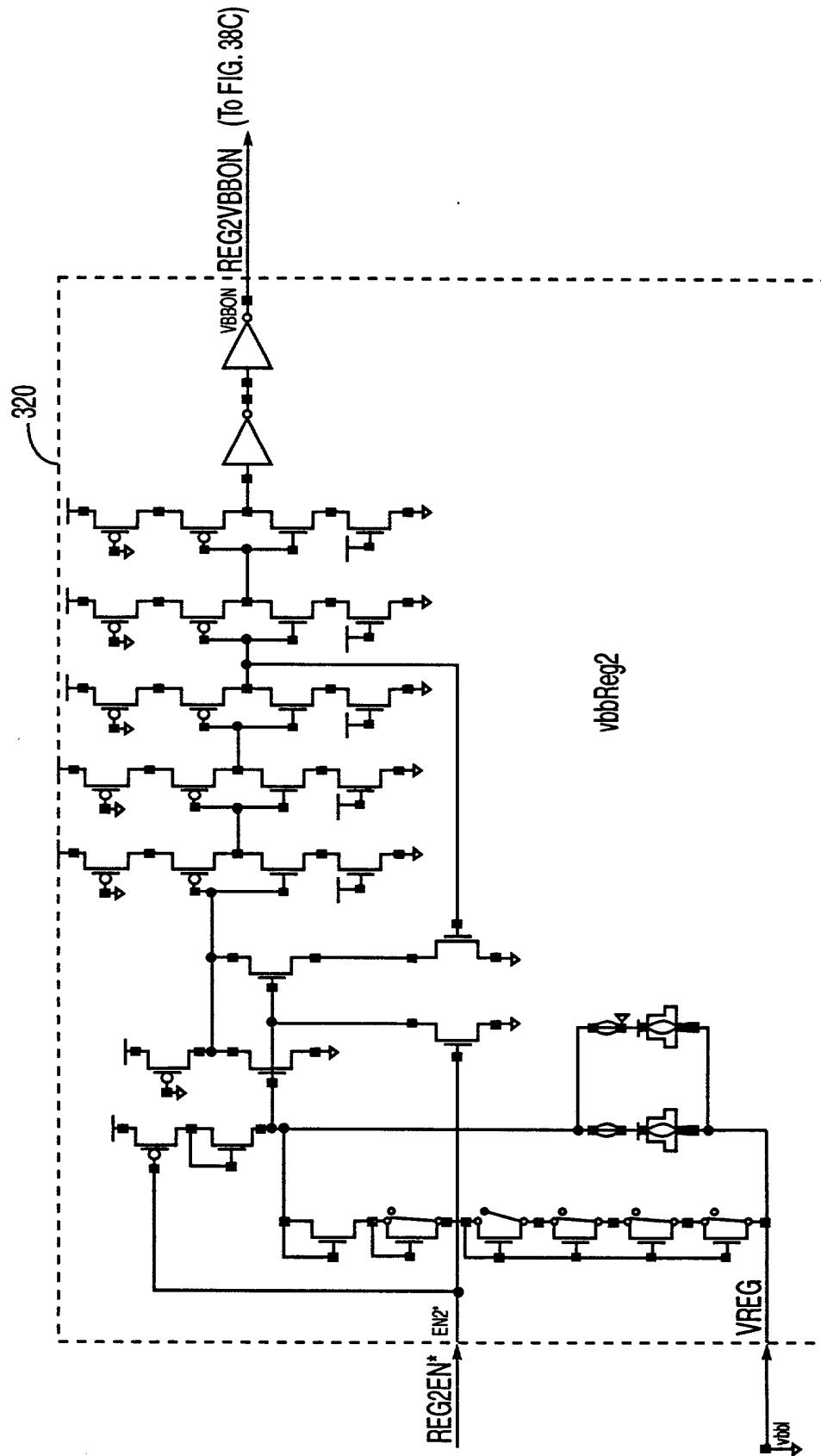


FIG. 38E

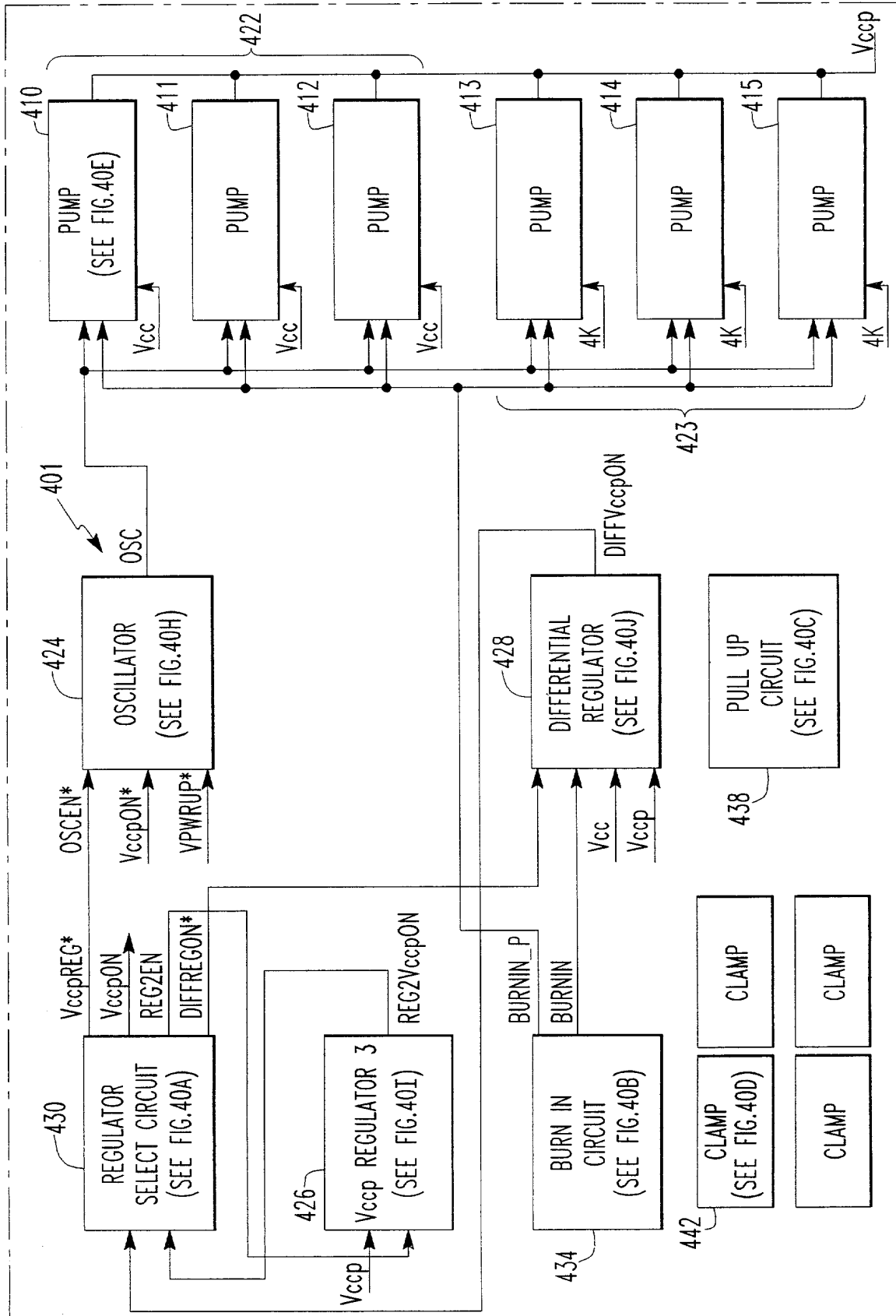


FIG. 39

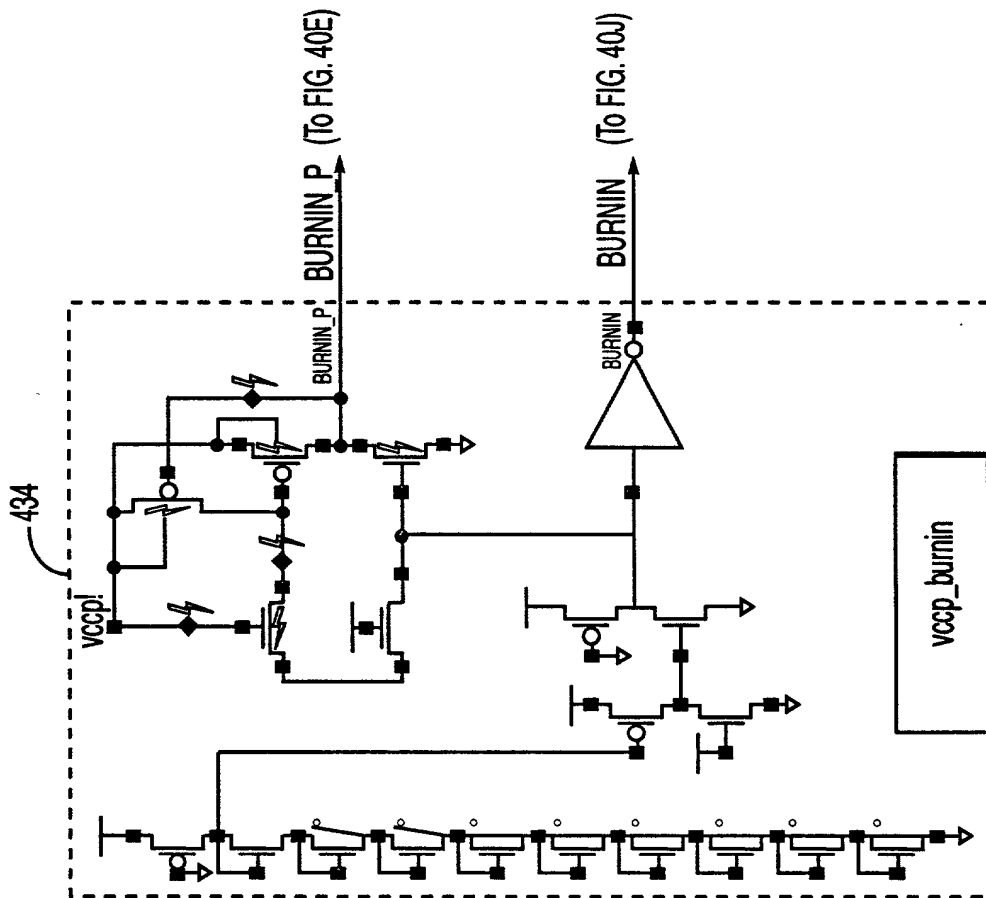


FIG. 40B

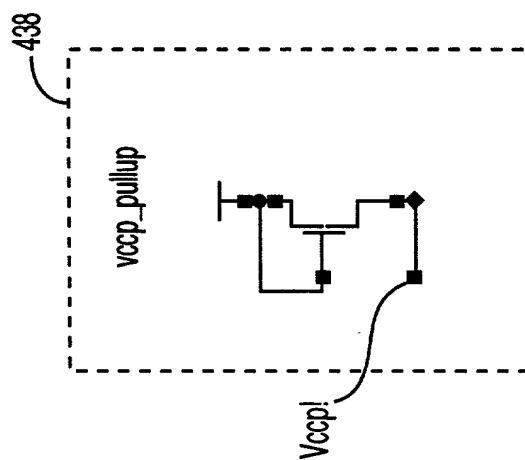


FIG. 40C

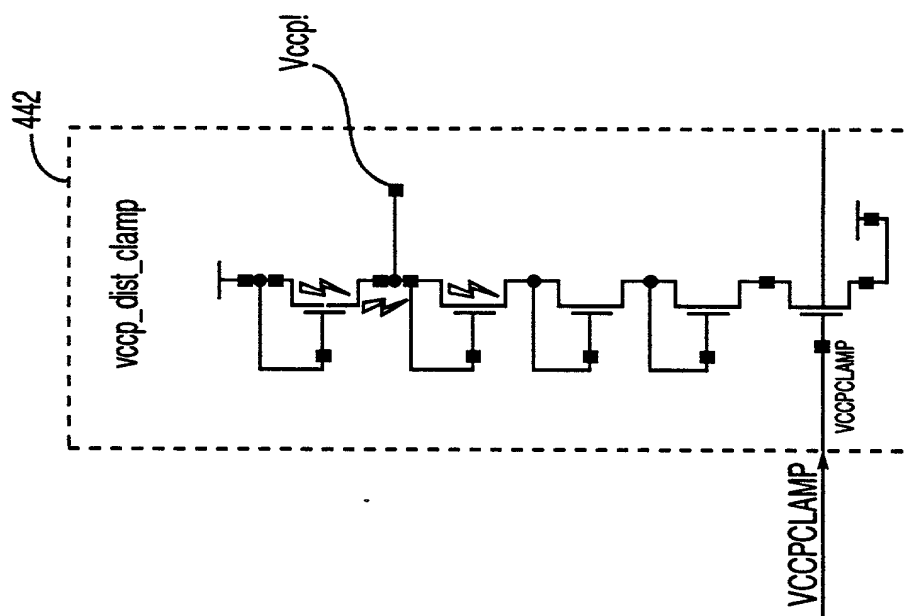


FIG. 40D

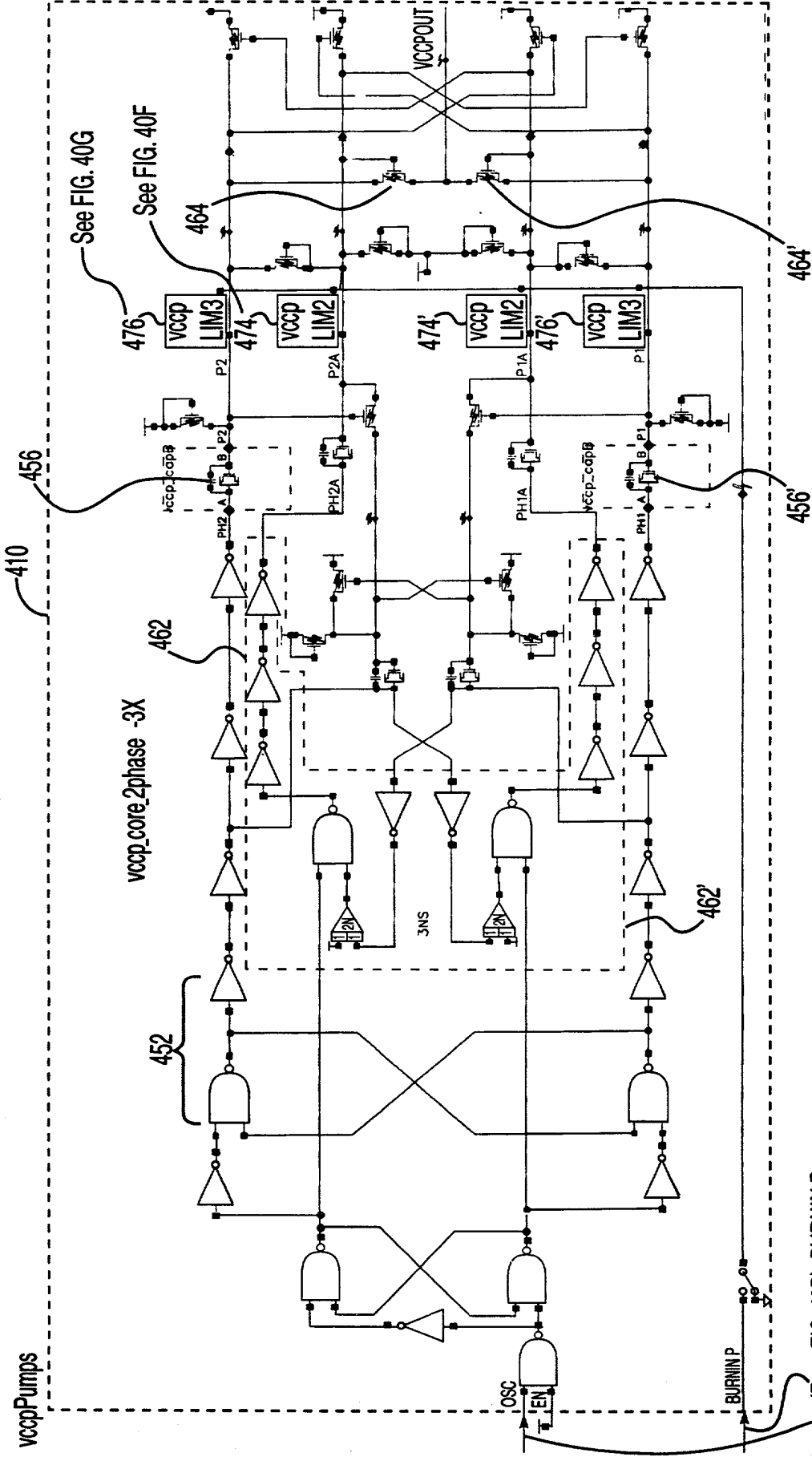


FIG. 40E

(From FIG. 40B) BURIN P

(From FIG. 40H) VCCPOSC

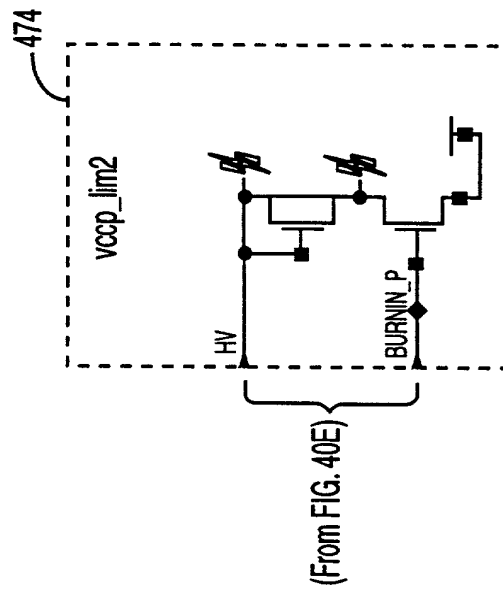


FIG. 40F

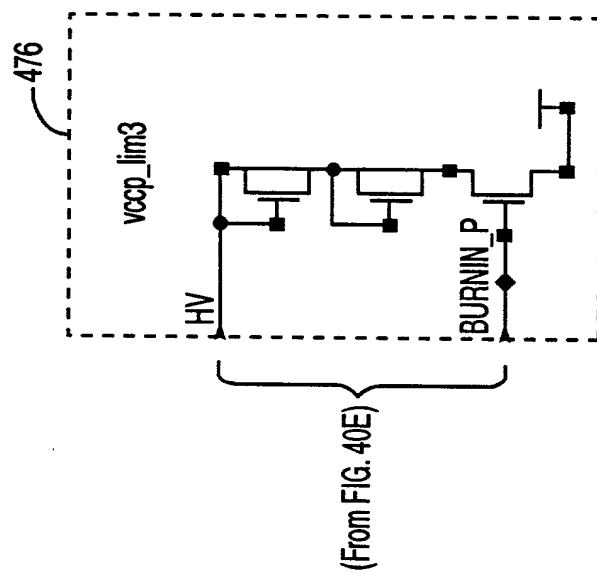
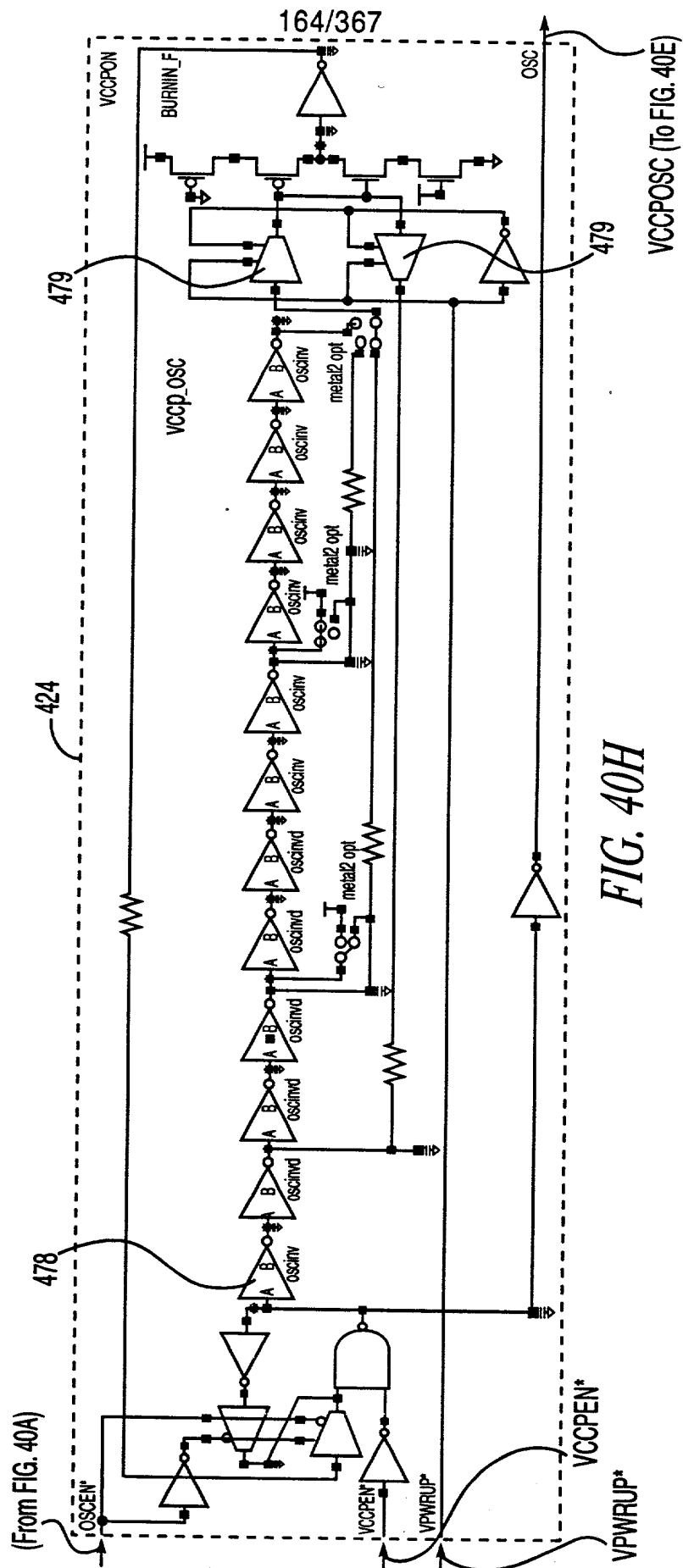


FIG. 40G



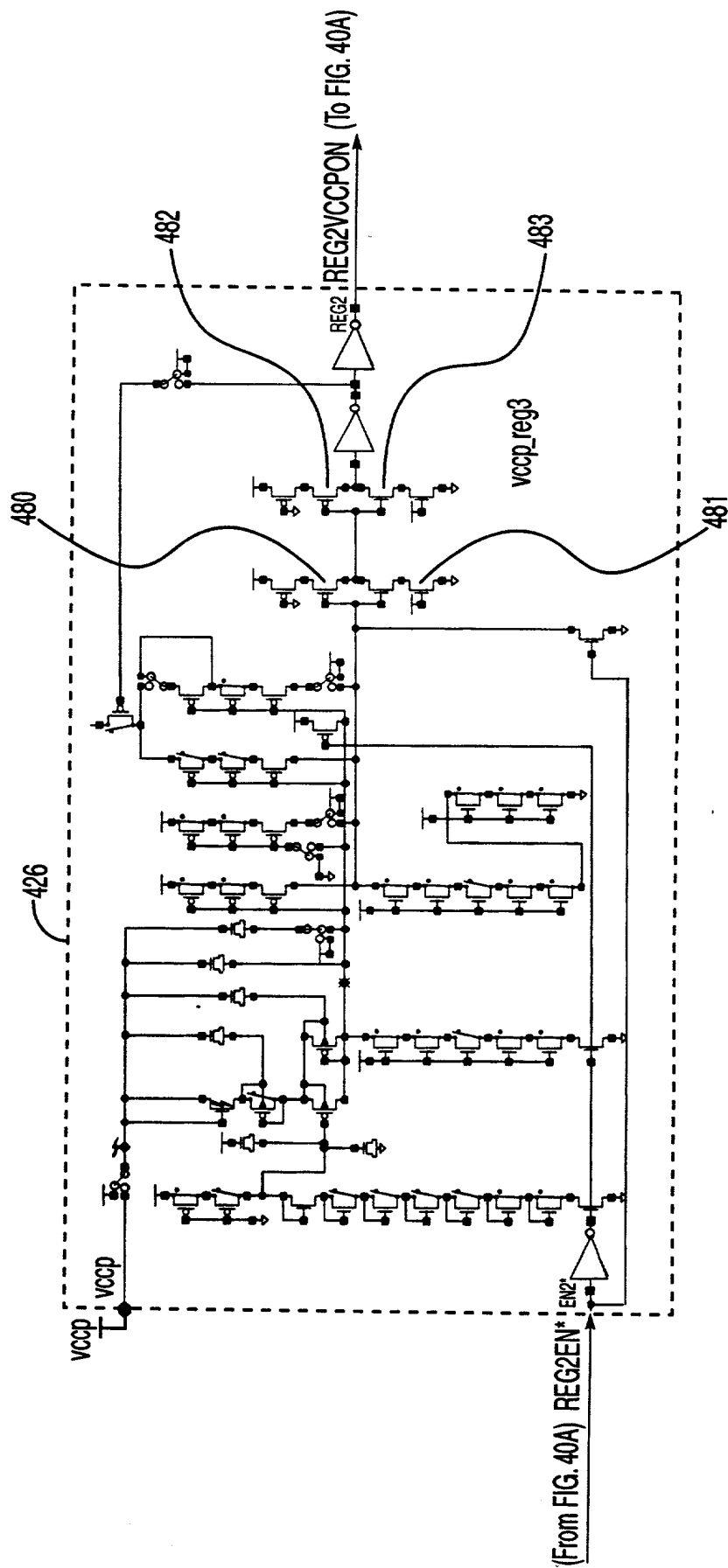


FIG. 40I

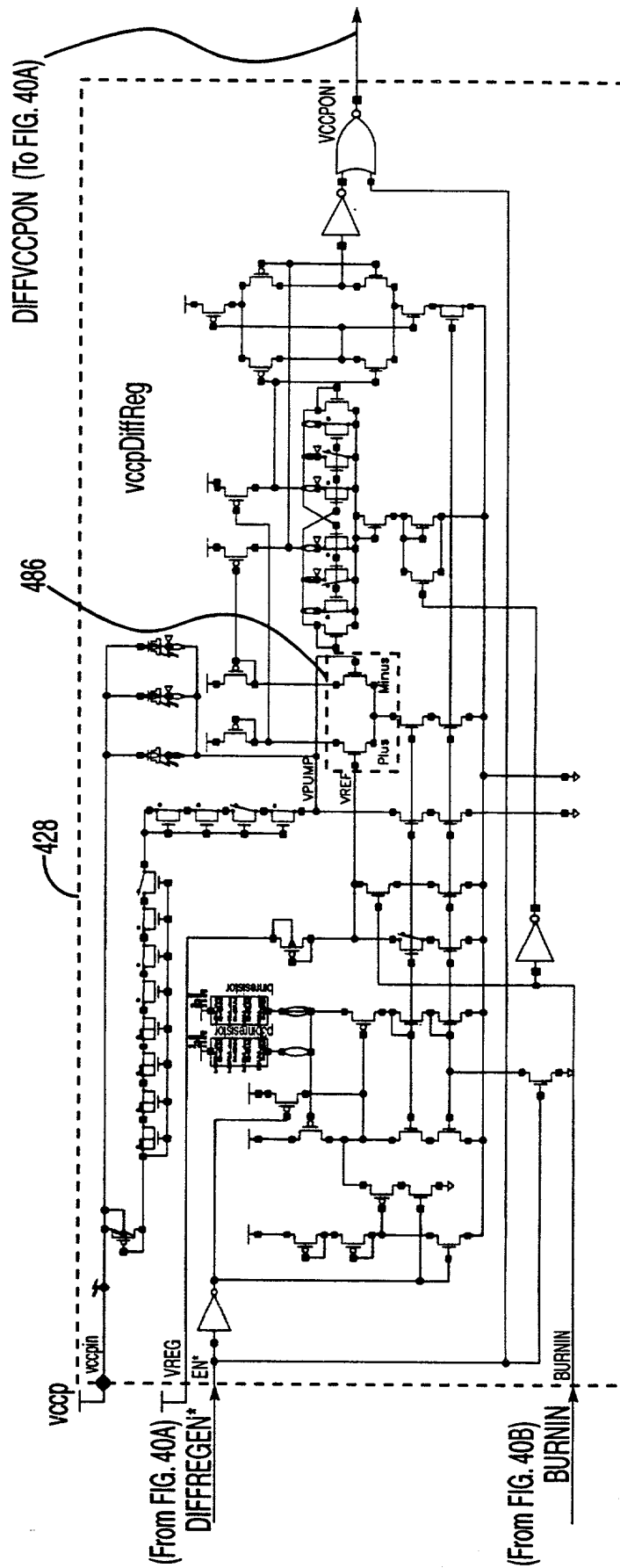


FIG. 40J

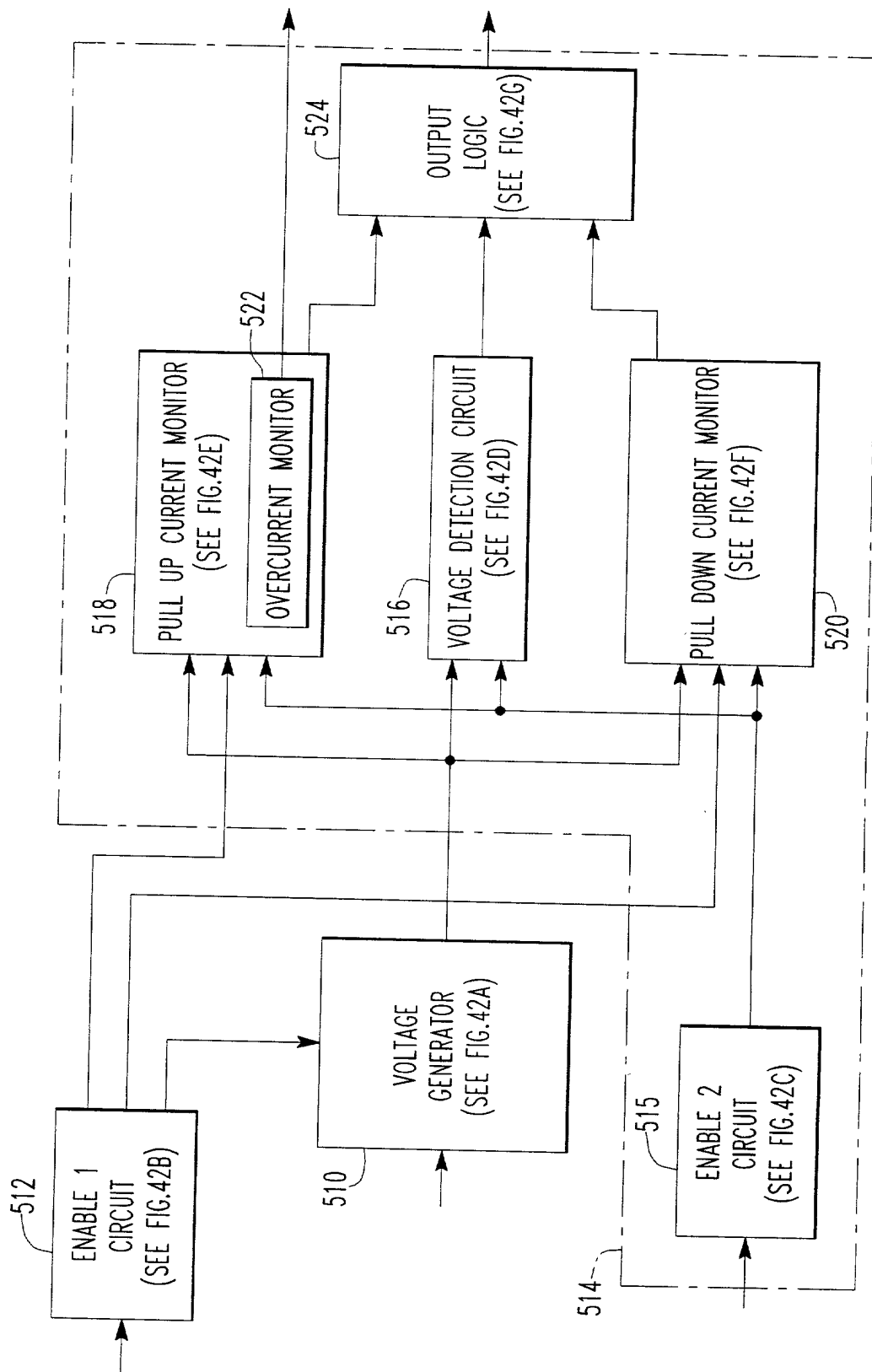
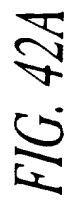


FIG. 41

500



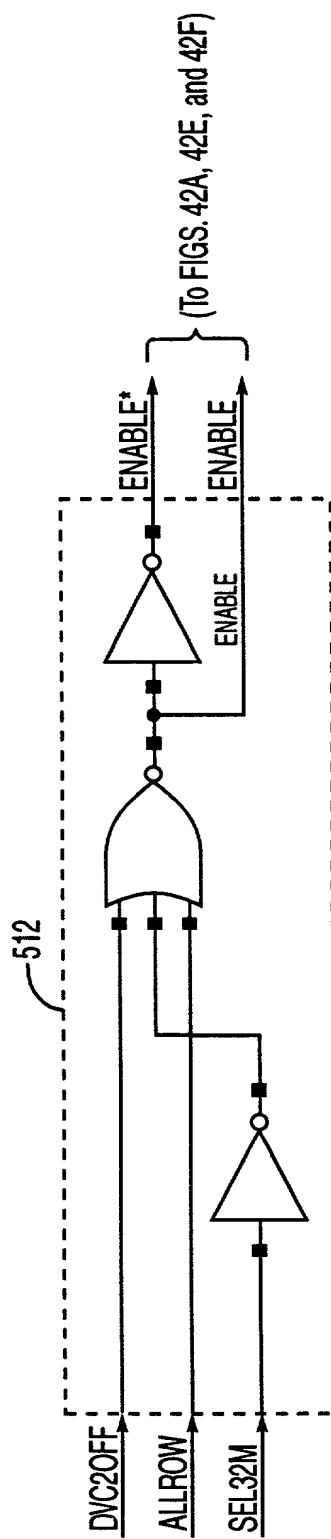


FIG. 42B

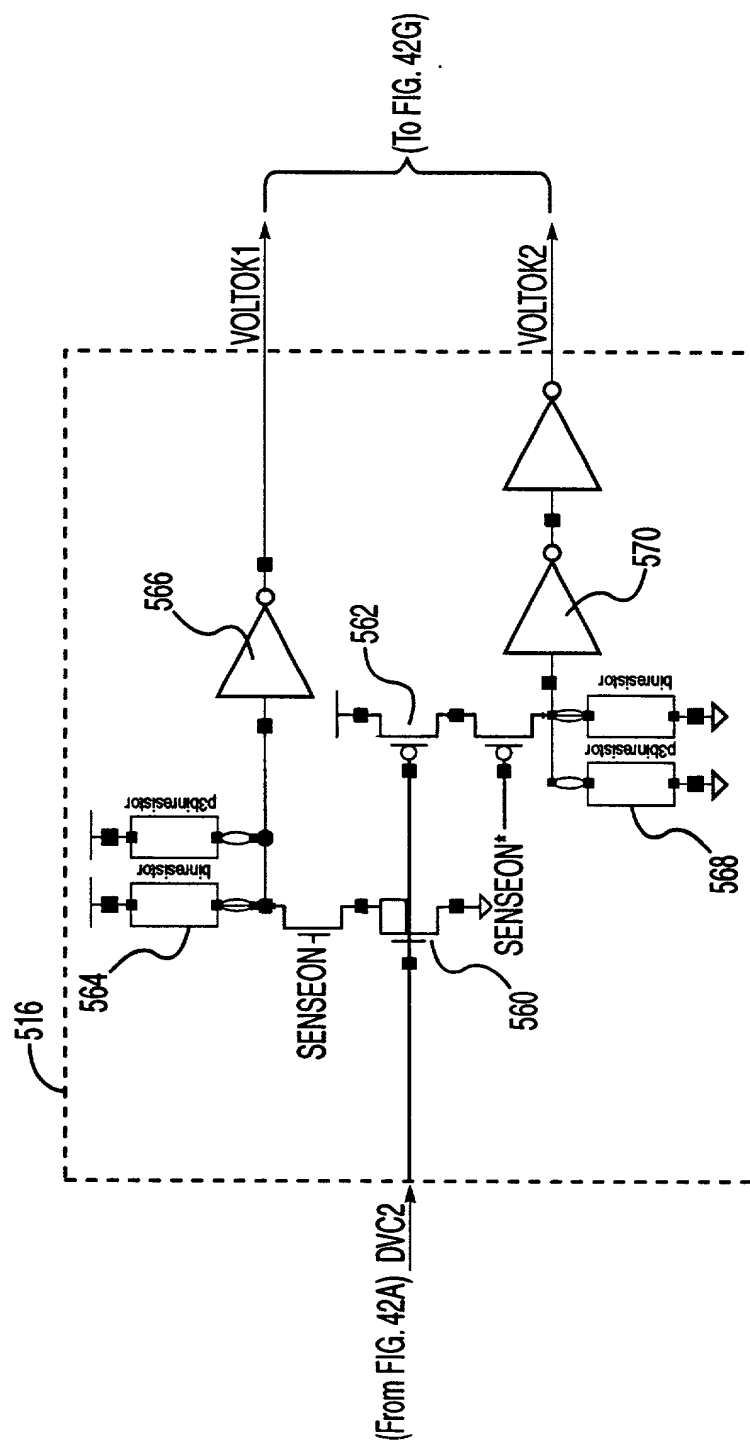


FIG. 42D

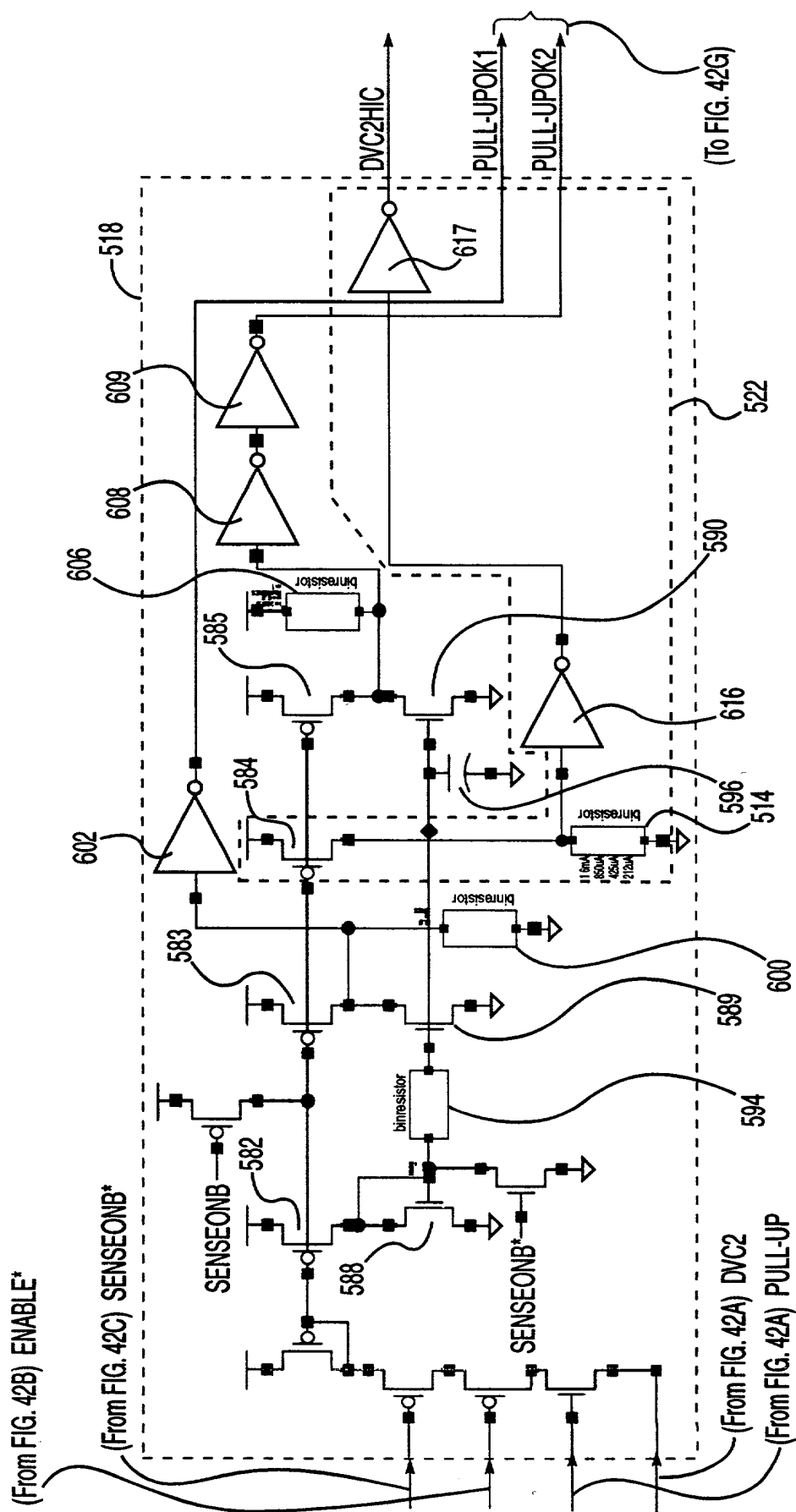


FIG. 42E

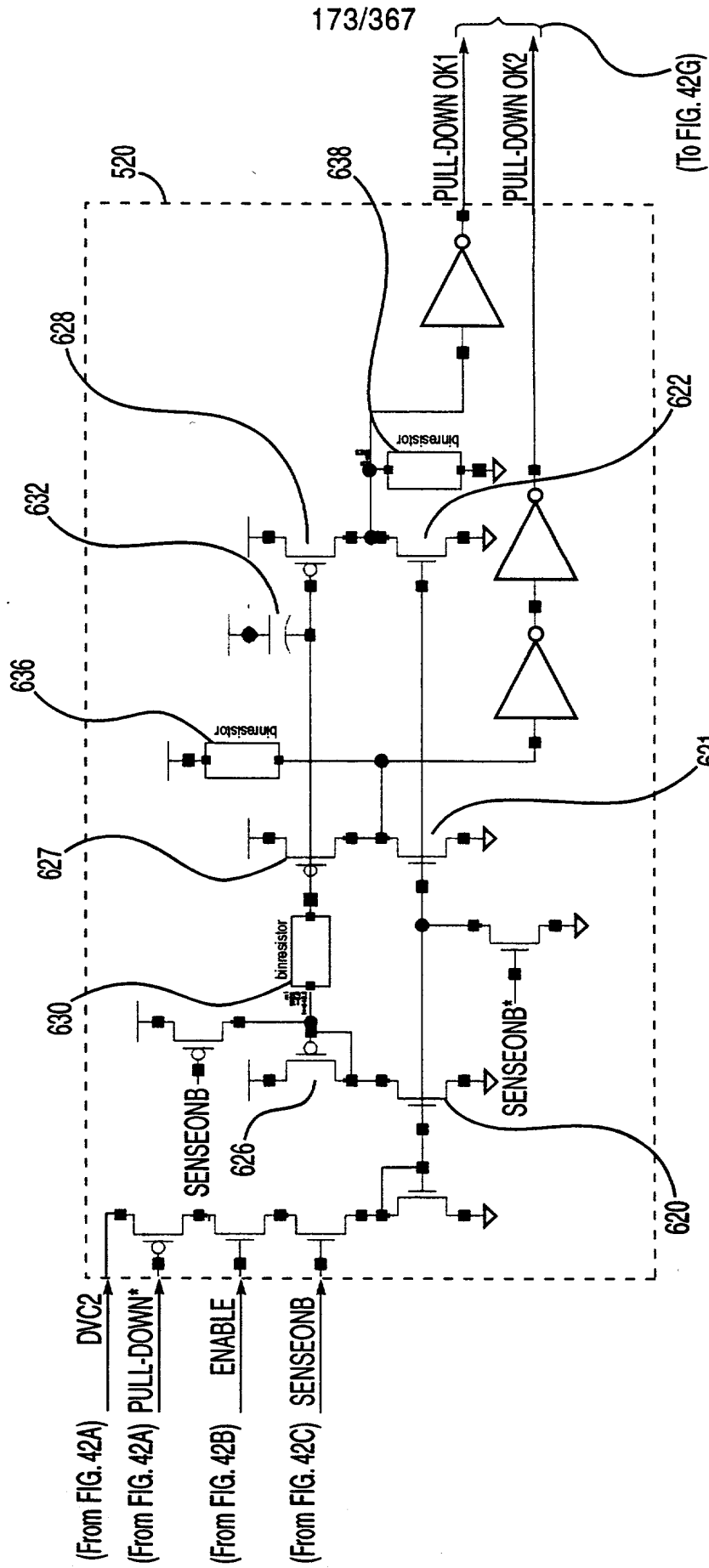


FIG. 42F

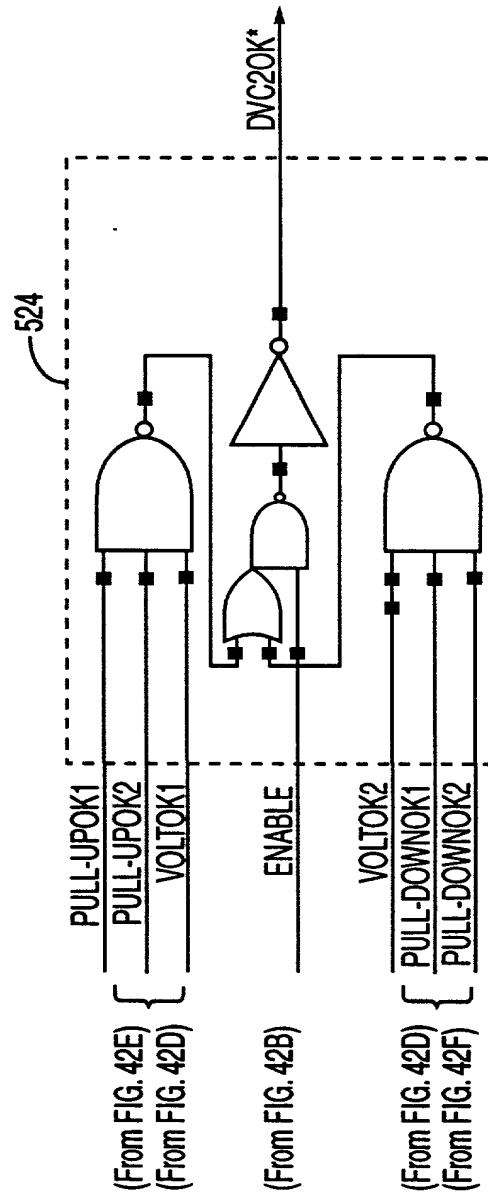


FIG. 42G

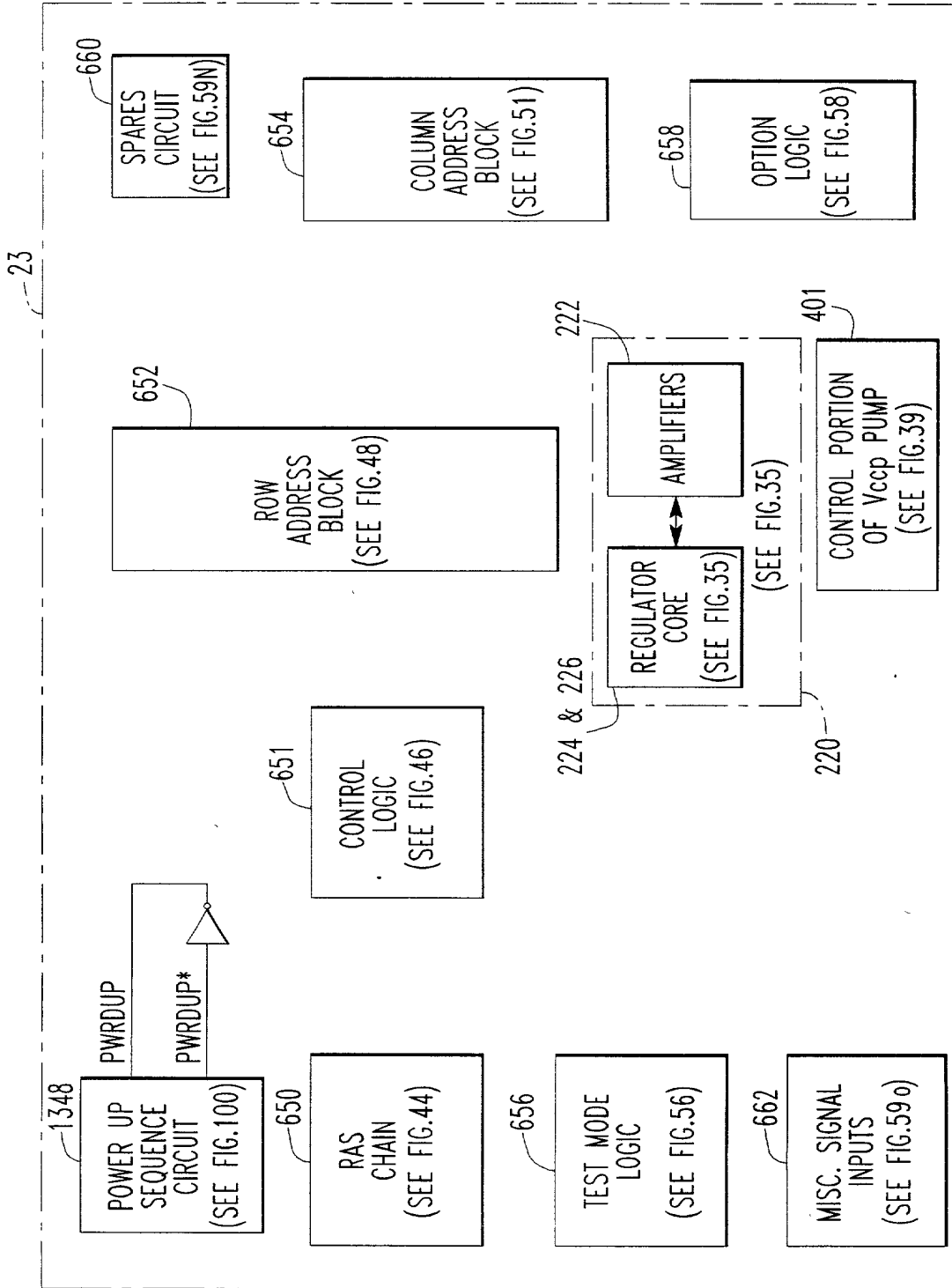


FIG. 43

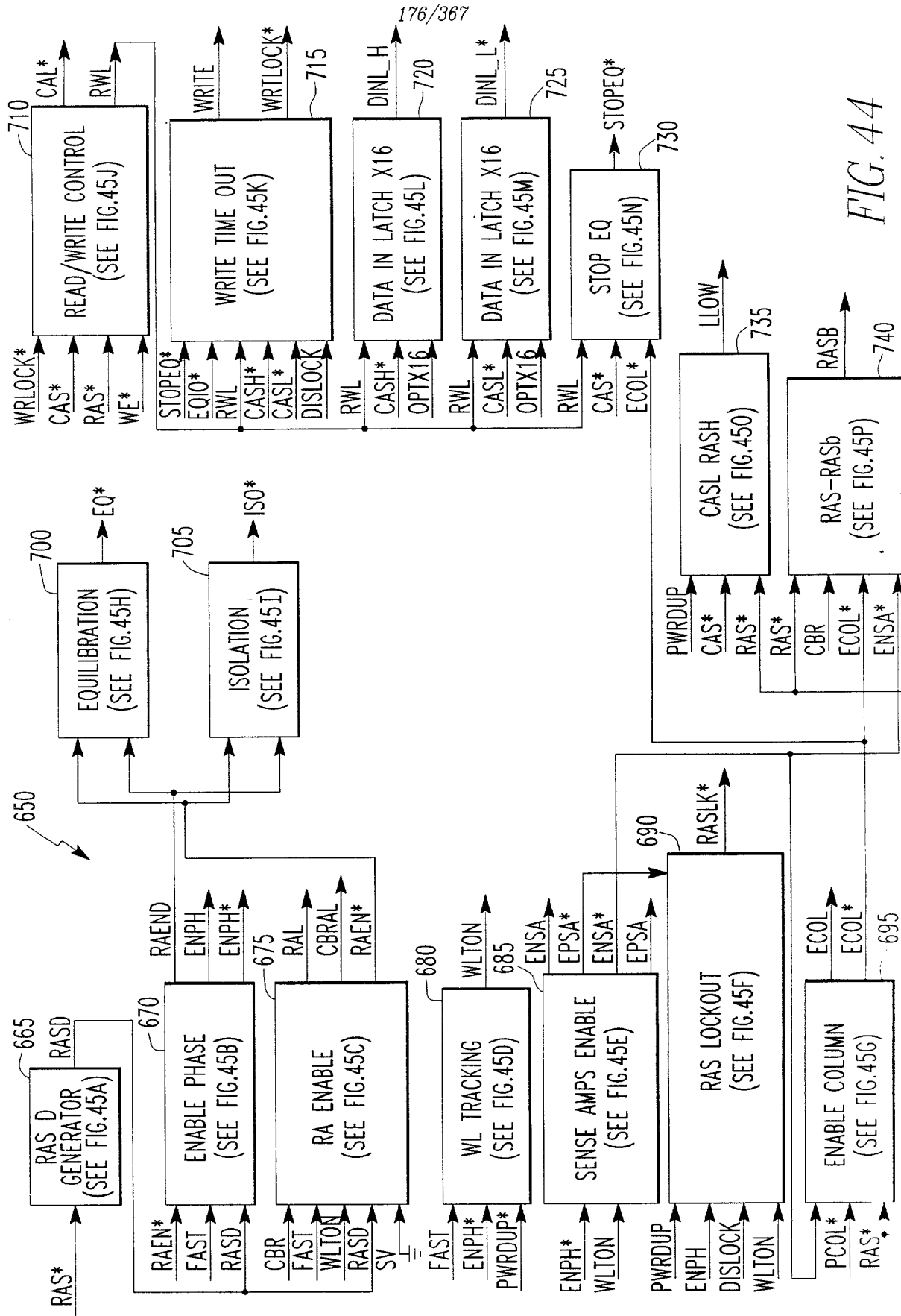


FIG. 44

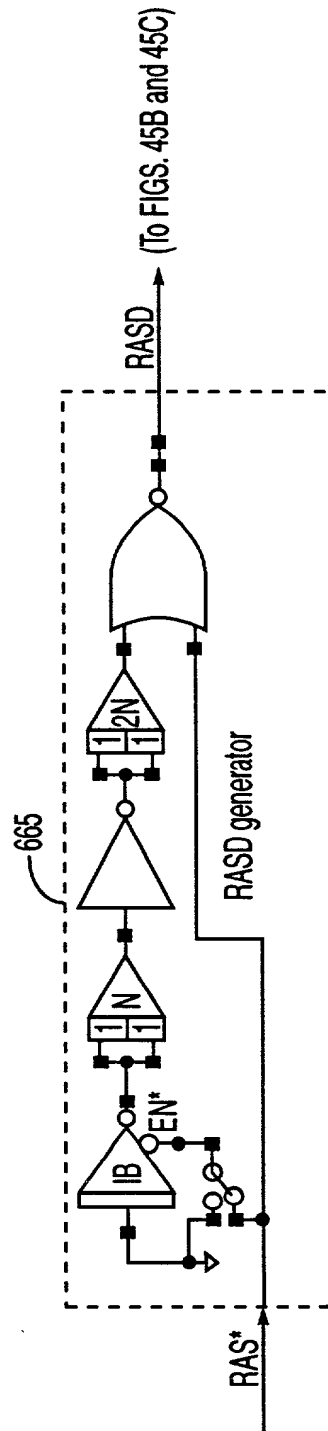


FIG. 45A

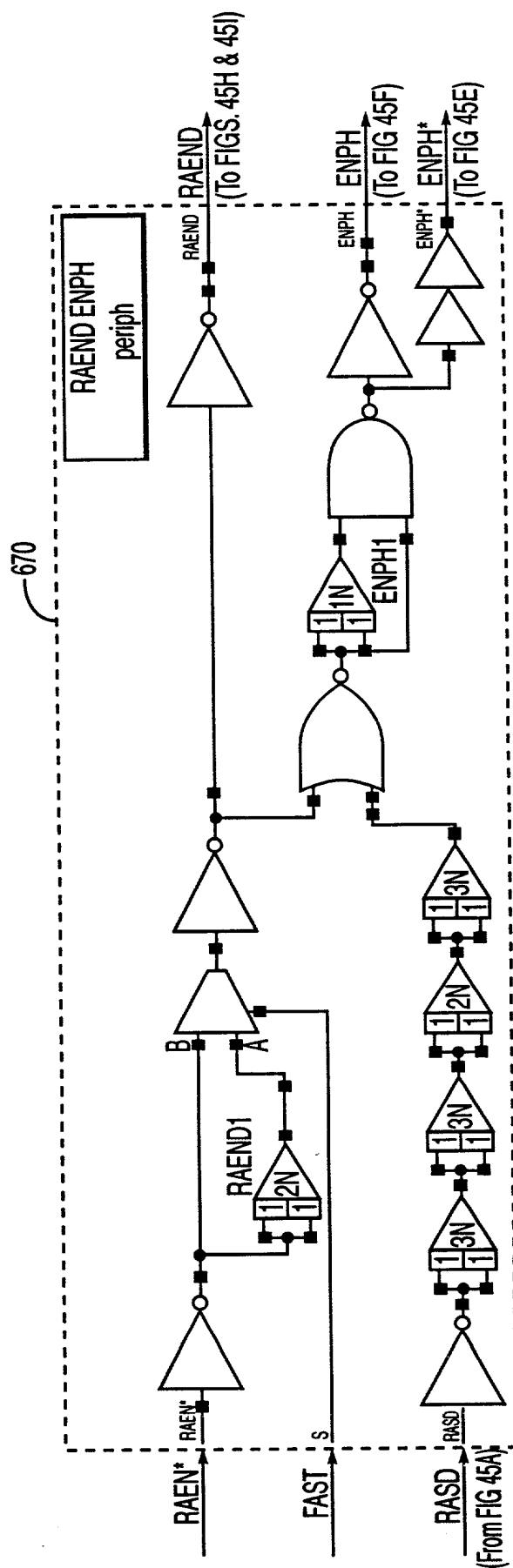


FIG. 45B

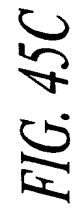


FIG. 45C

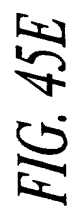
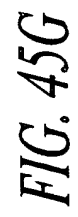


FIG. 45E



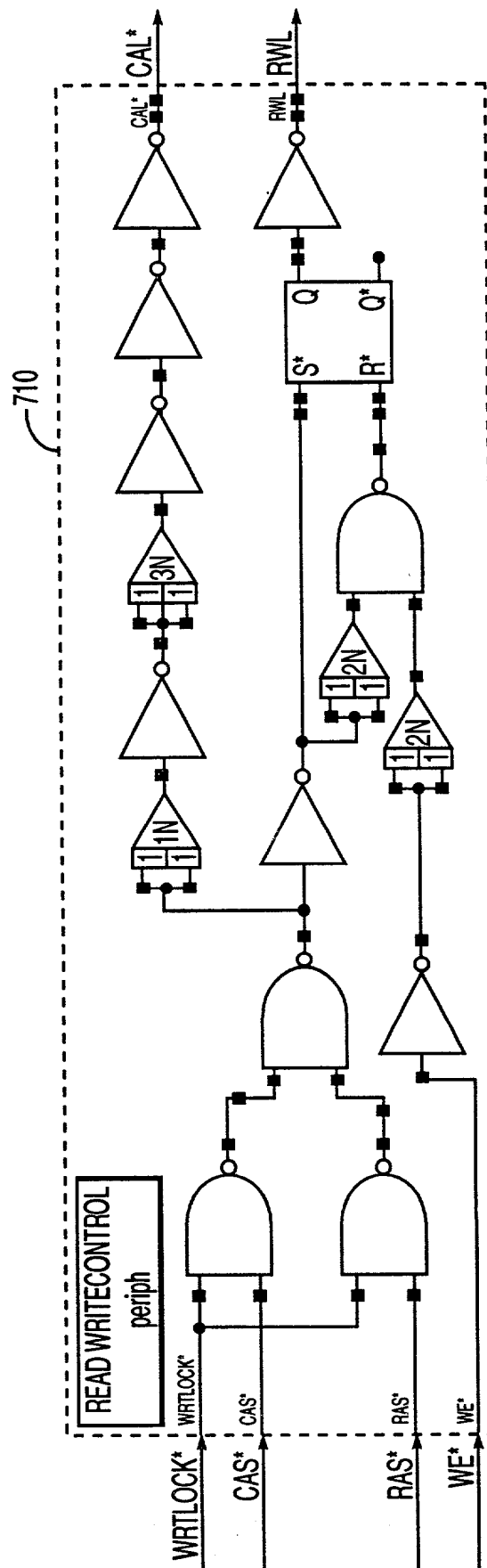


FIG. 45J

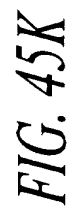


FIG. 45K

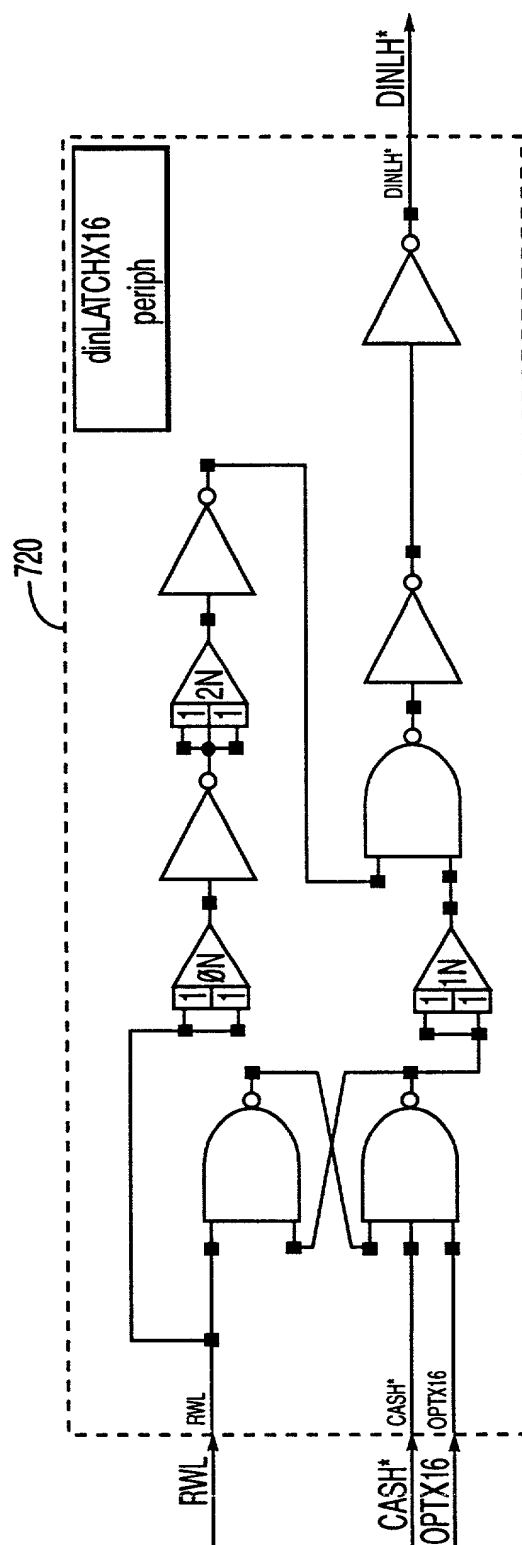


FIG. 45L

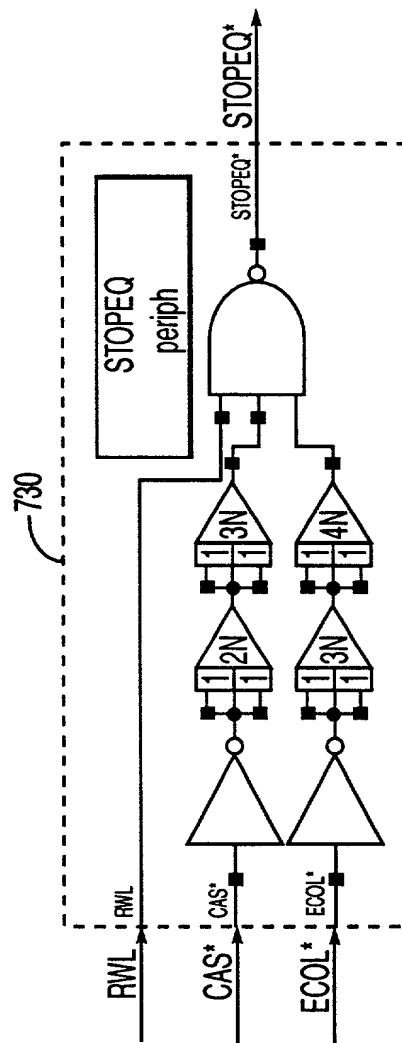


FIG. 45N

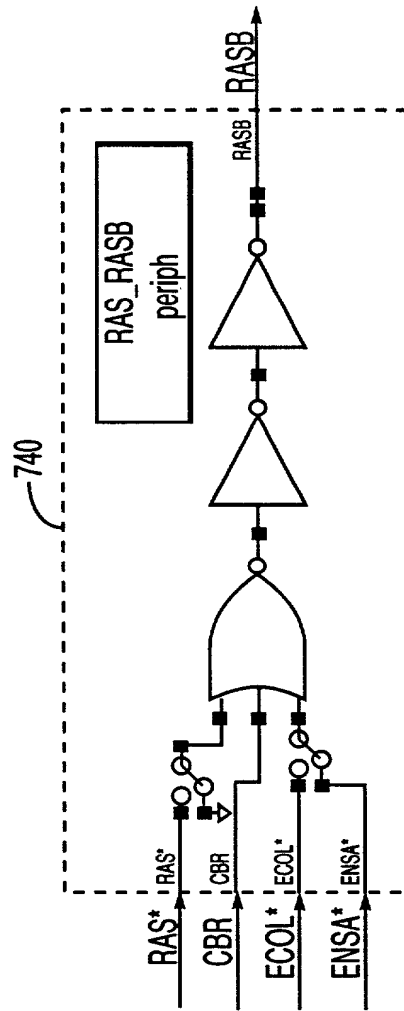


FIG. 45P

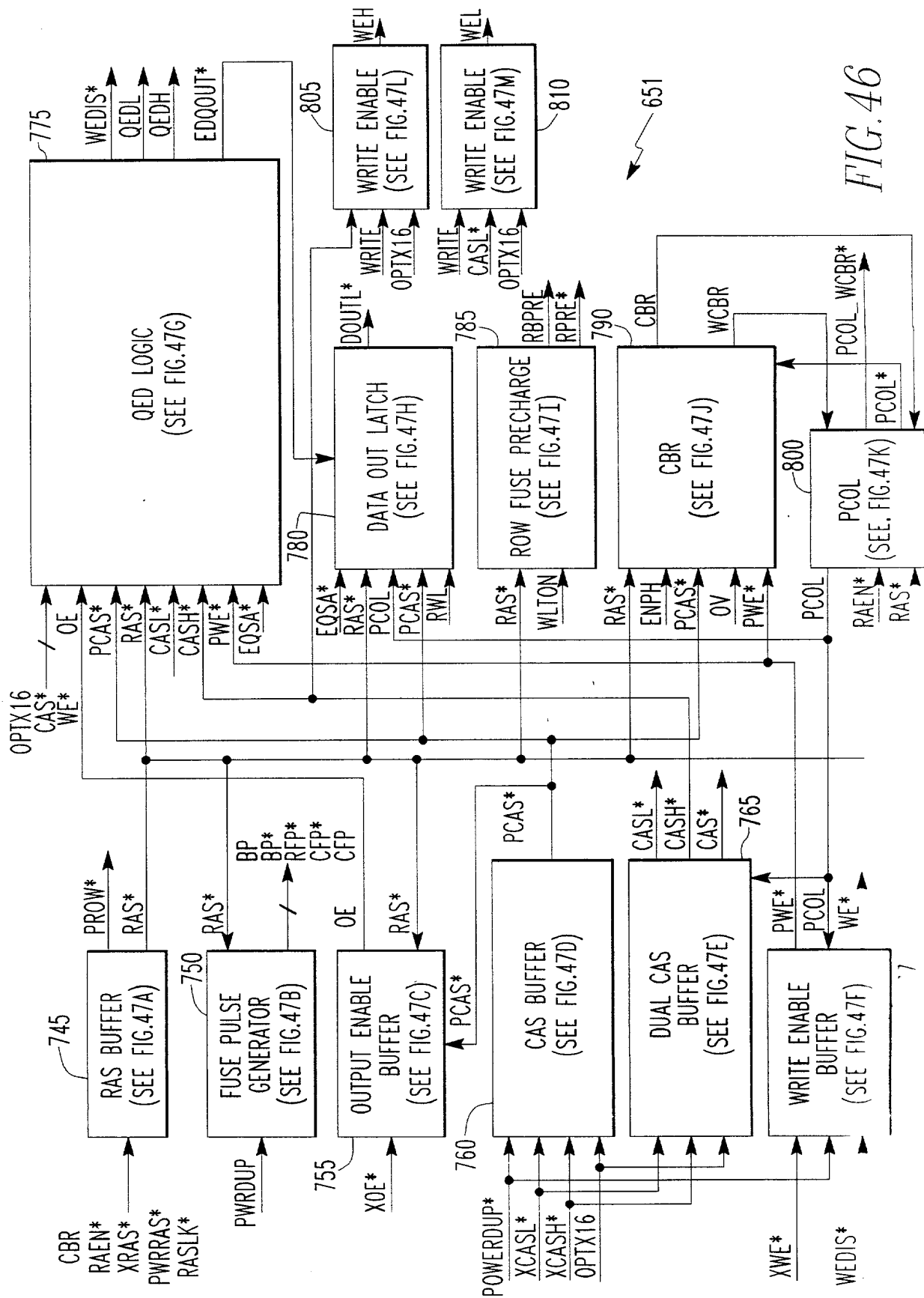


FIG. 46

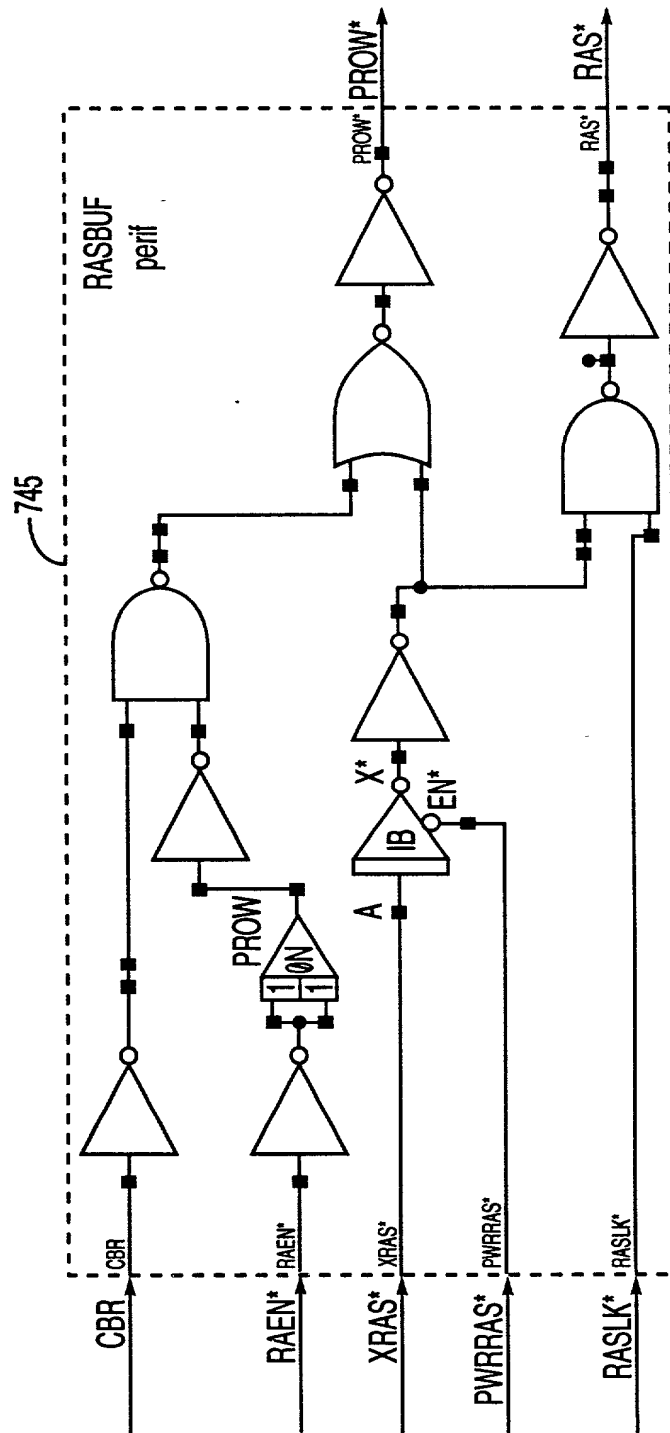


FIG. 47A

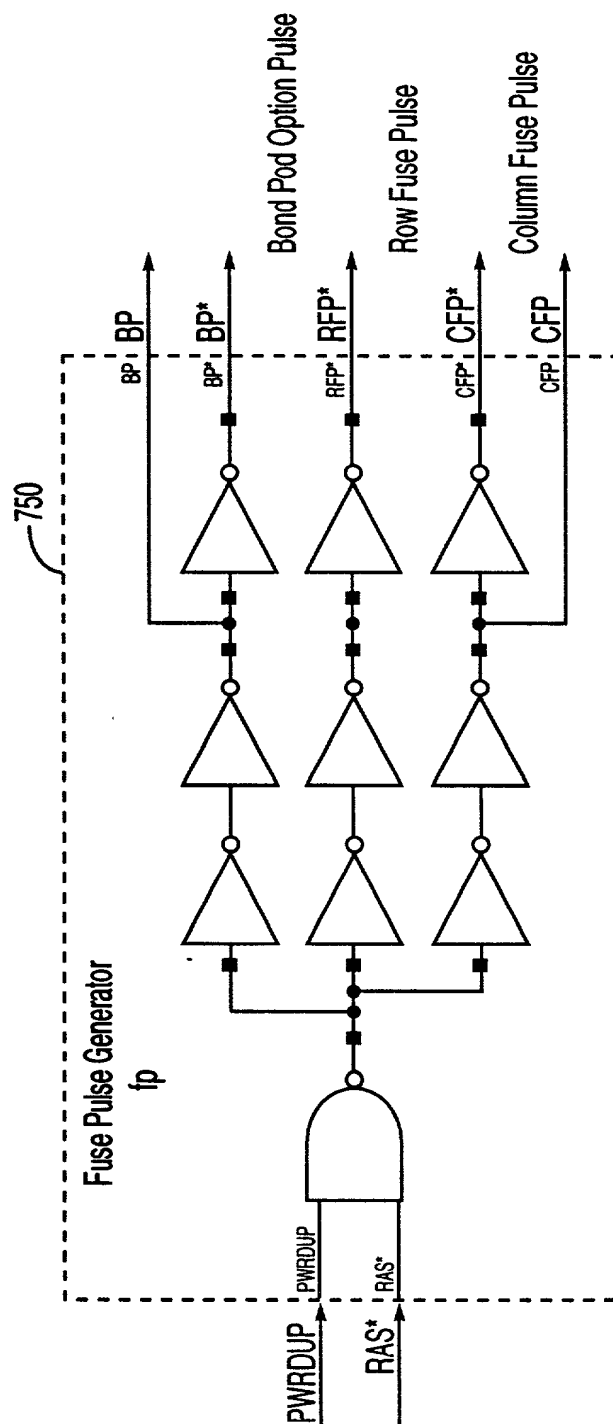


FIG. 47B

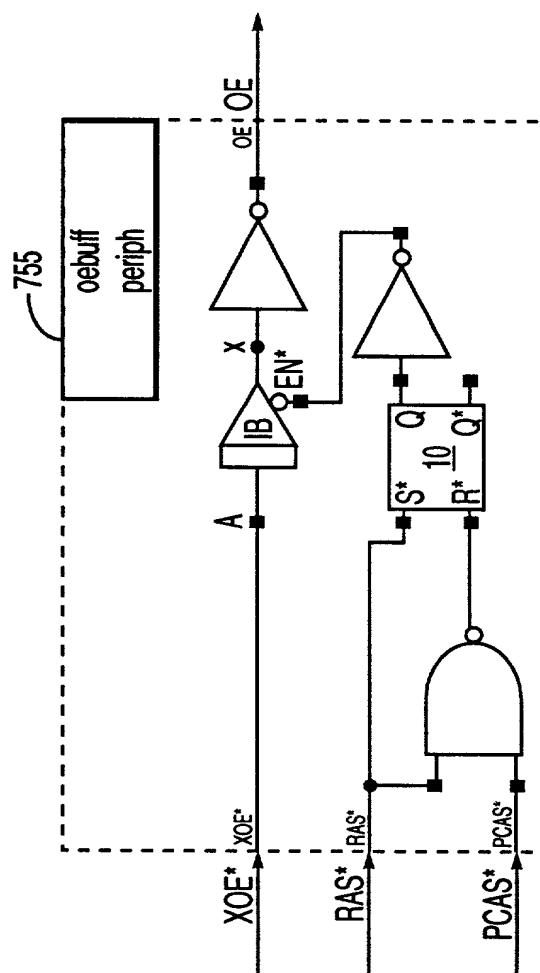


FIG. 47C

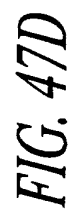


FIG. 47D

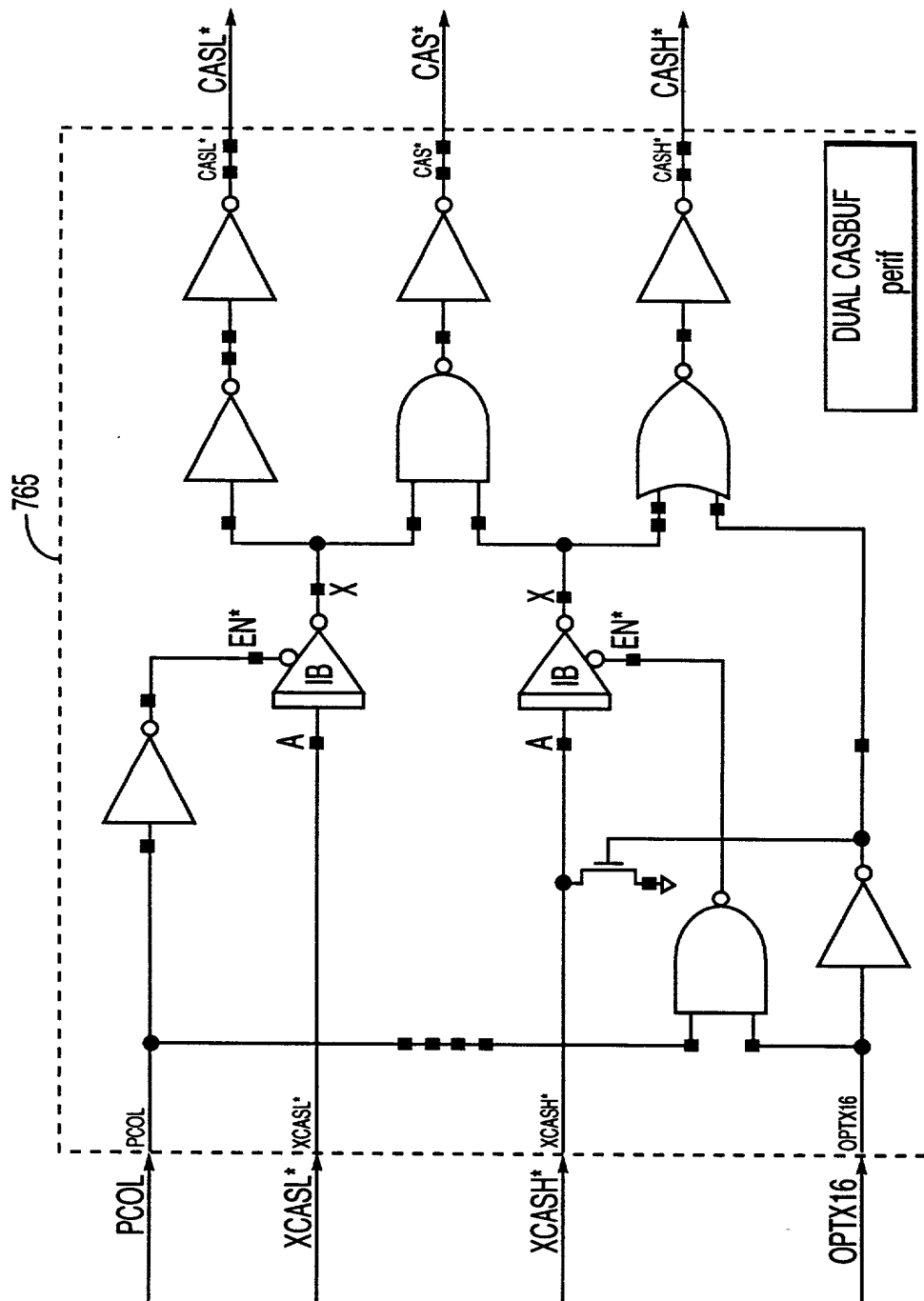


FIG. 47E

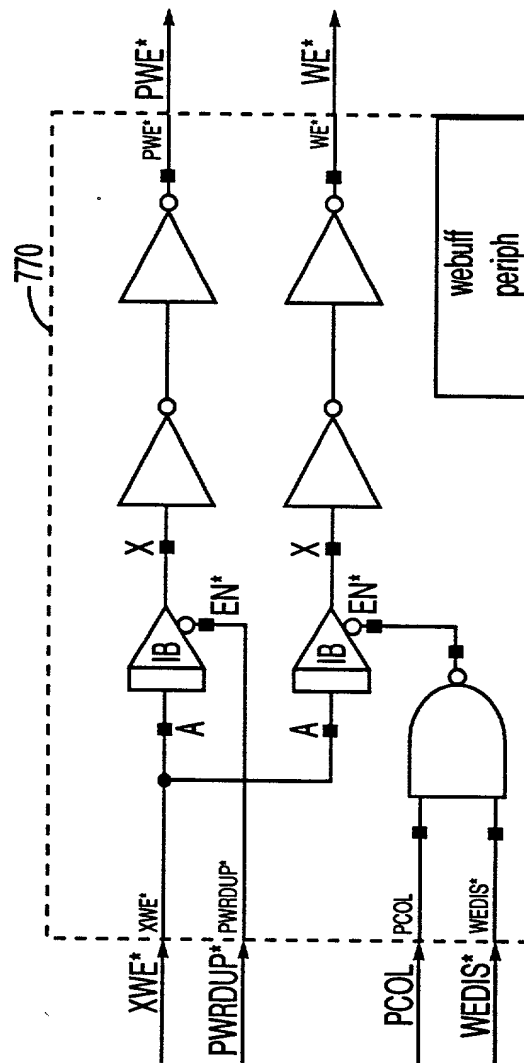


FIG. 47F

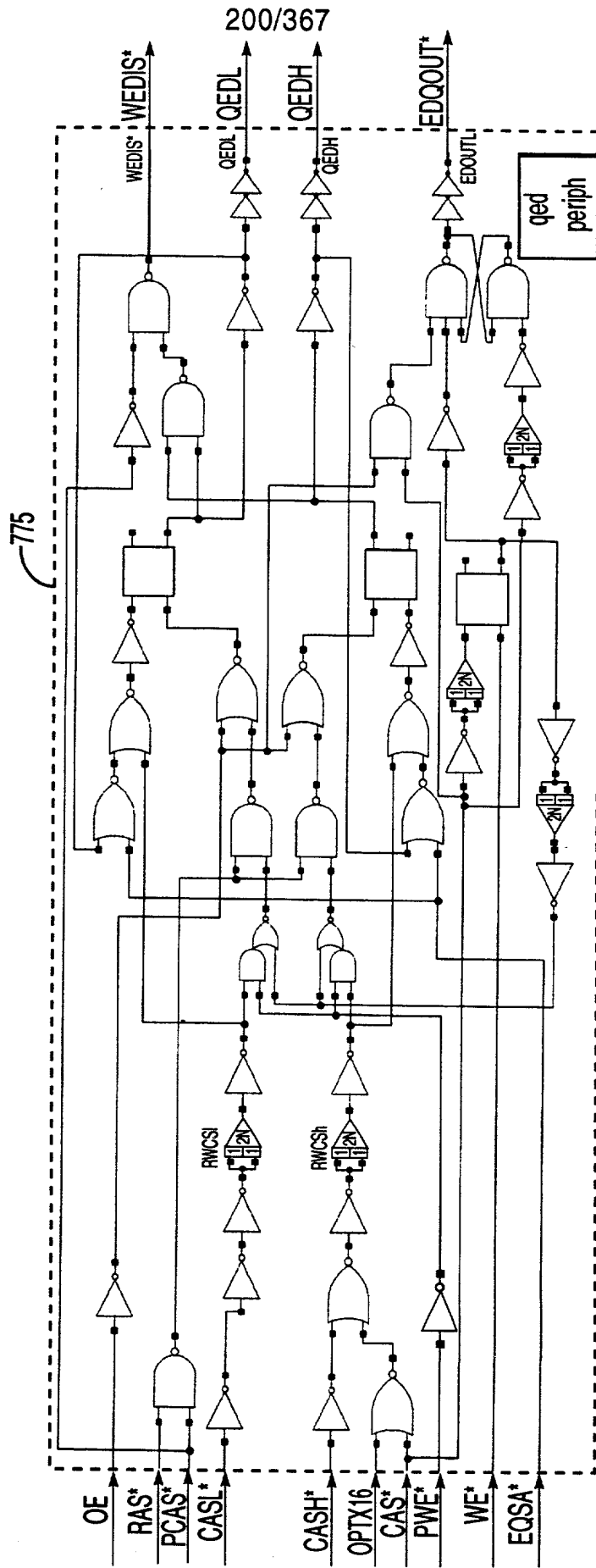


FIG. 47G

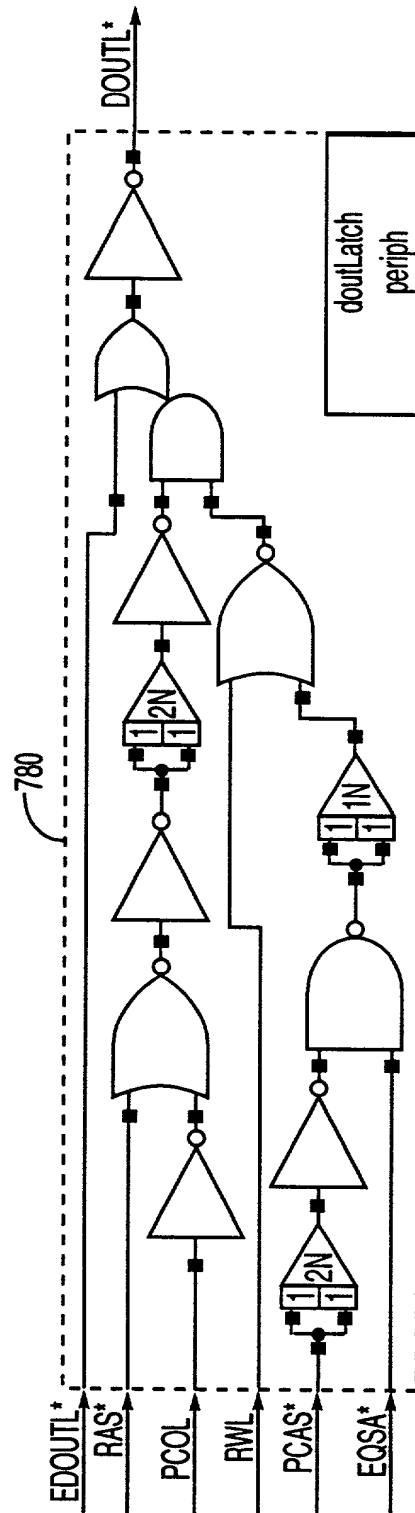


FIG. 47H

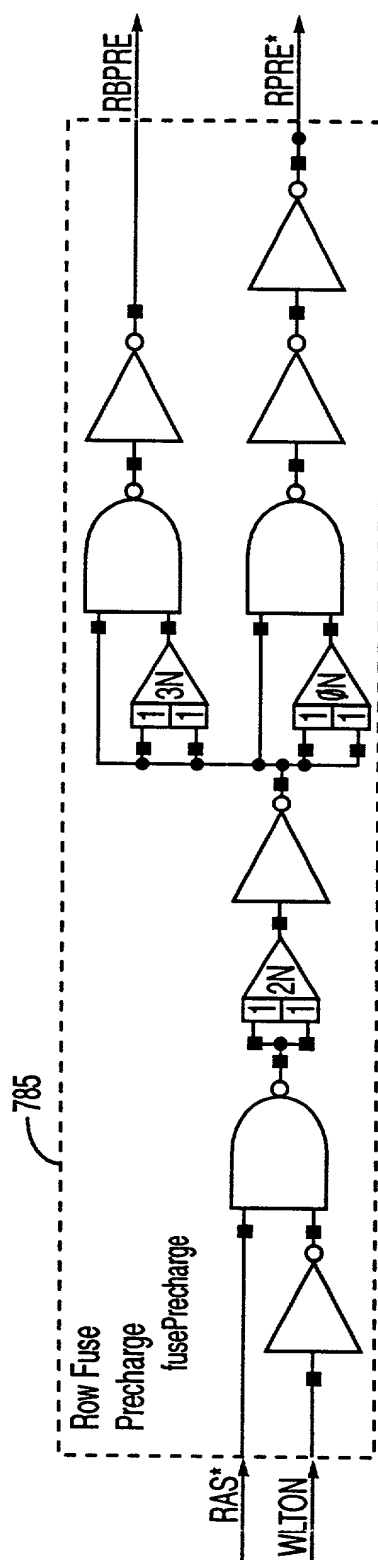


FIG. 47I

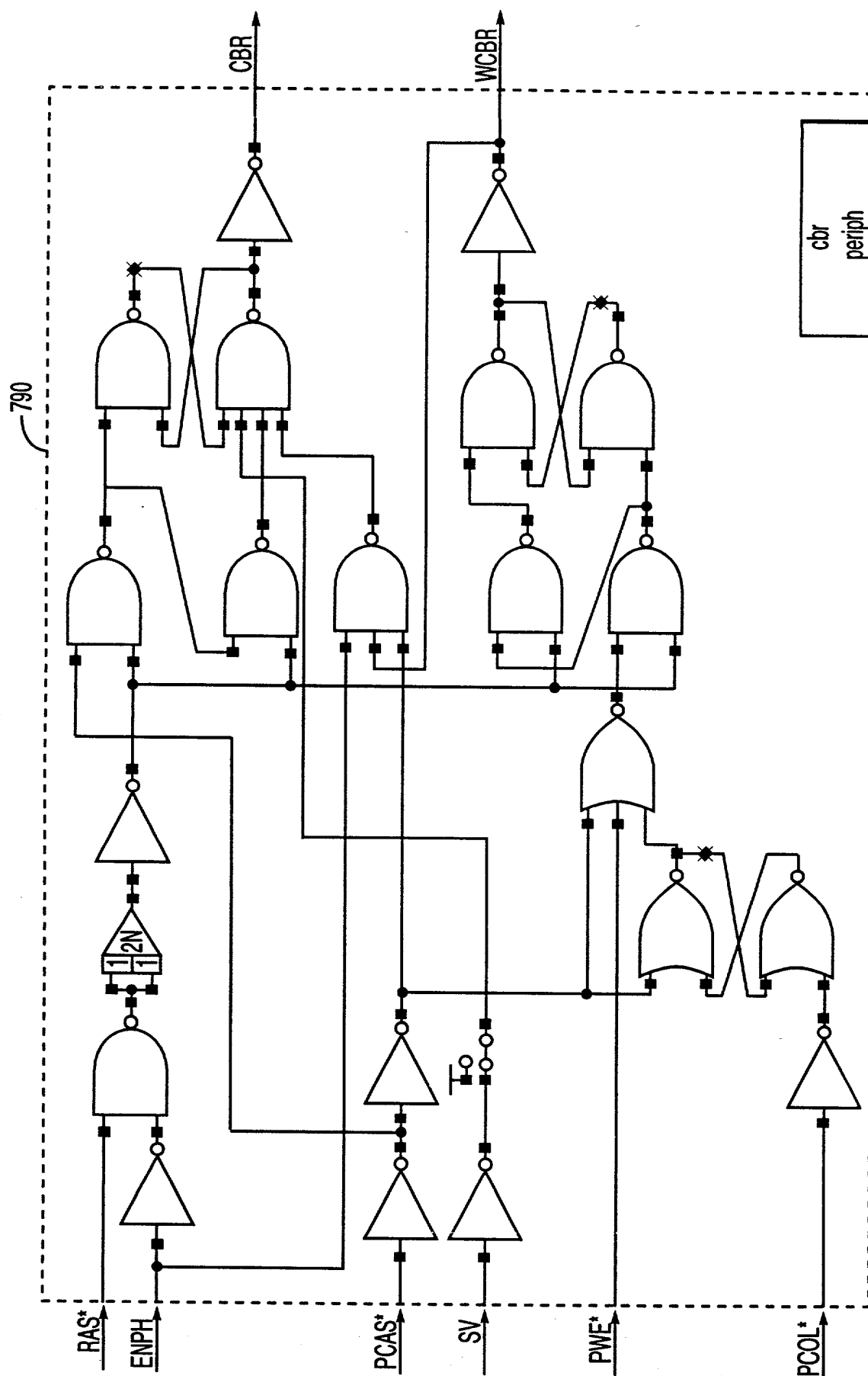


FIG. 47J

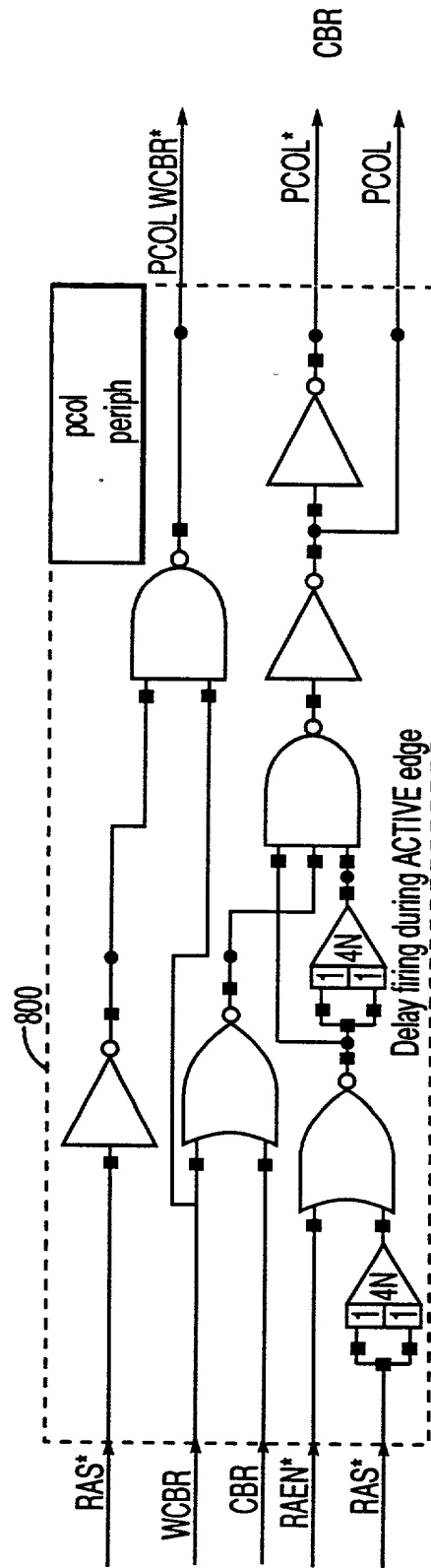


FIG. 47K

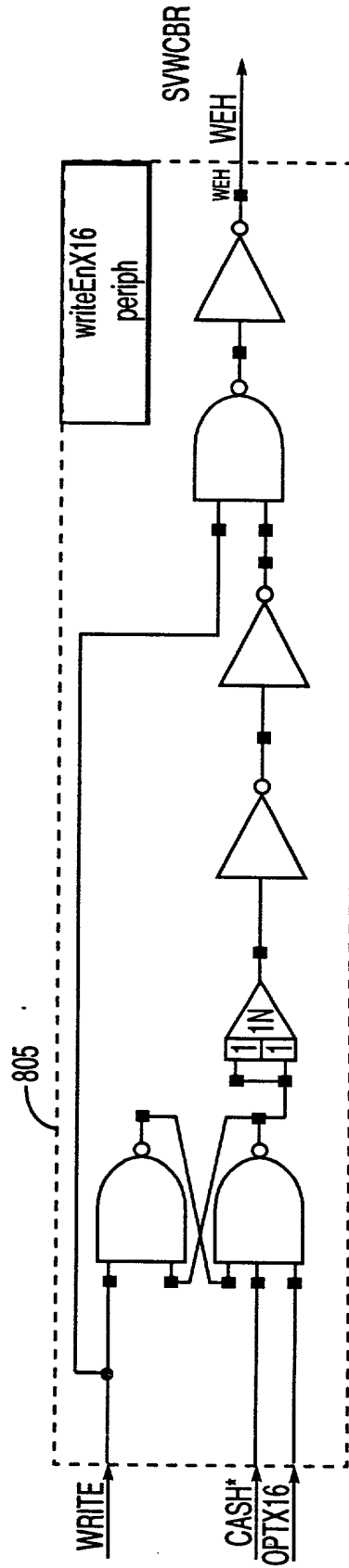


FIG. 47L

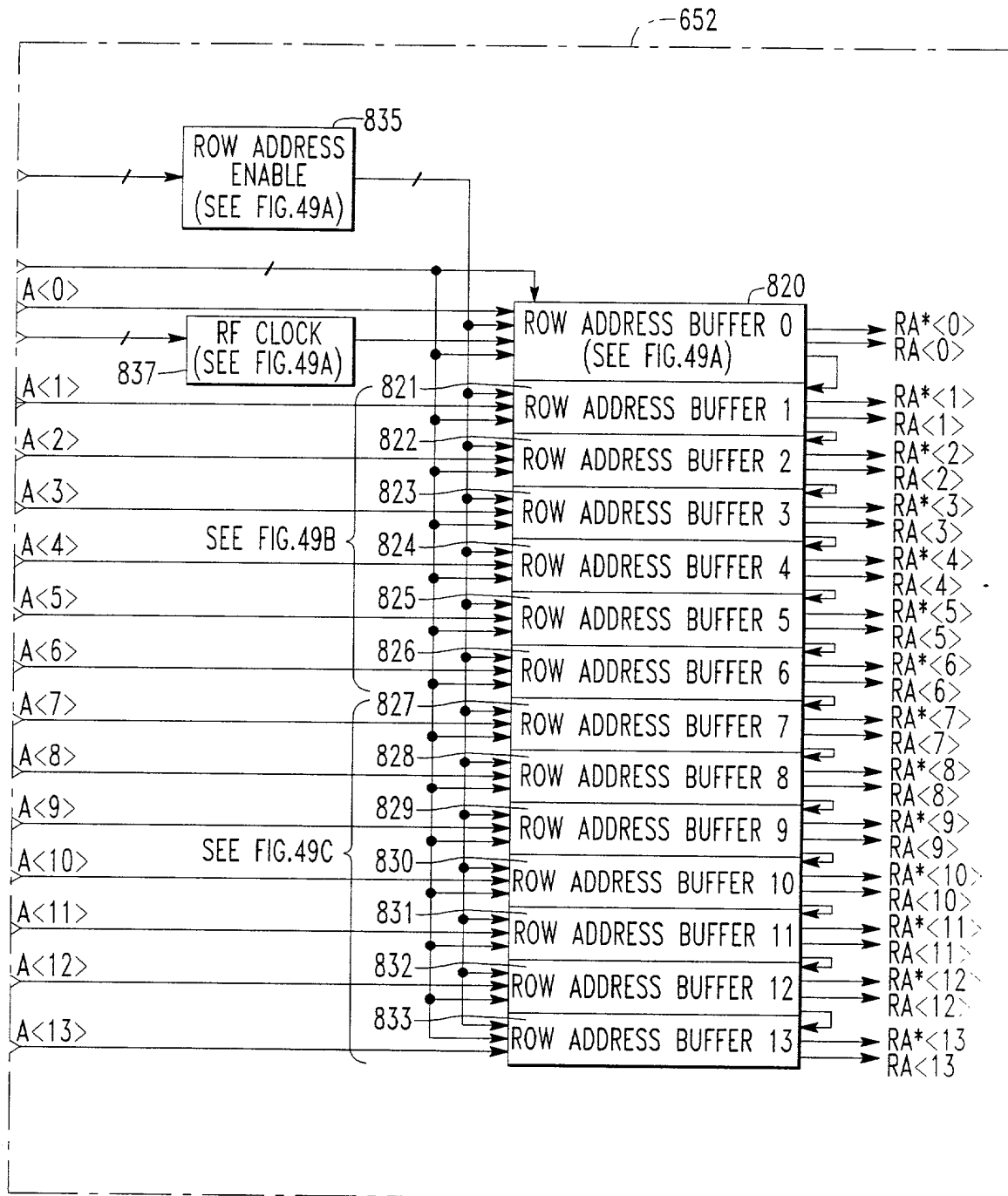


FIG. 48A

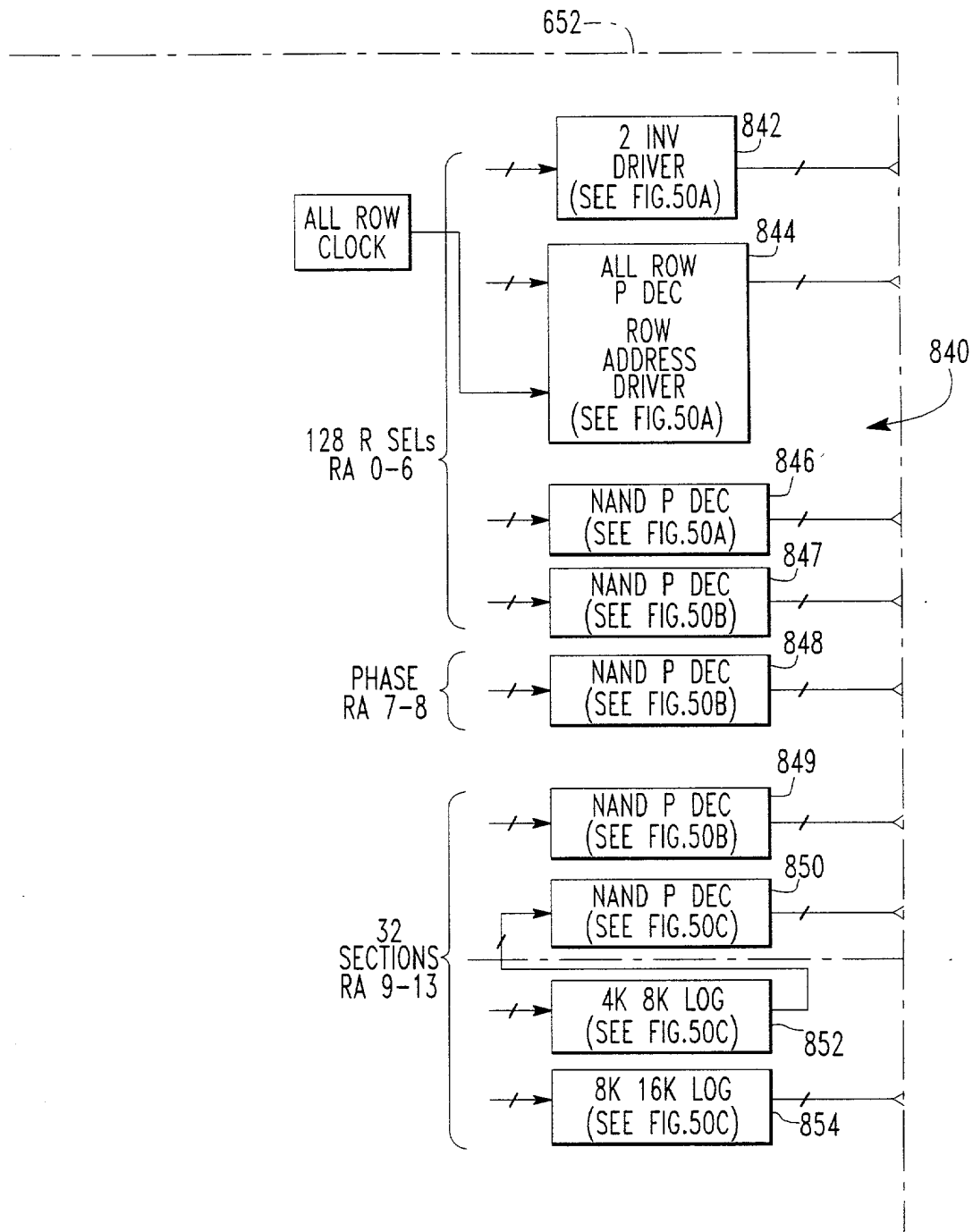
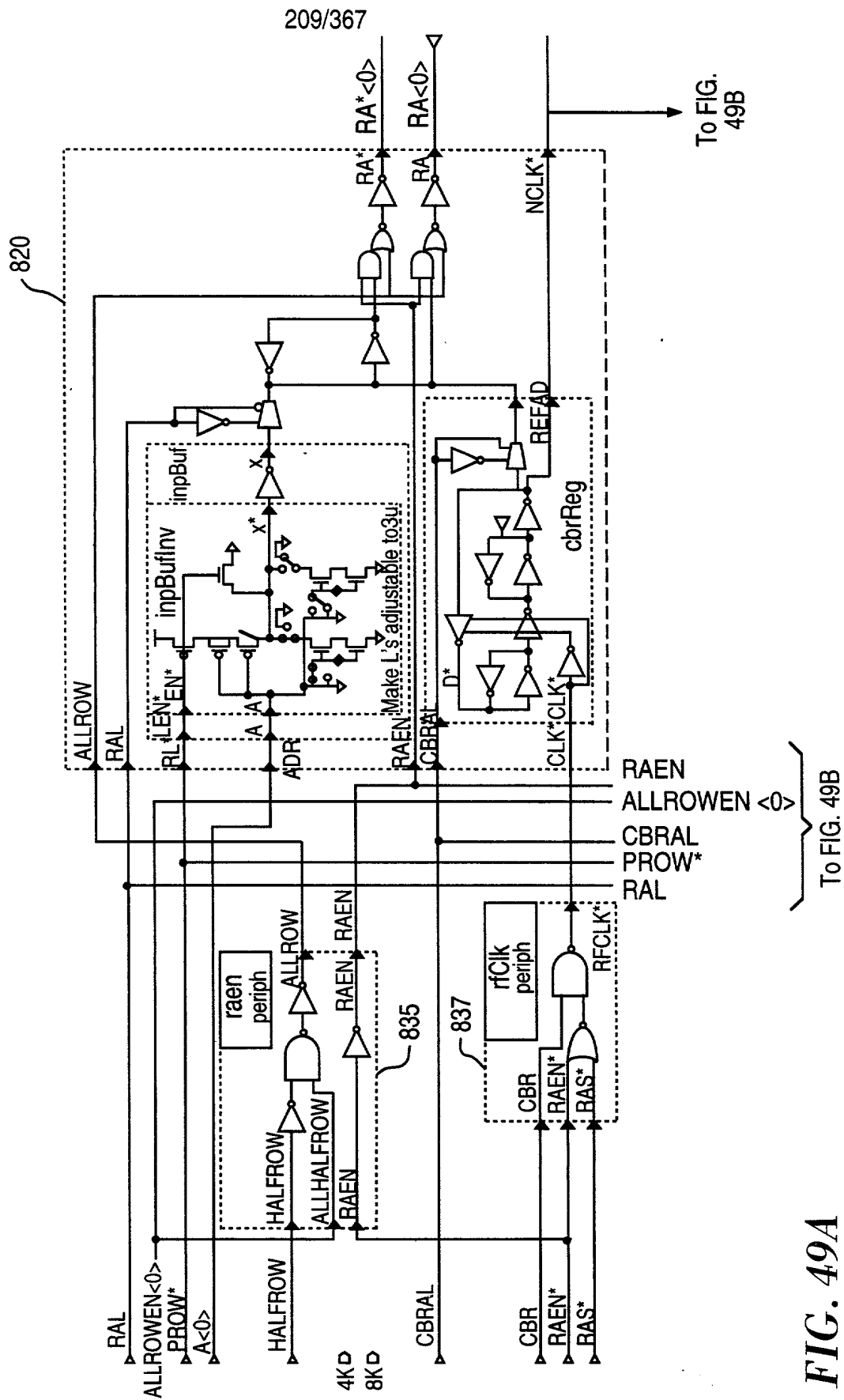
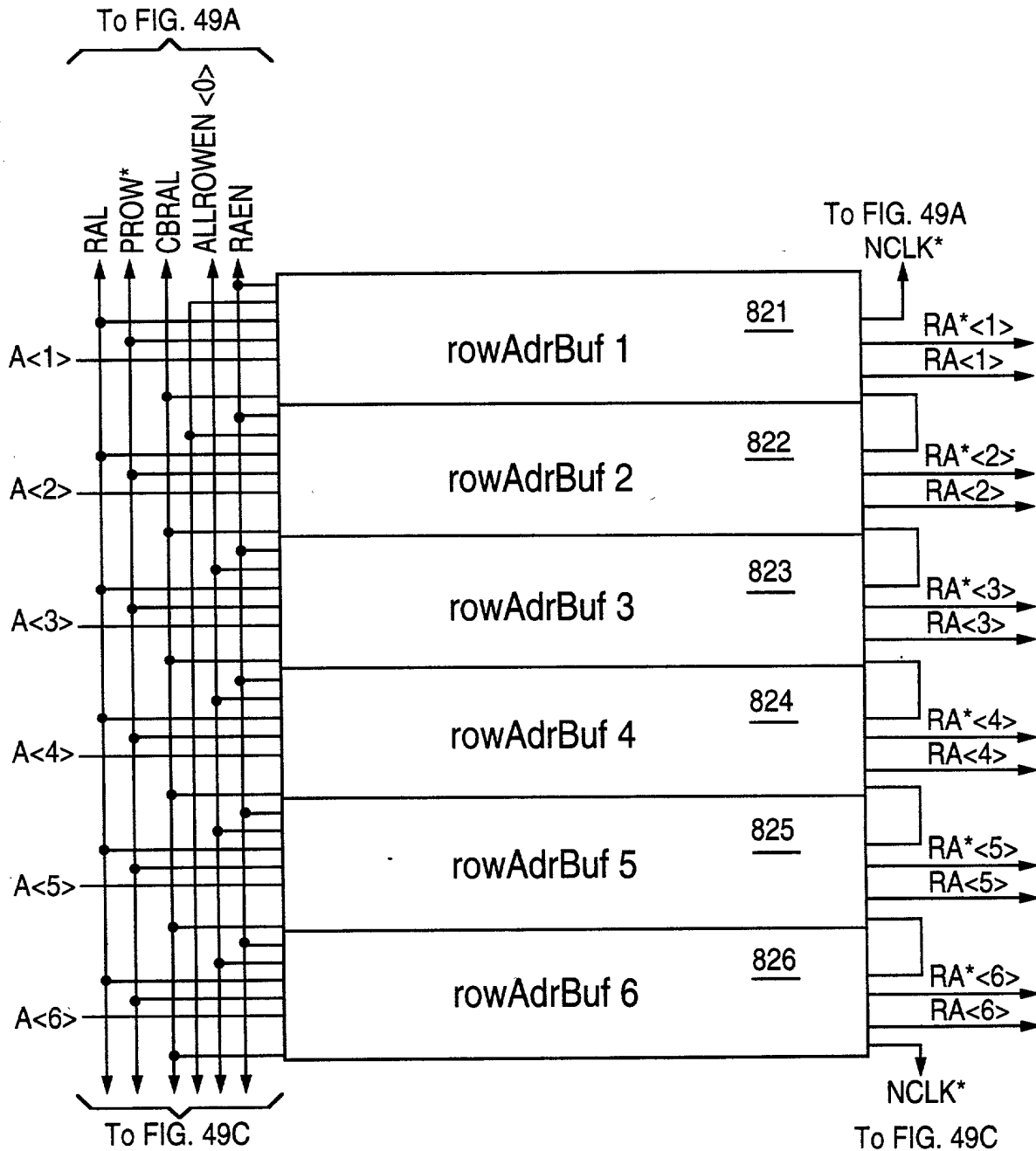
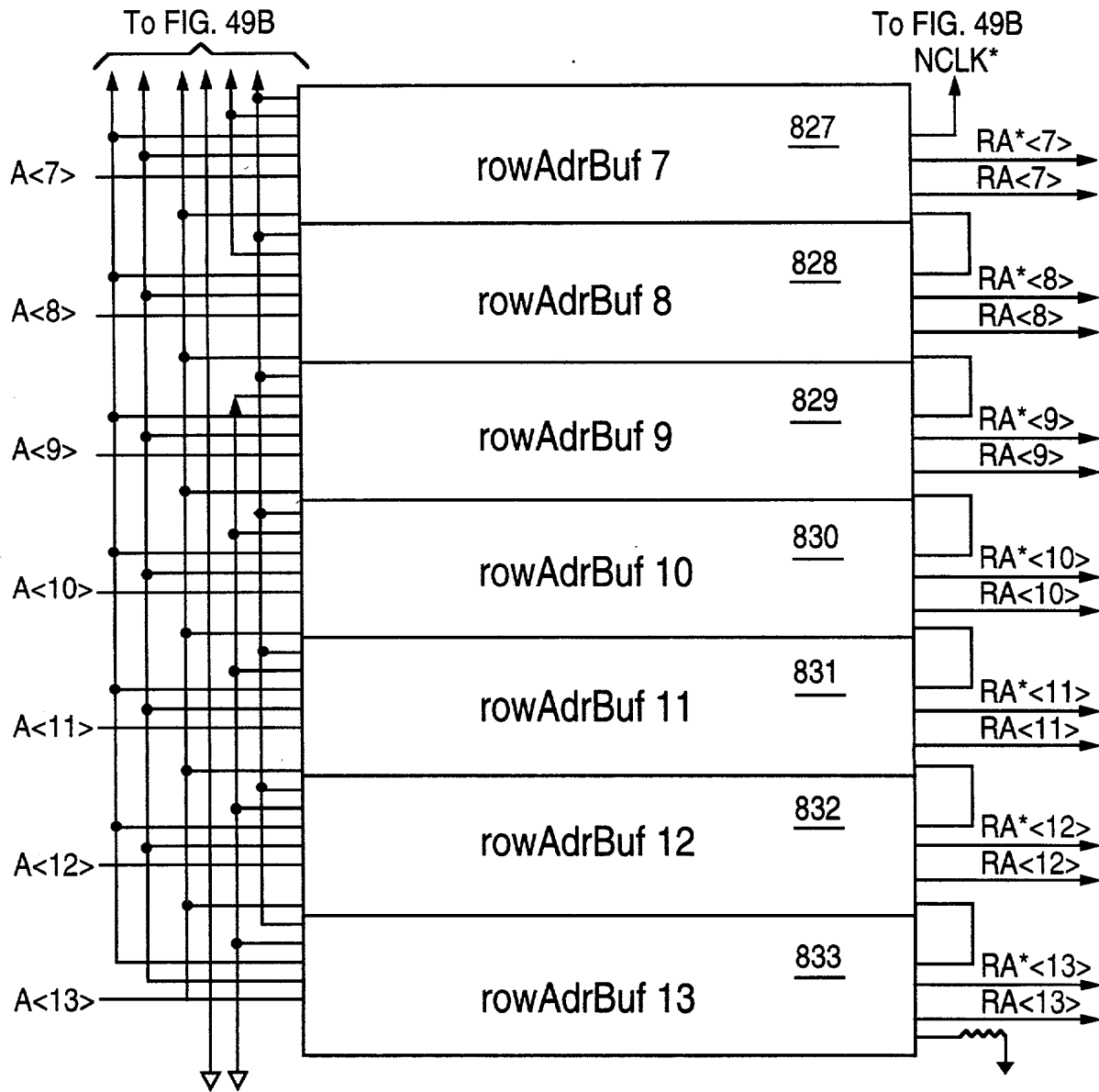


FIG. 48B



**FIG. 49B**

**FIG. 49C**

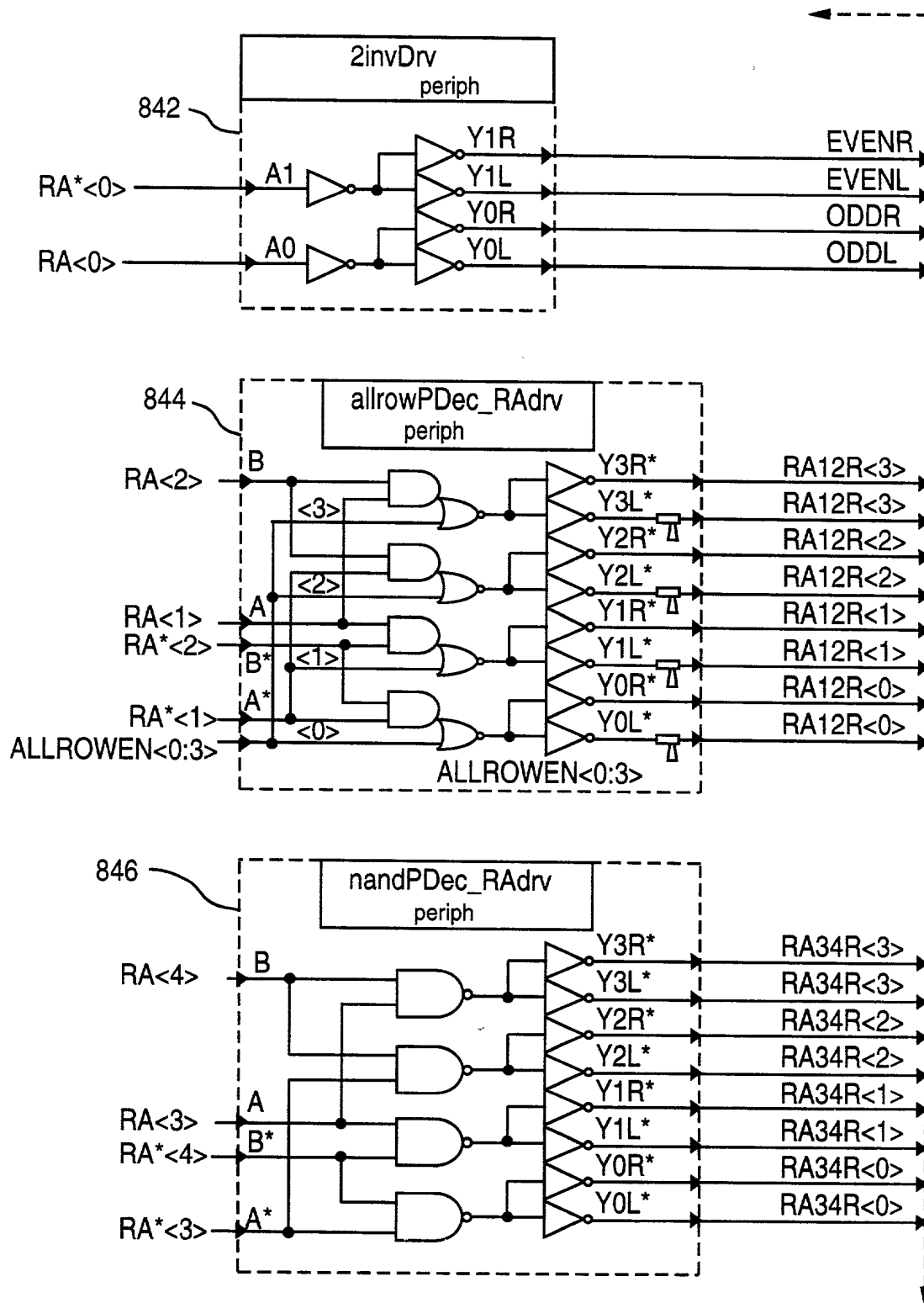
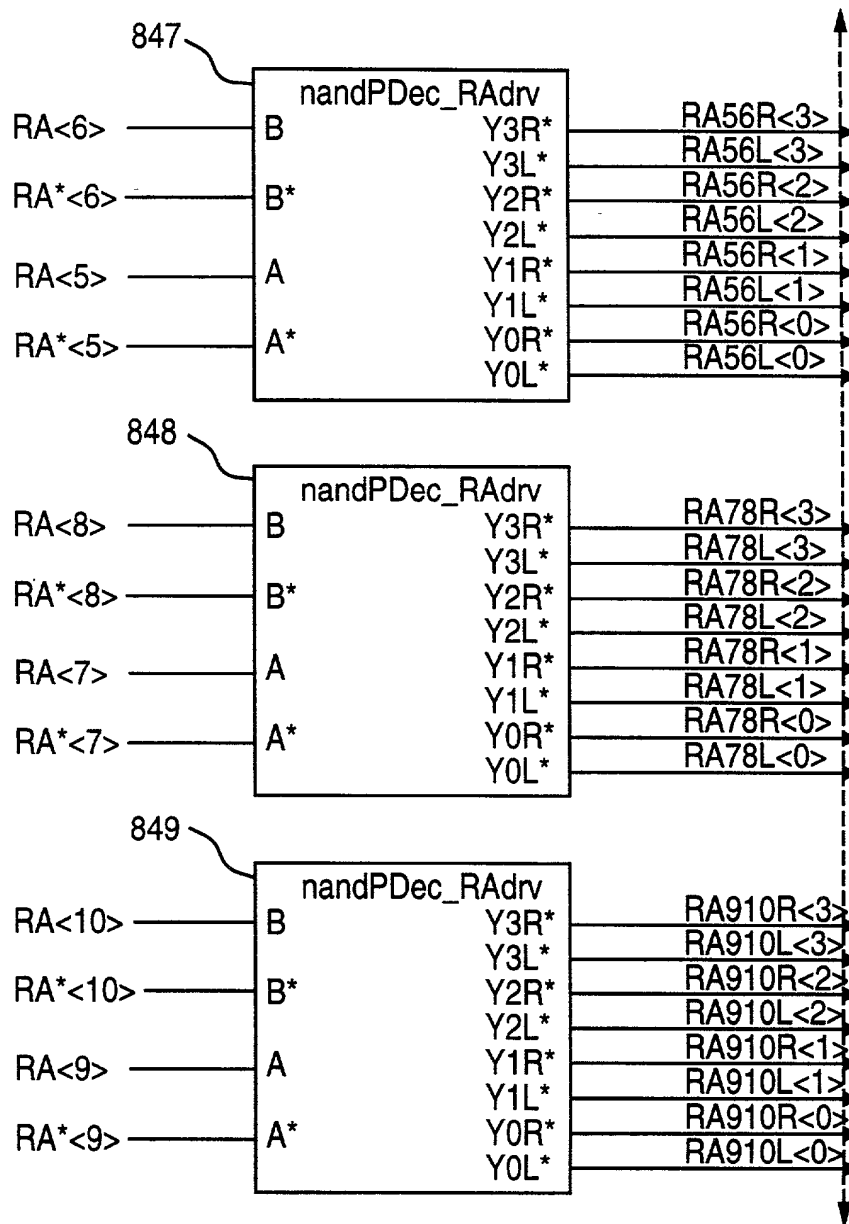


FIG. 50A

**FIG. 50B**

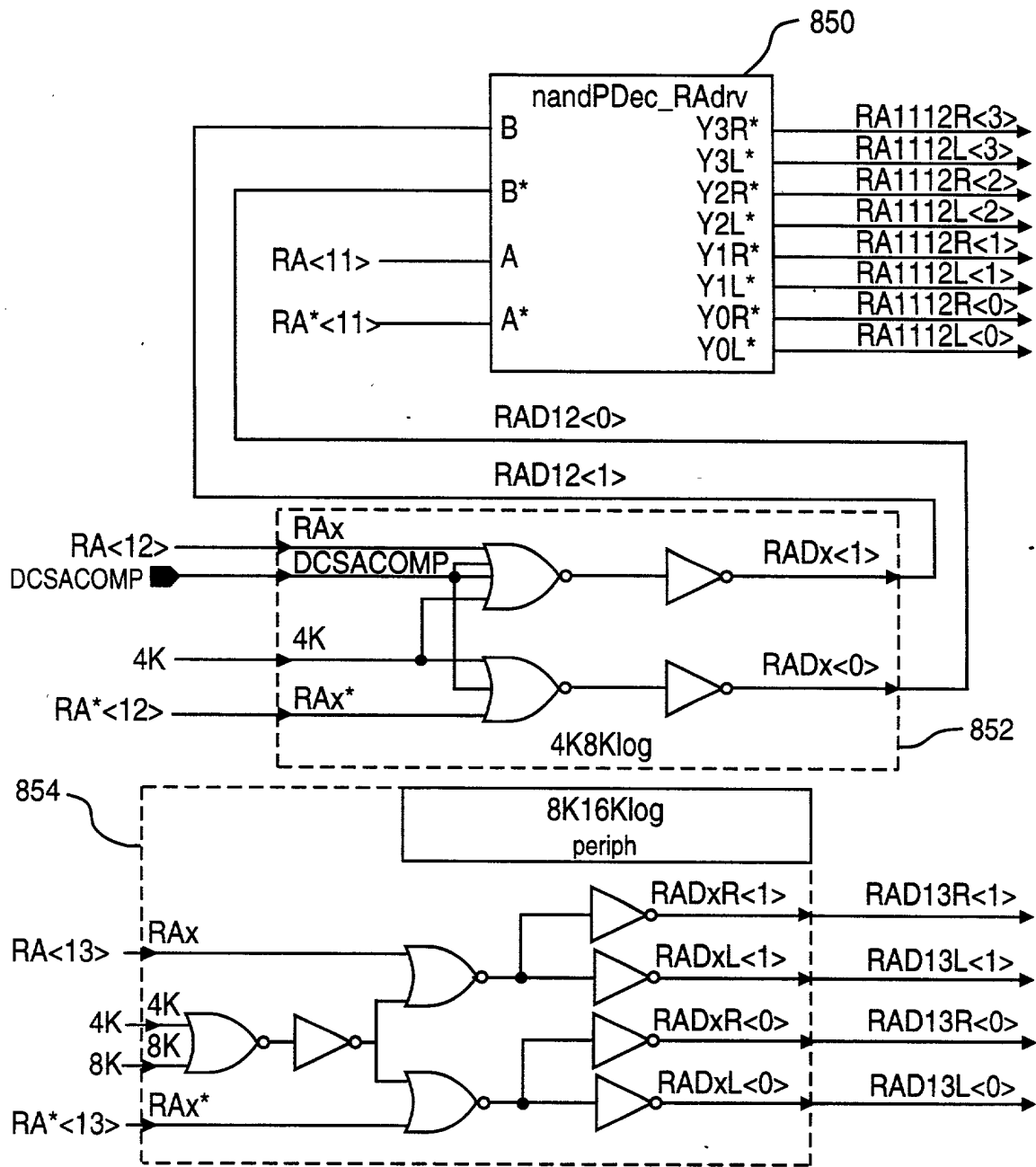


FIG. 50C

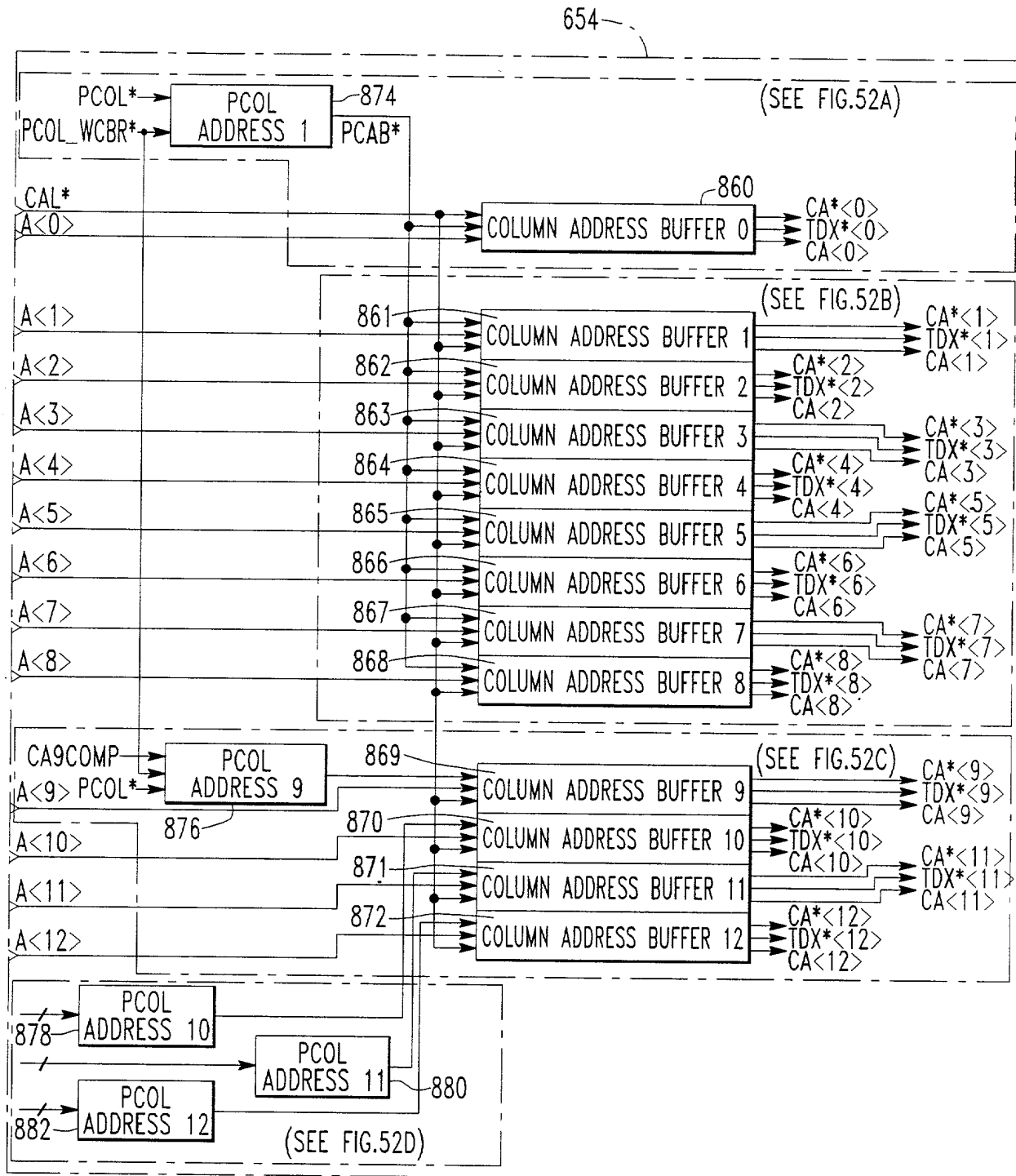


FIG. 51A

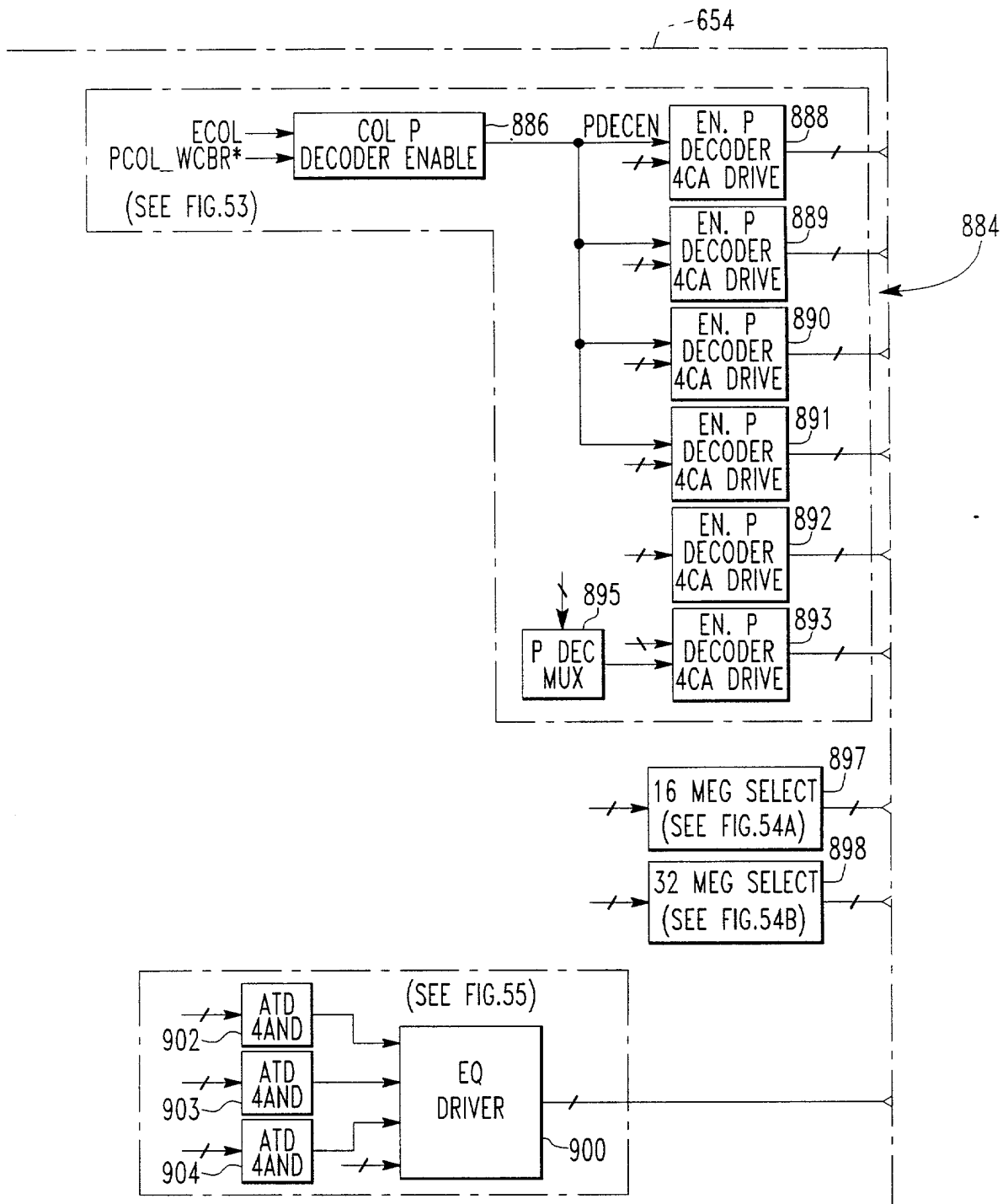
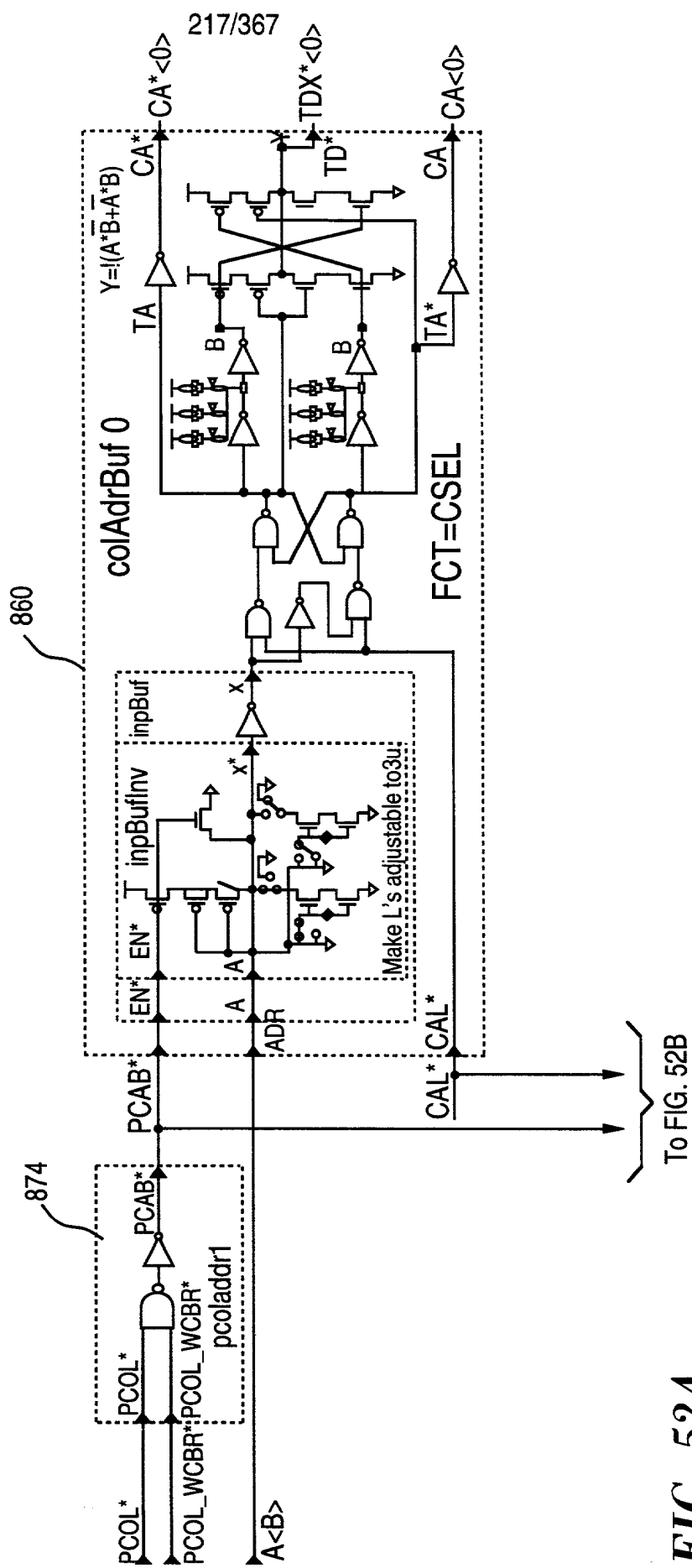


FIG. 51B



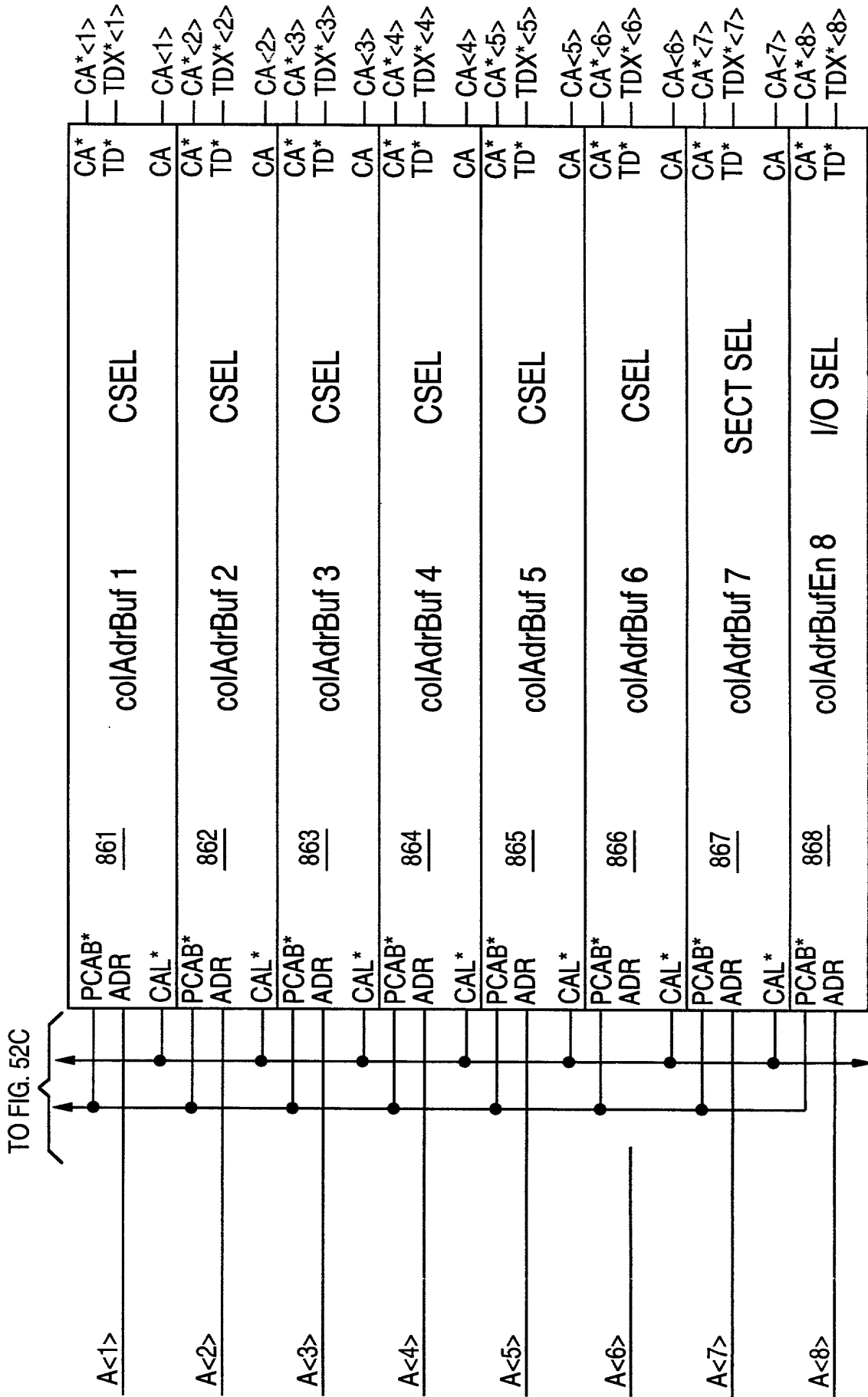


FIG. 52B

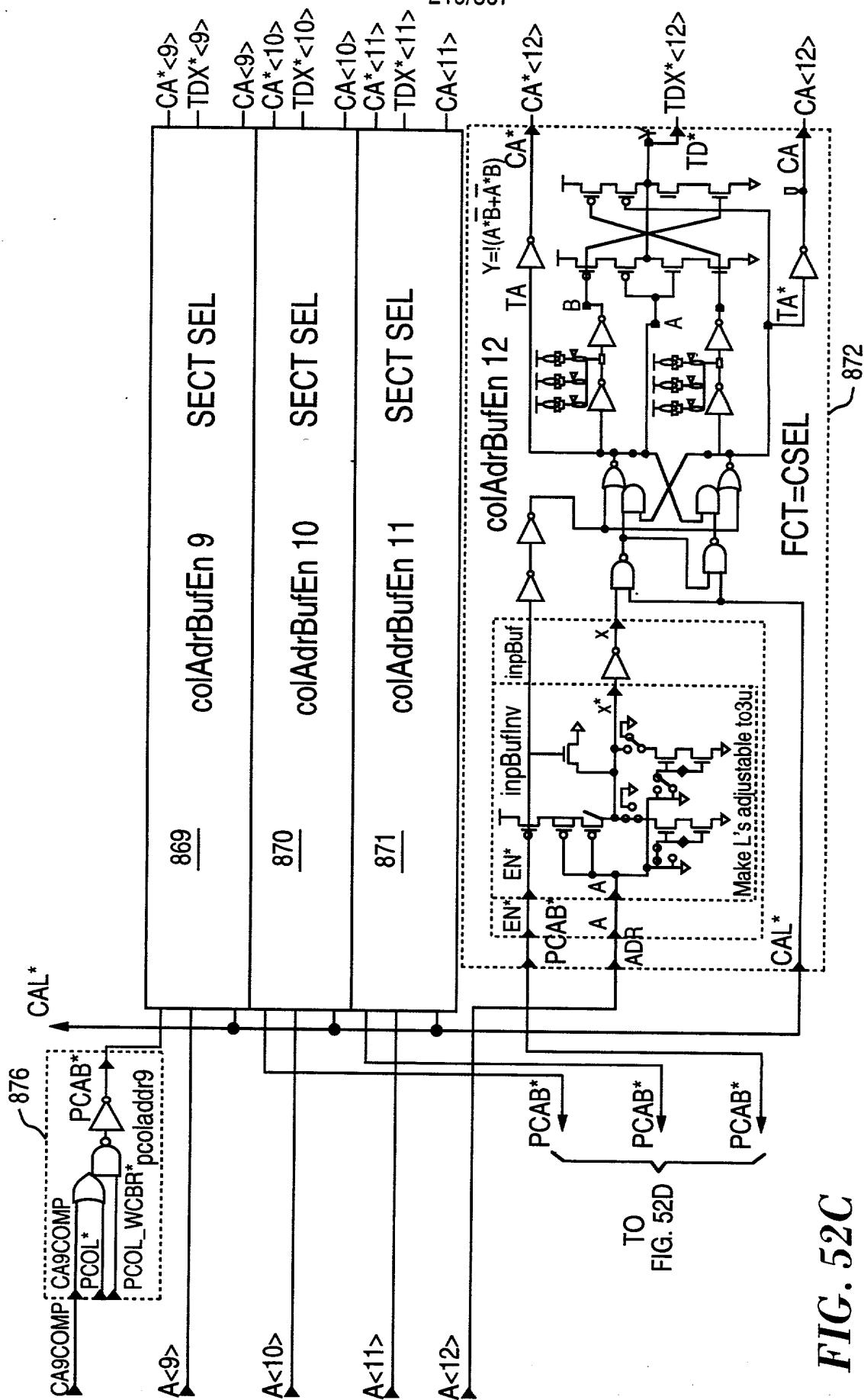


FIG. 52C

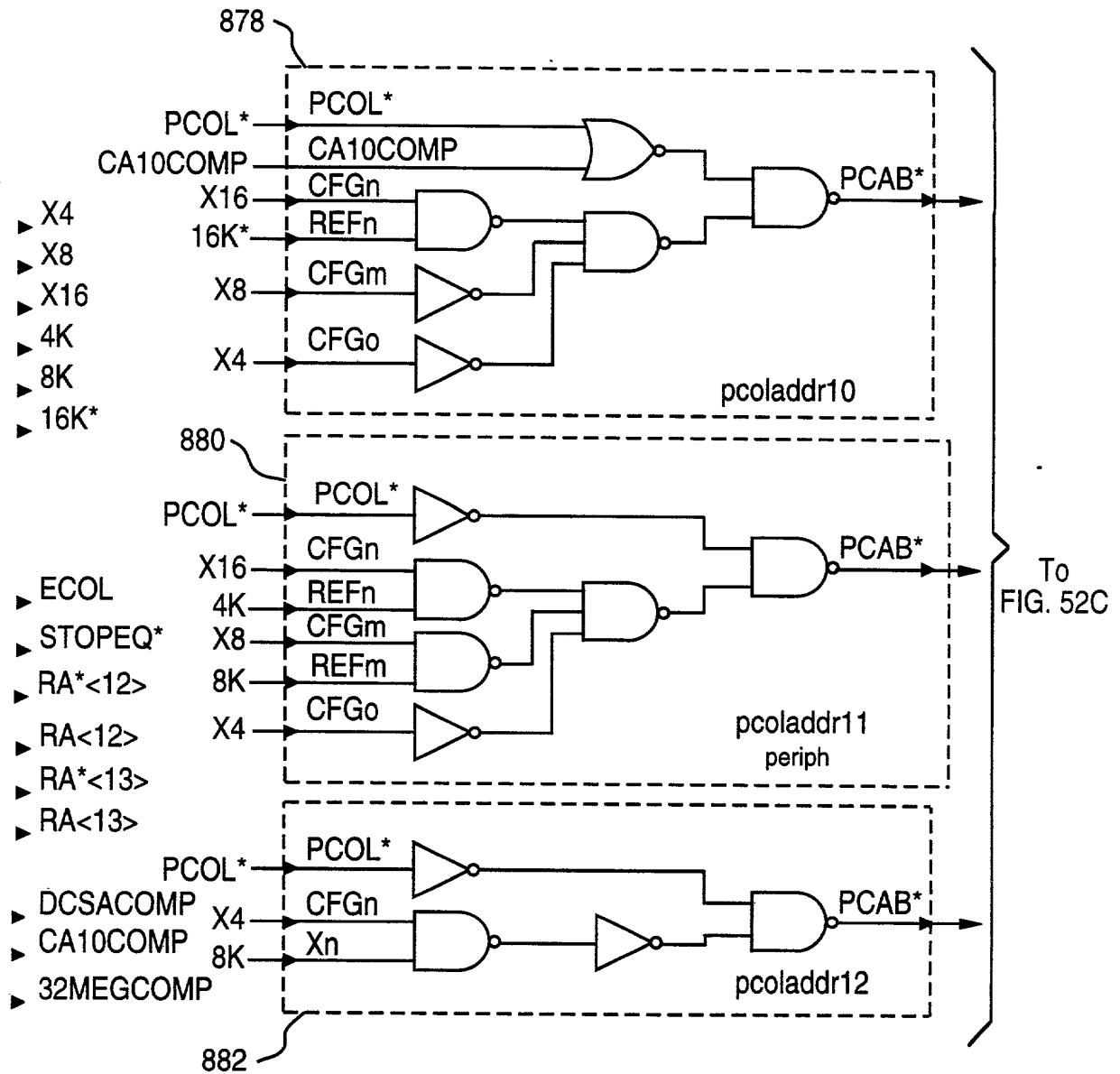
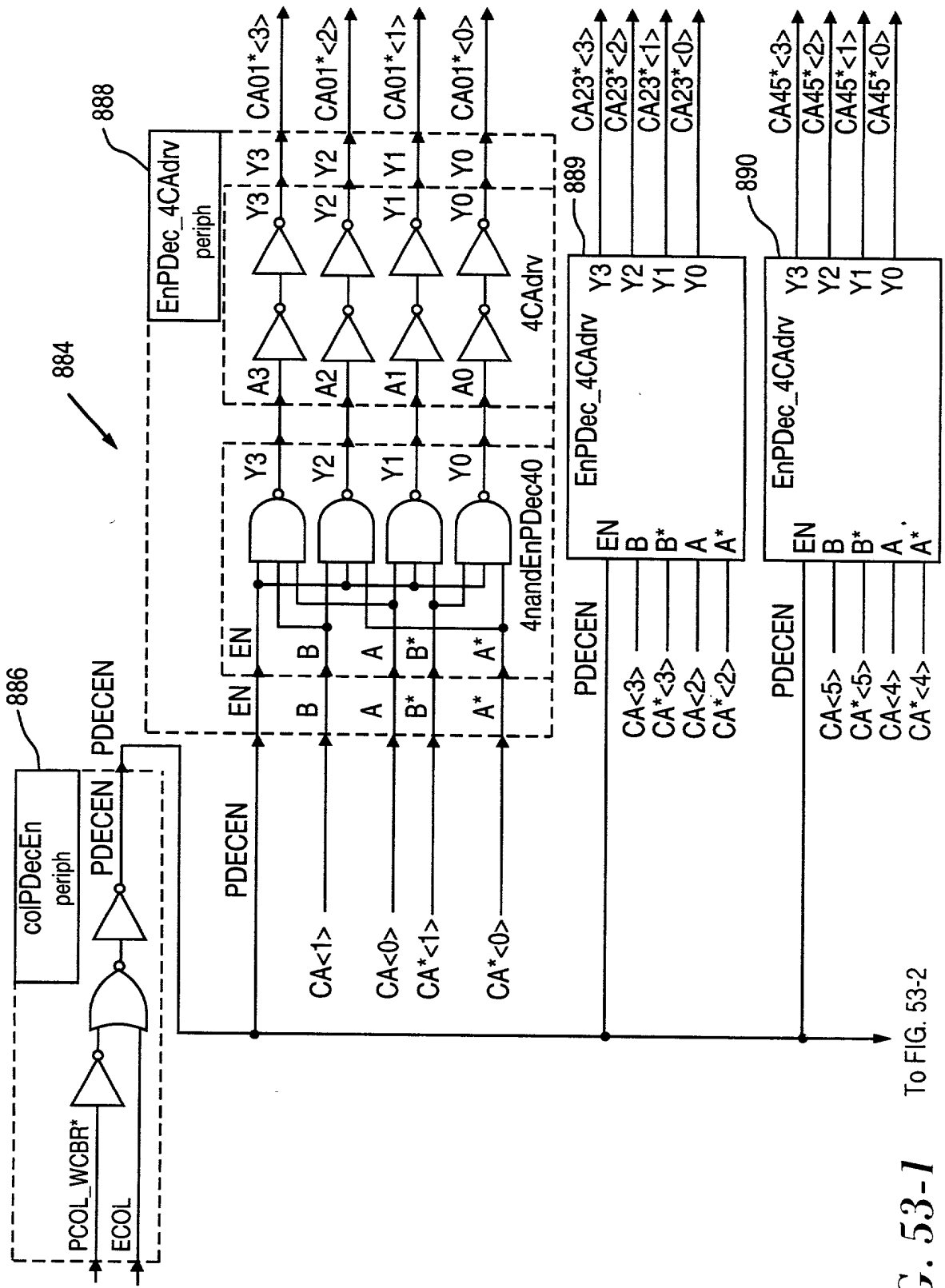


FIG. 52D



To FIG. 53-2

FIG. 53-1

To FIG. 53-1

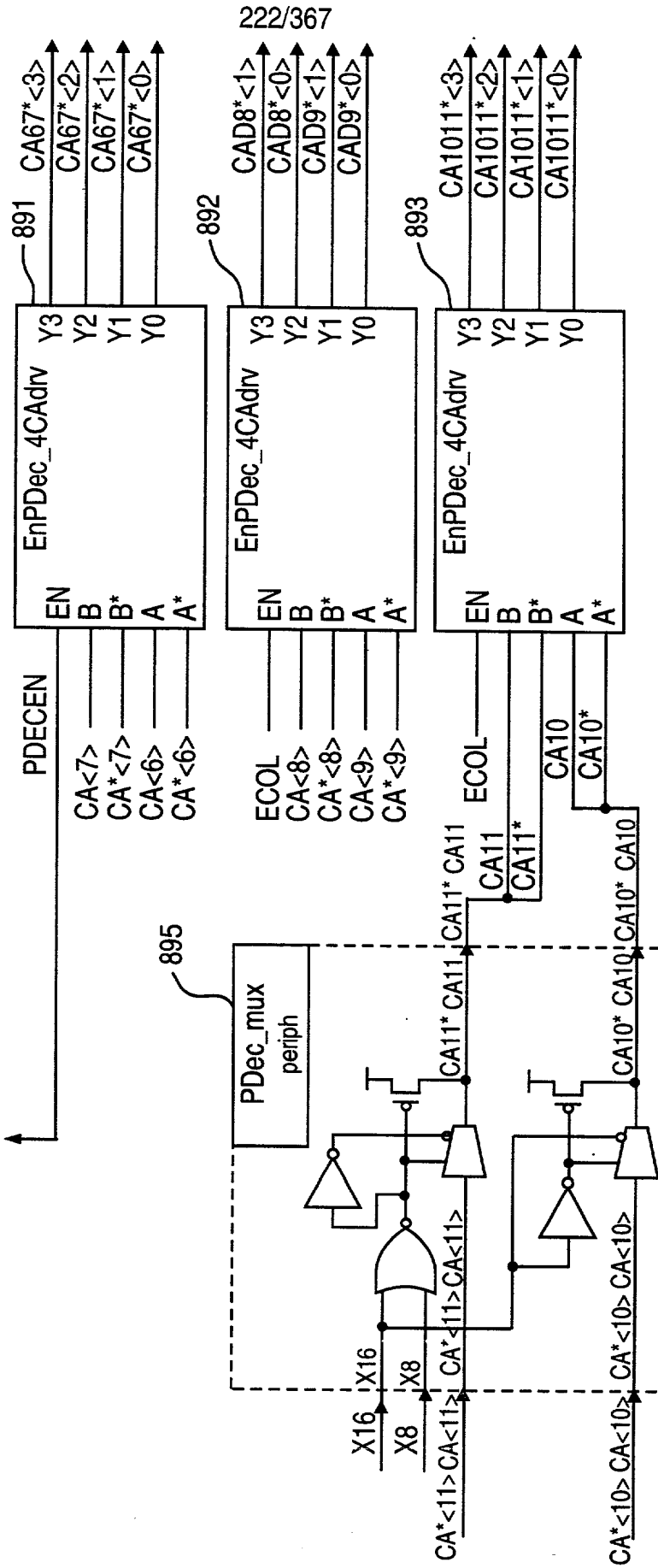


FIG. 53-2

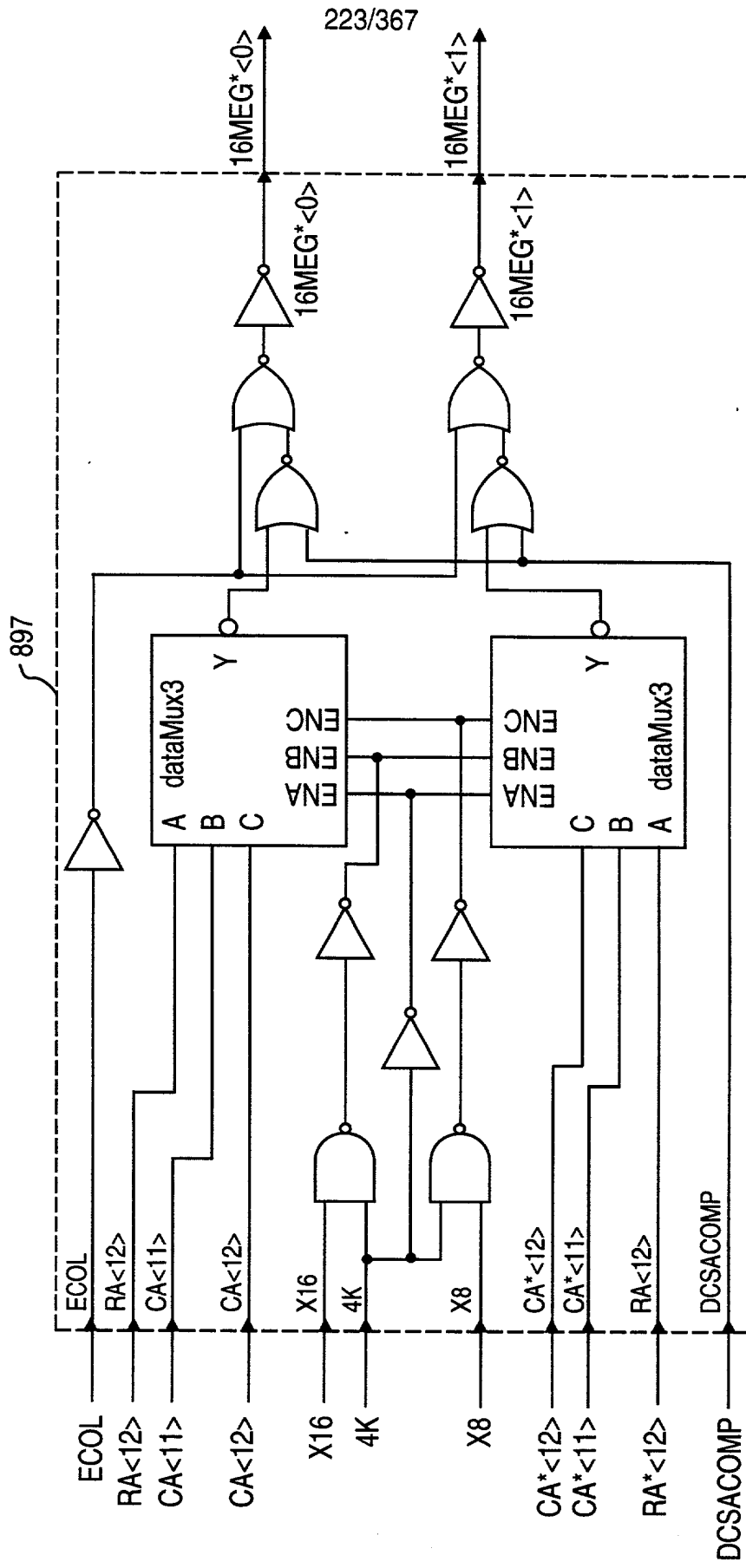


FIG. 54A

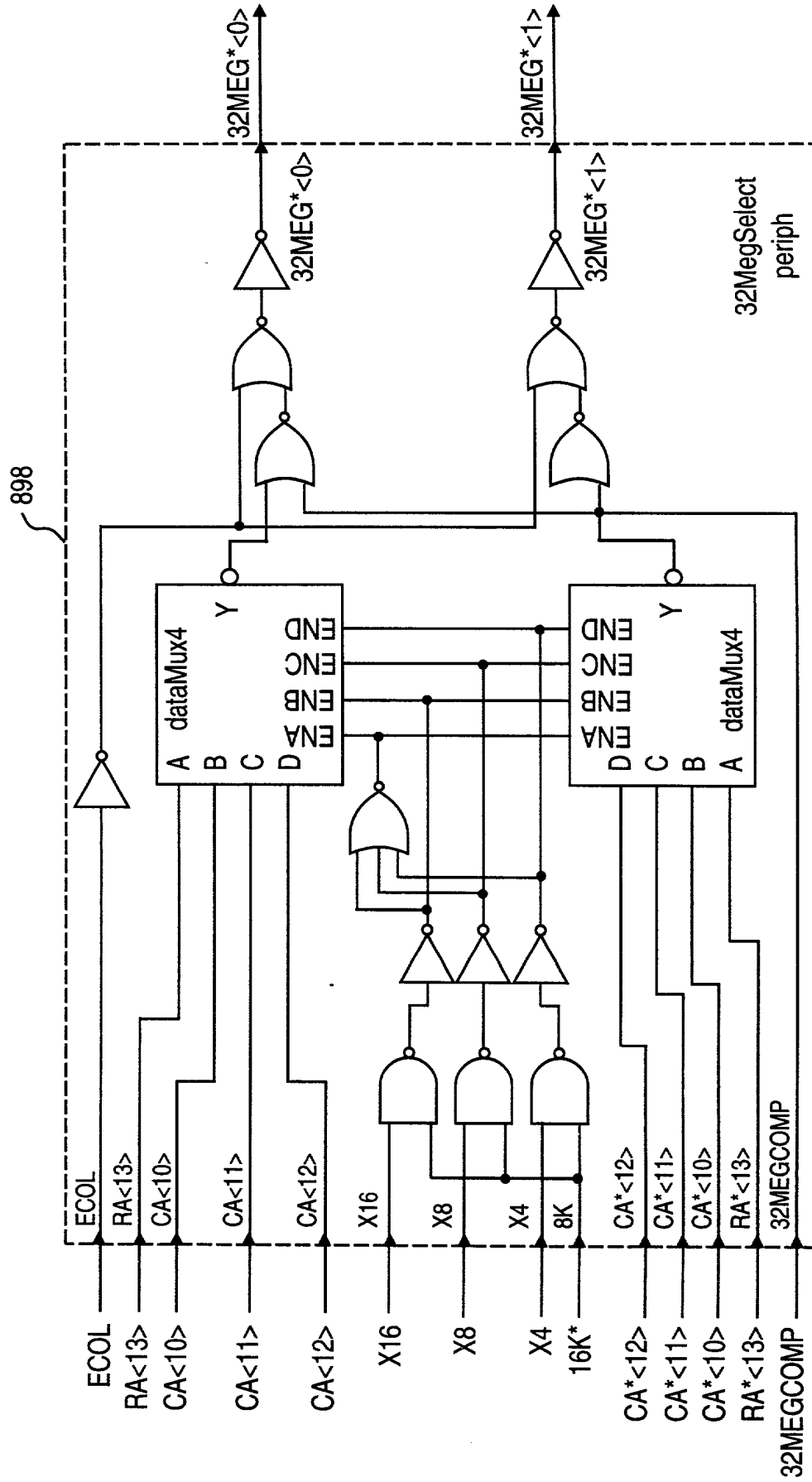


FIG. 54B

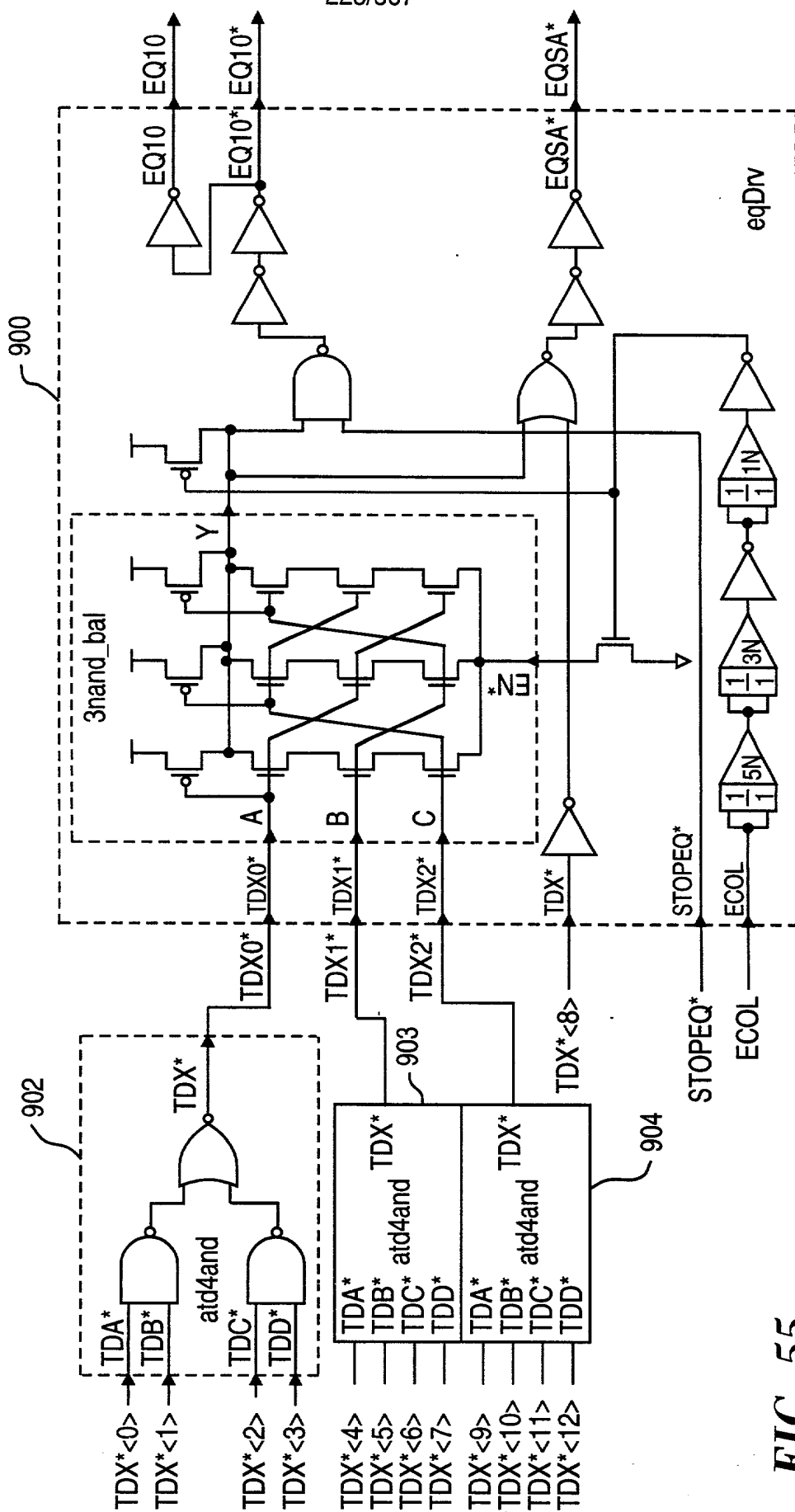


FIG. 55

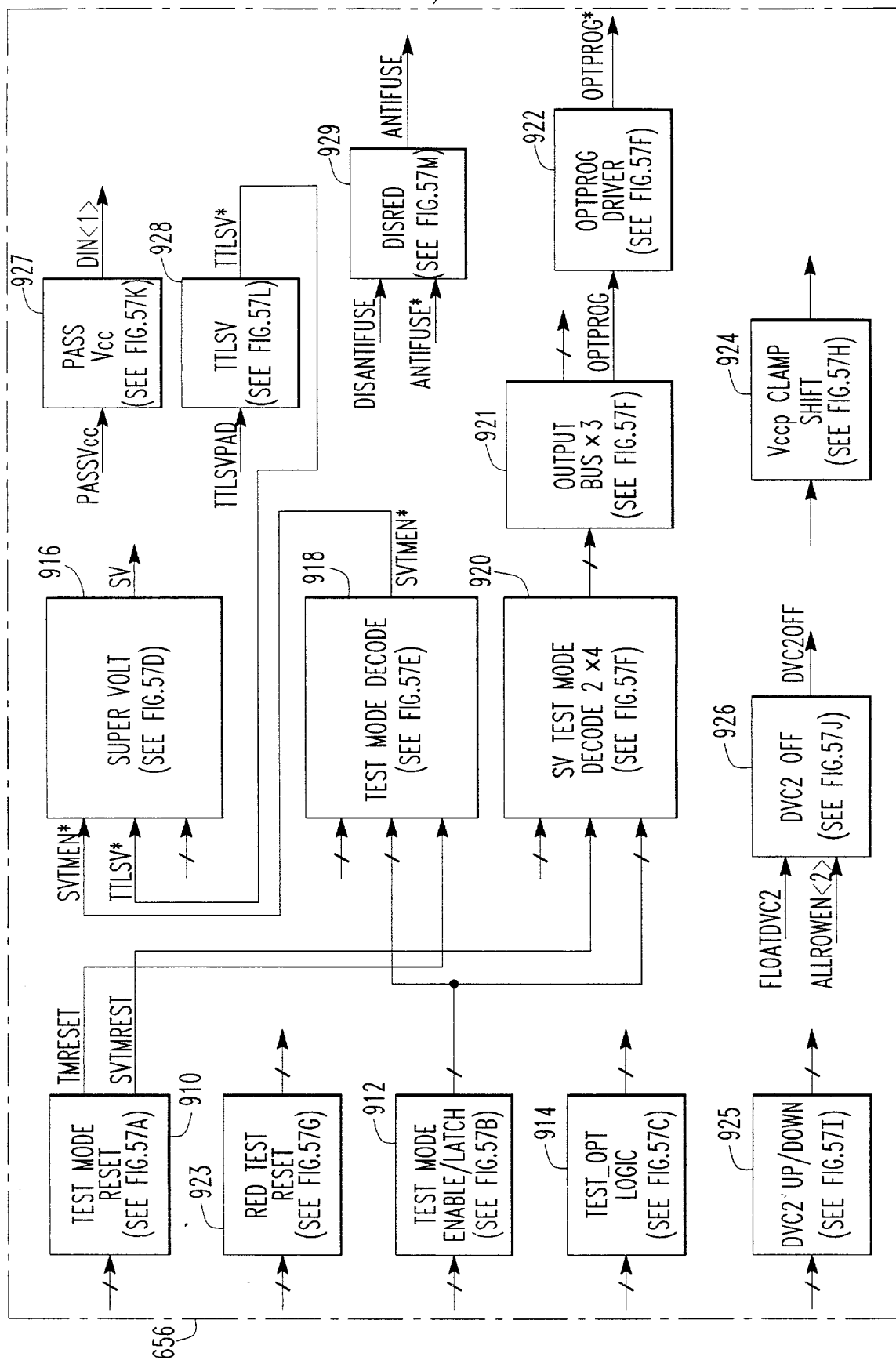


FIG. 56

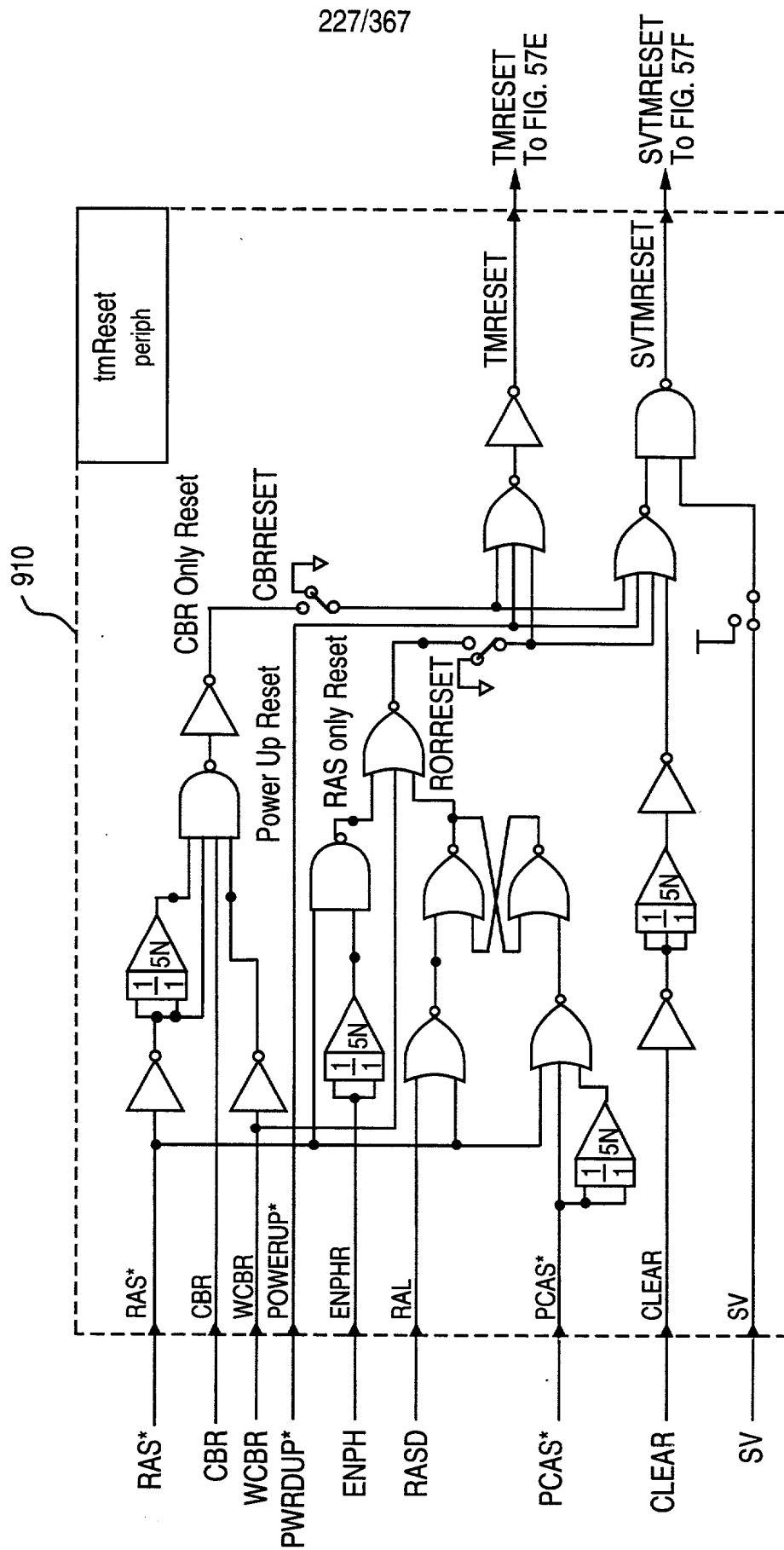


FIG. 57A

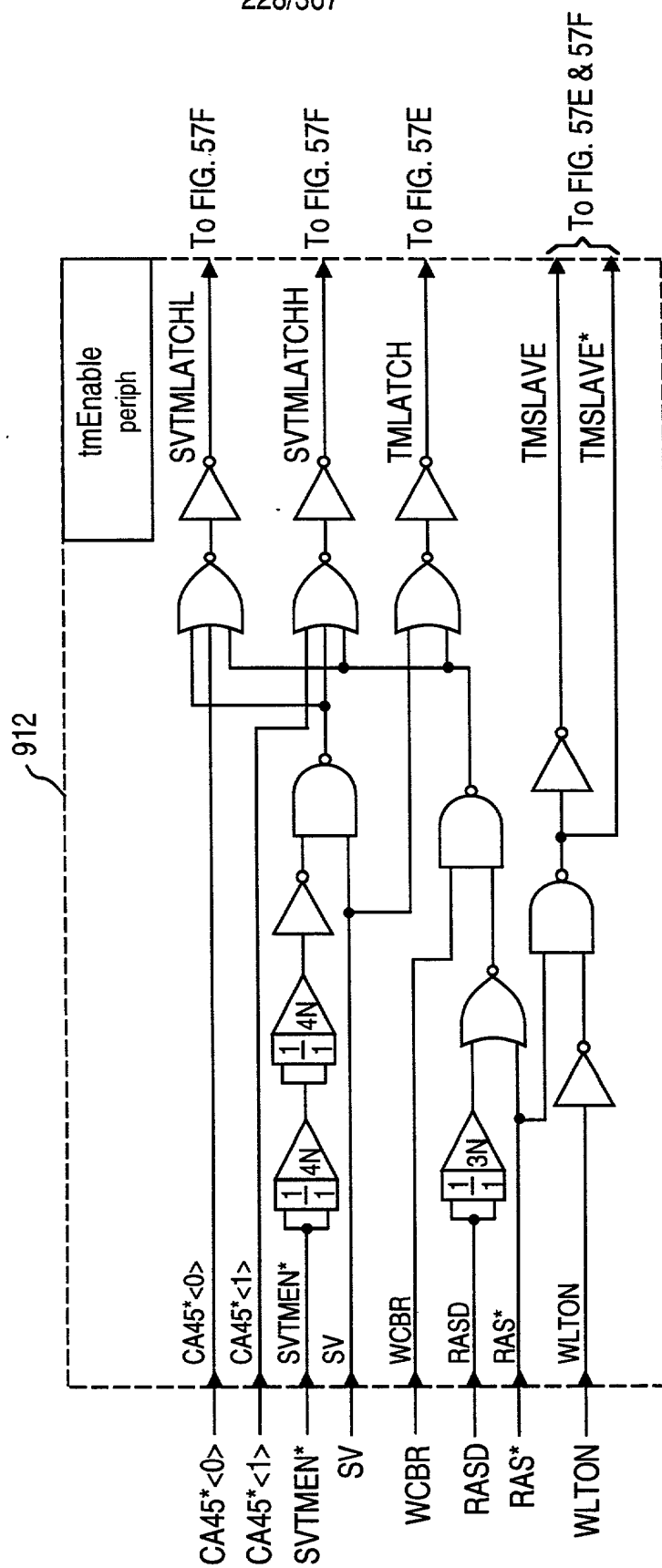


FIG. 57B

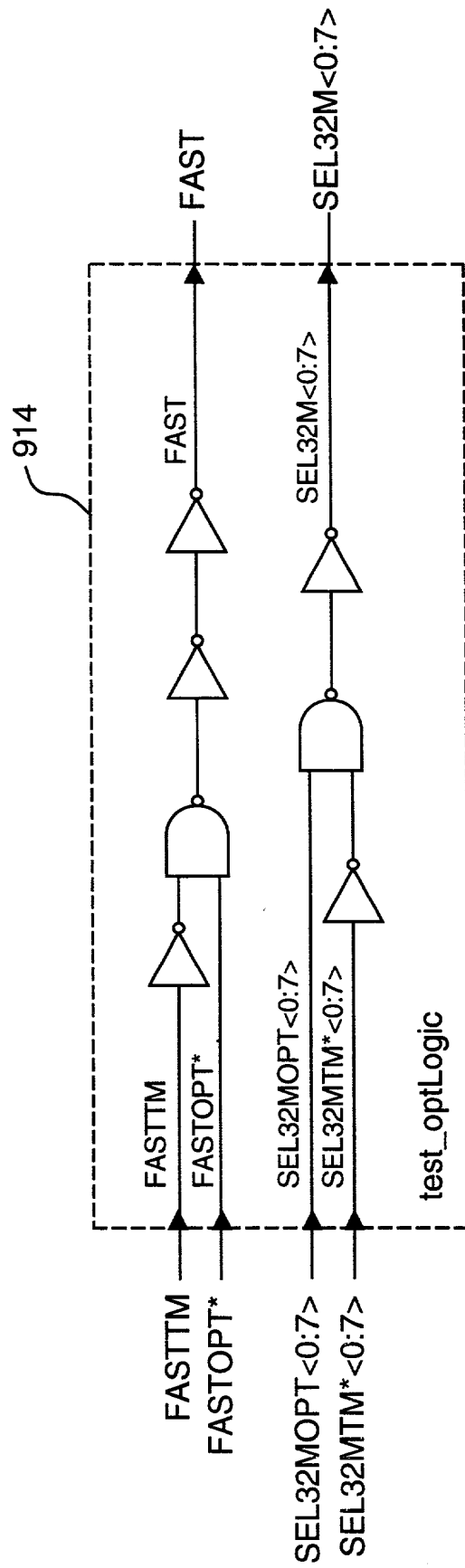
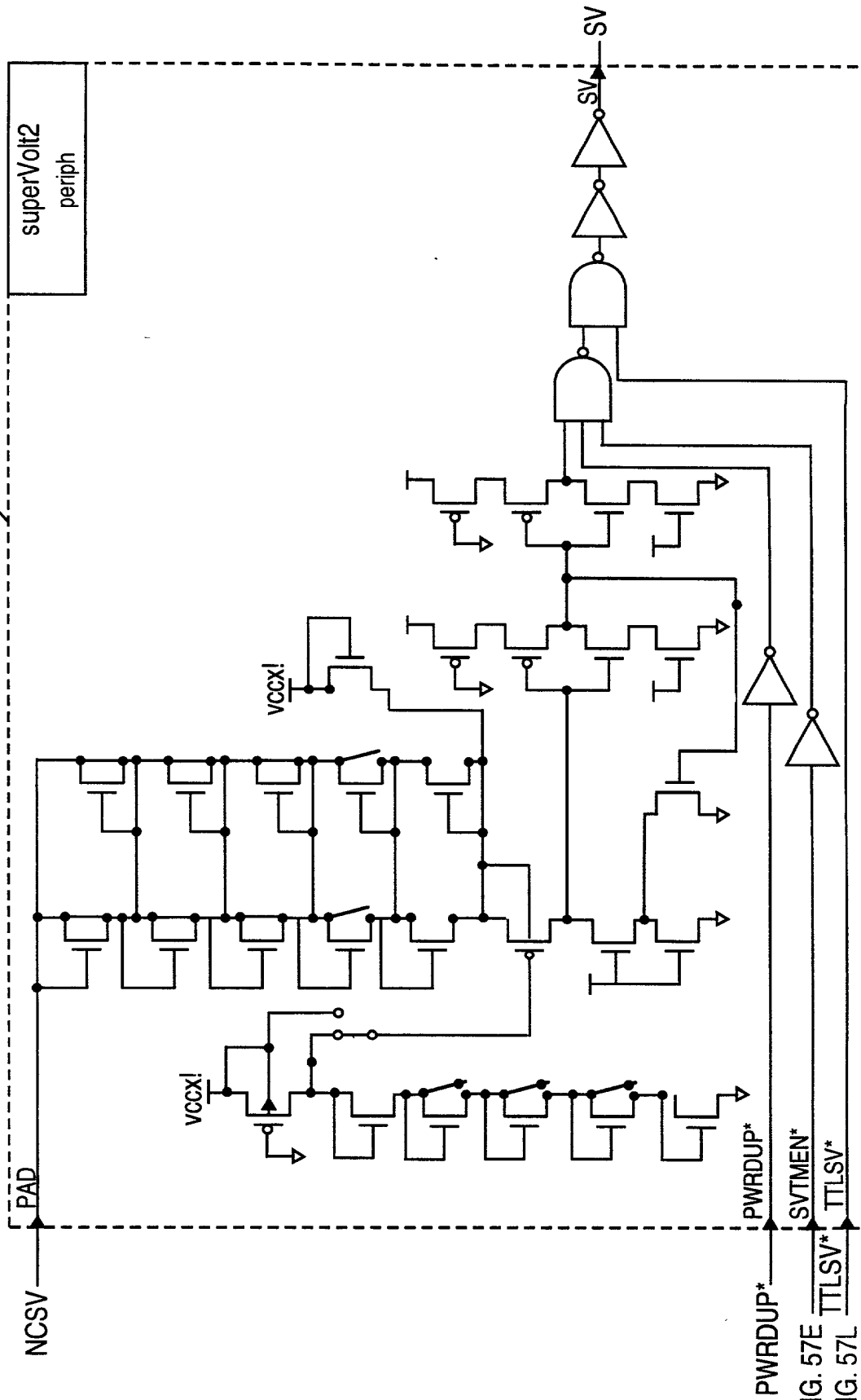


FIG. 57C

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From FIG. 57E
From FIG. 57L

FIG. 57D

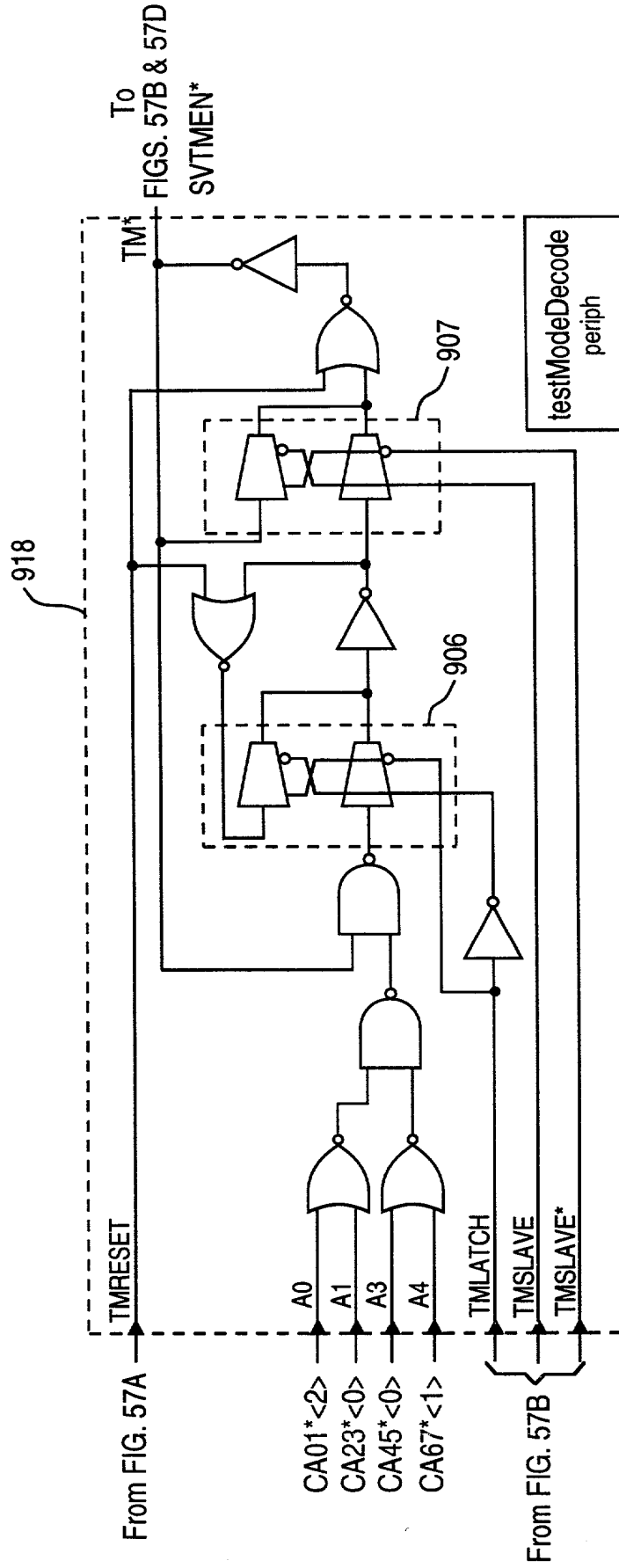


FIG. 57E

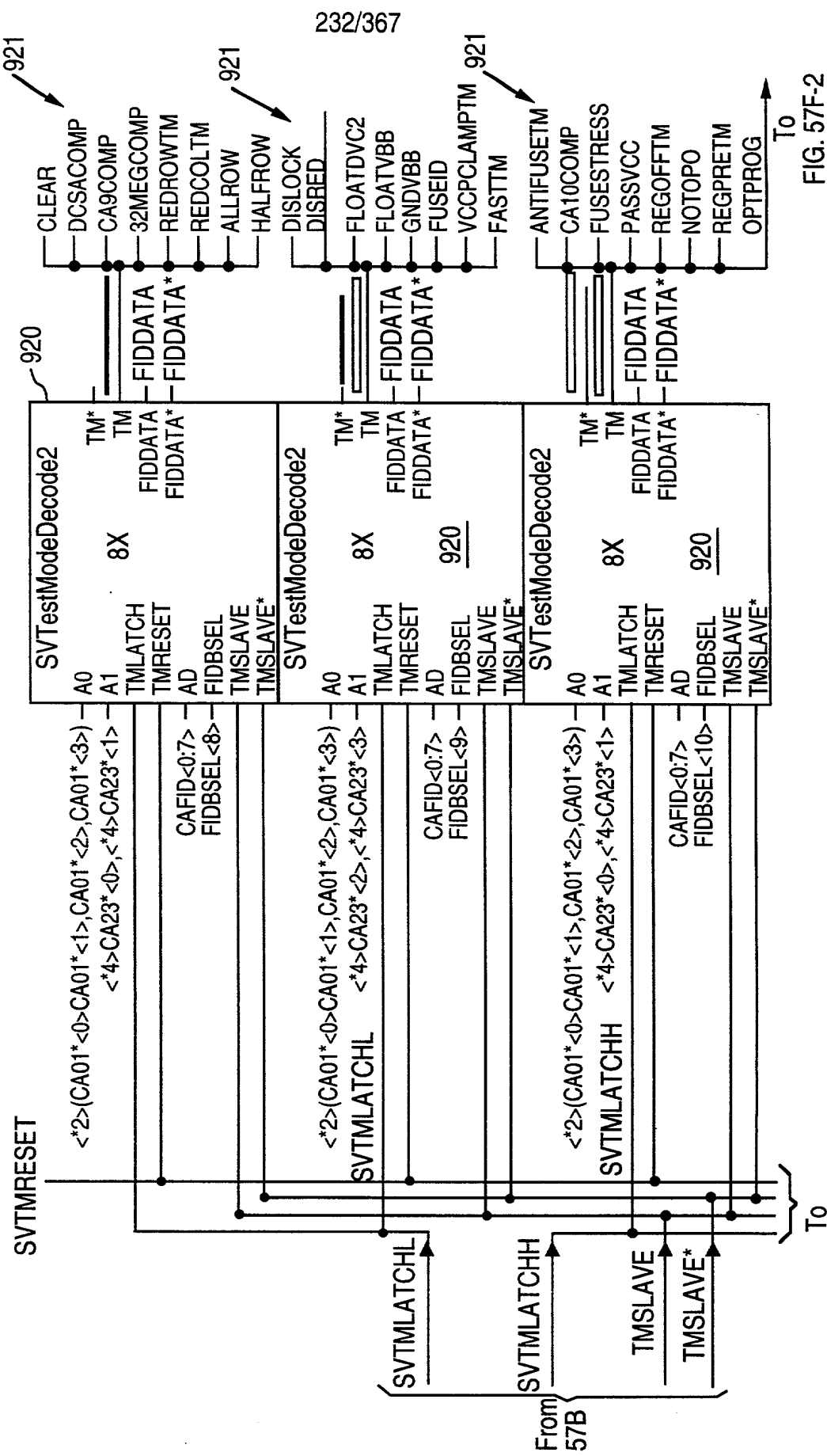


FIG. 57F-1

FIG. 57F-3

FIG. 57F-2

FIG. 57F-1

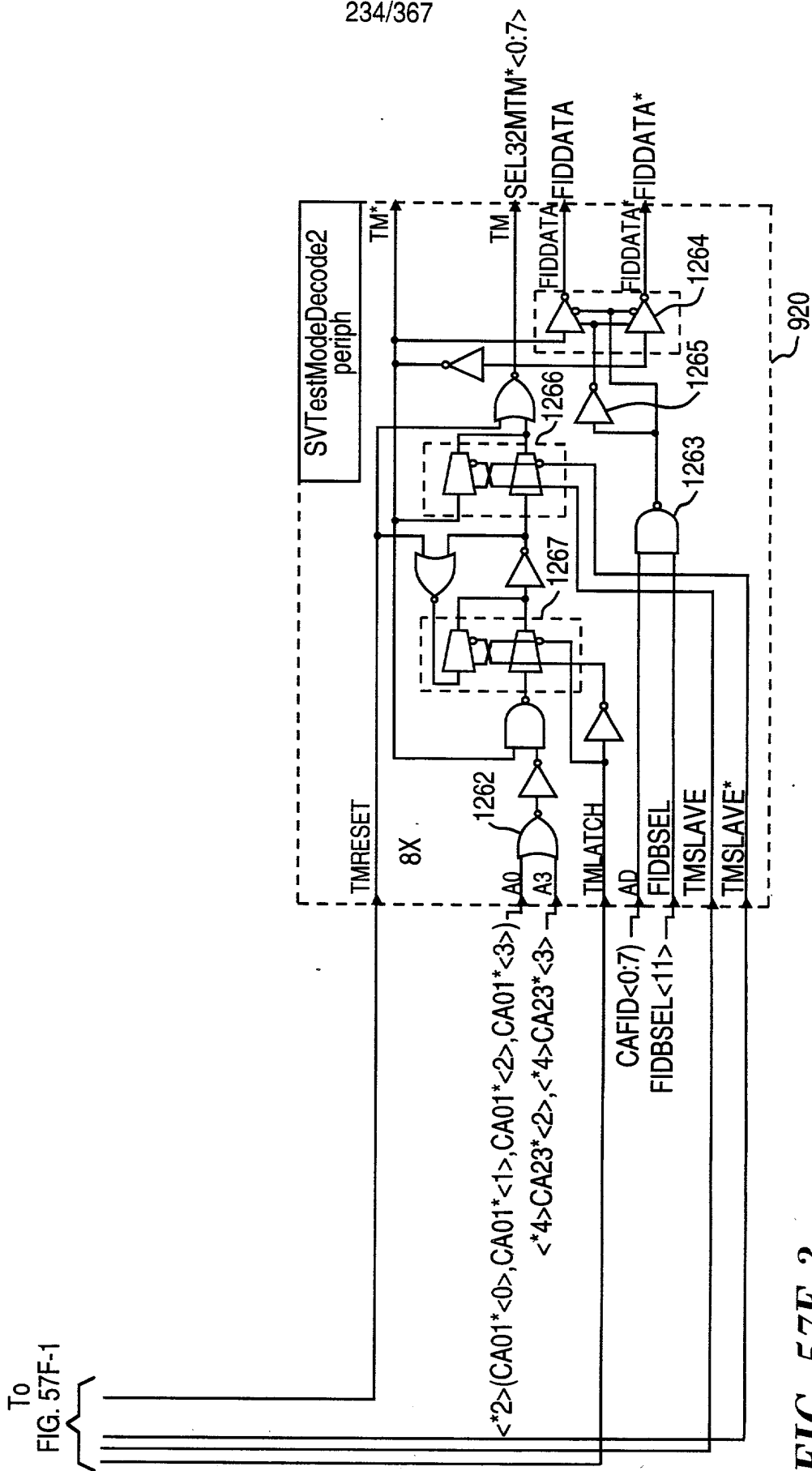


FIG. 57F-3

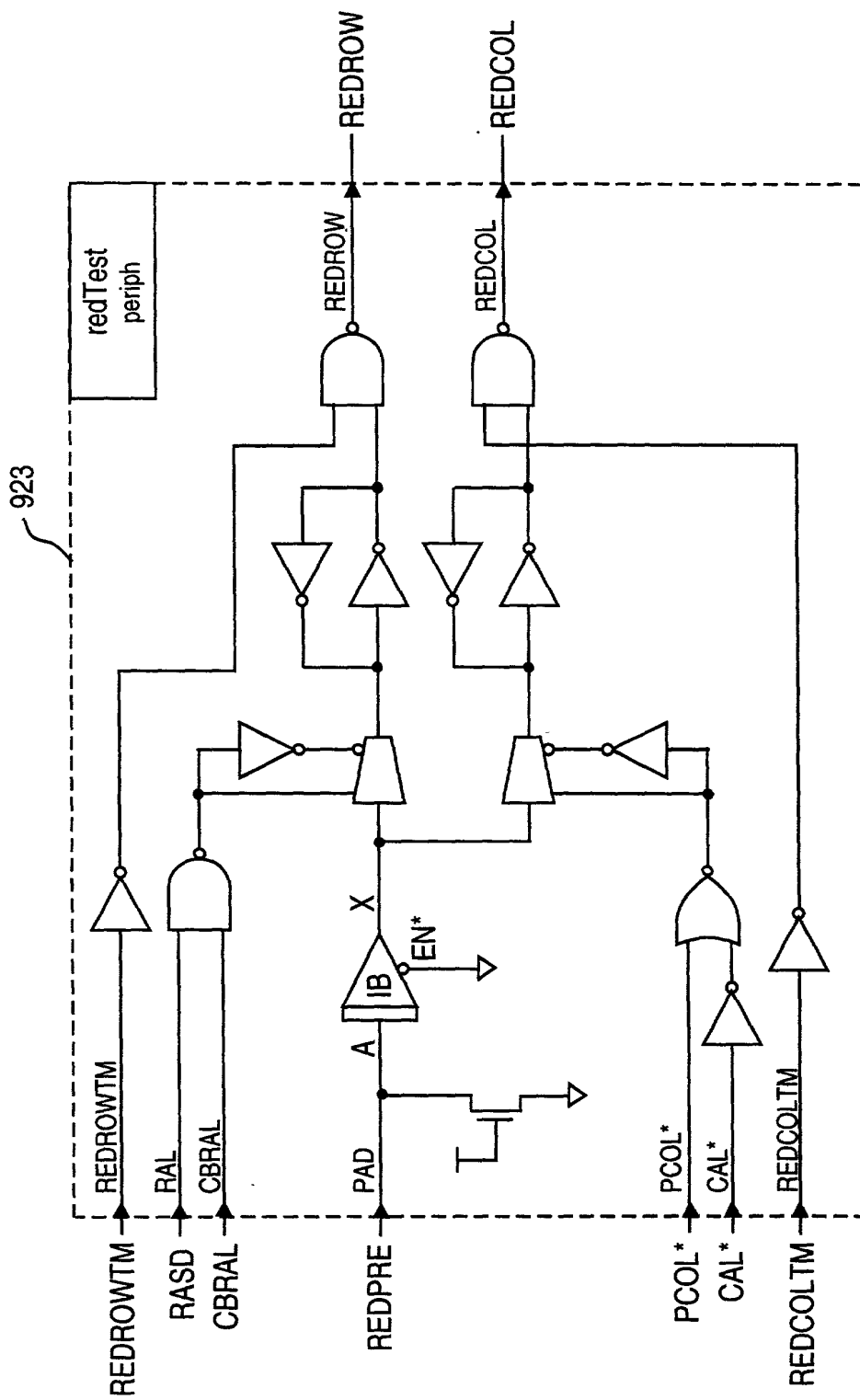
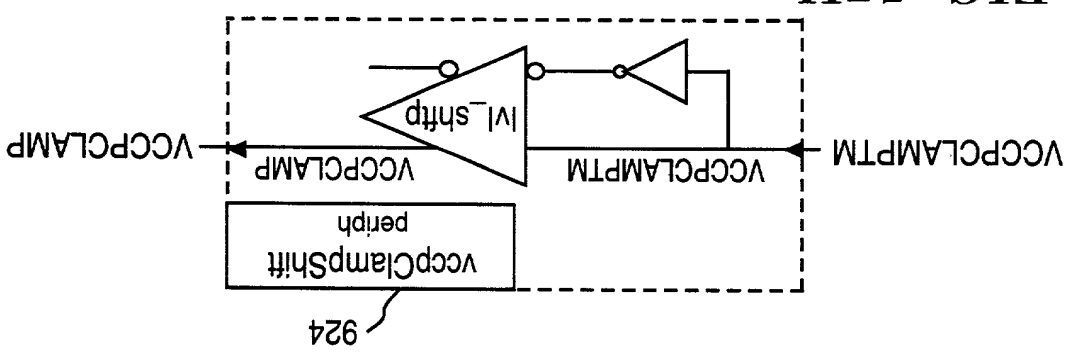


FIG. 57C

FIG. 57H



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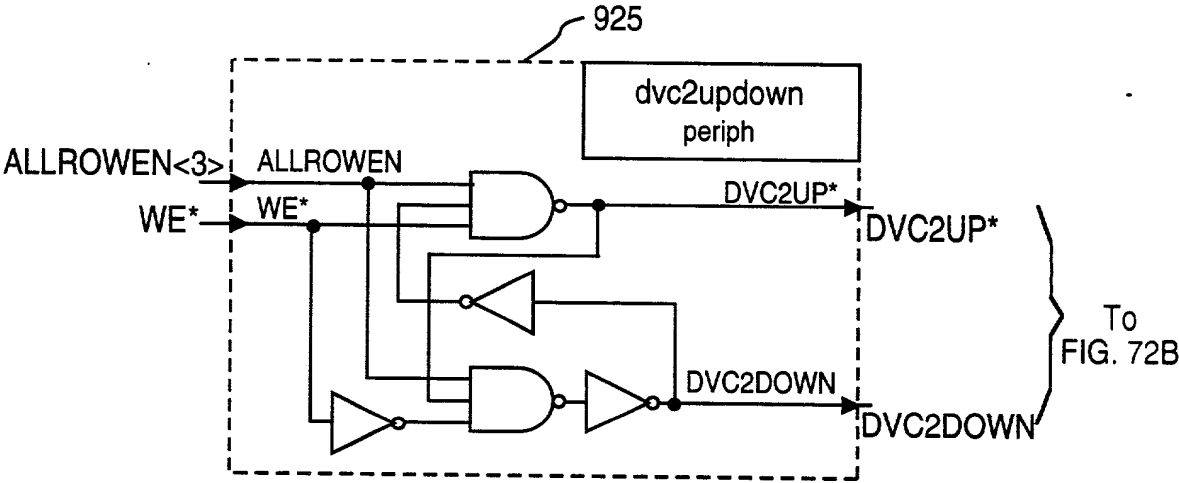
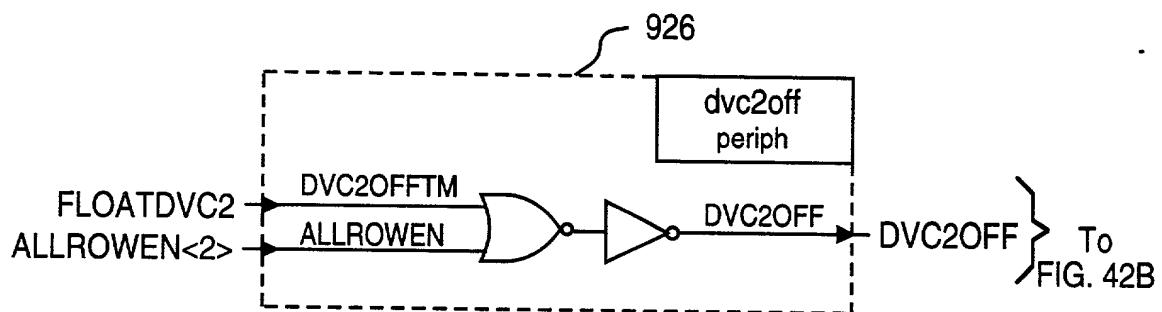
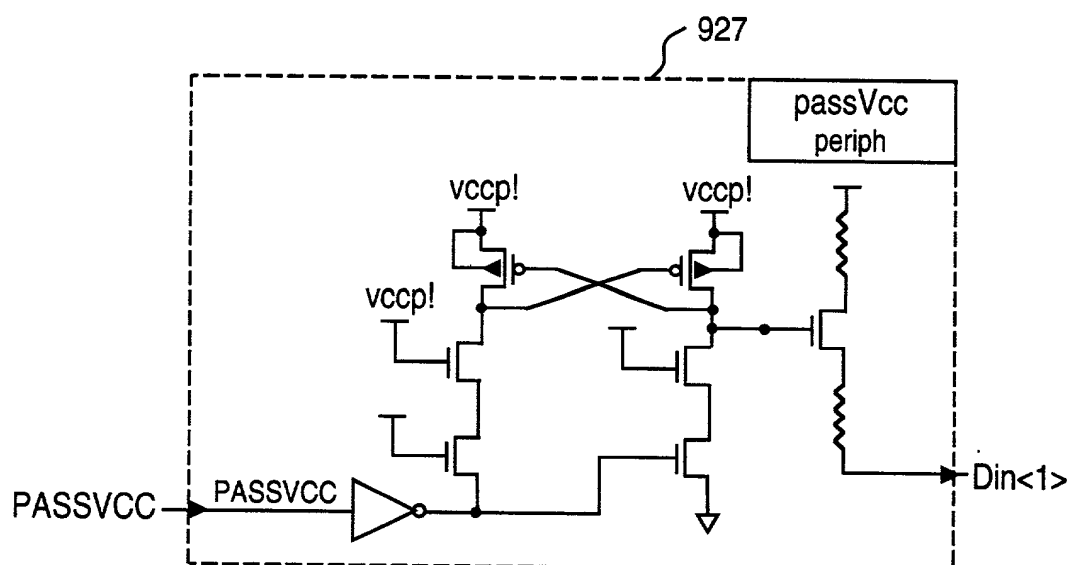
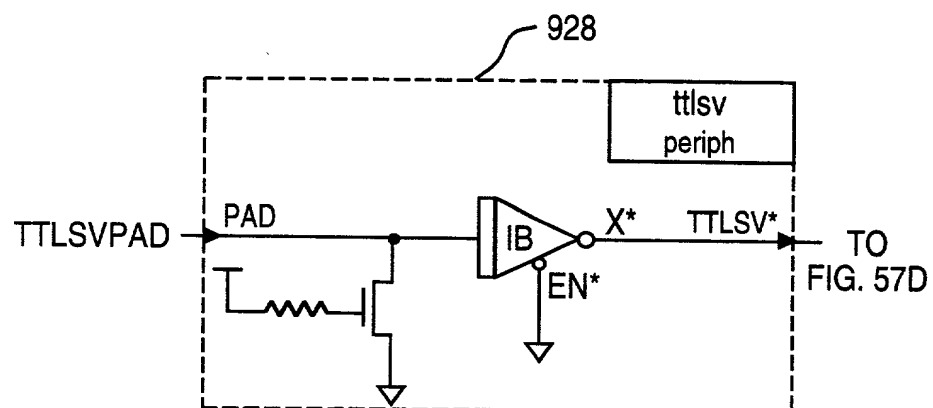
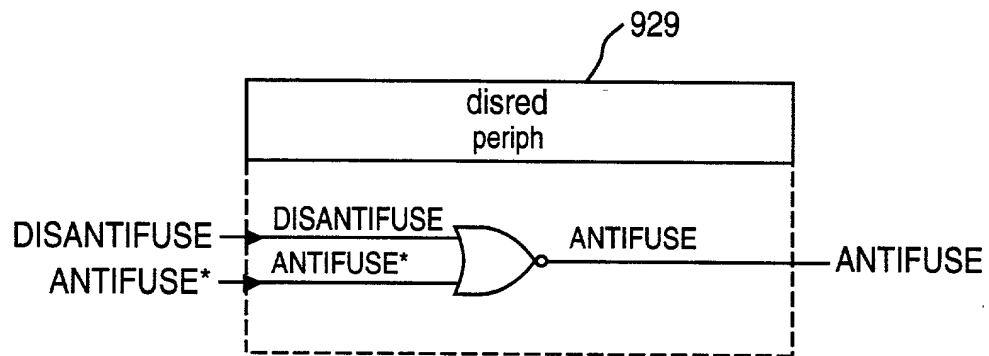


FIG. 57I

**FIG. 57J**

**FIG. 57K**

**FIG. 57L**

**FIG. 57M**

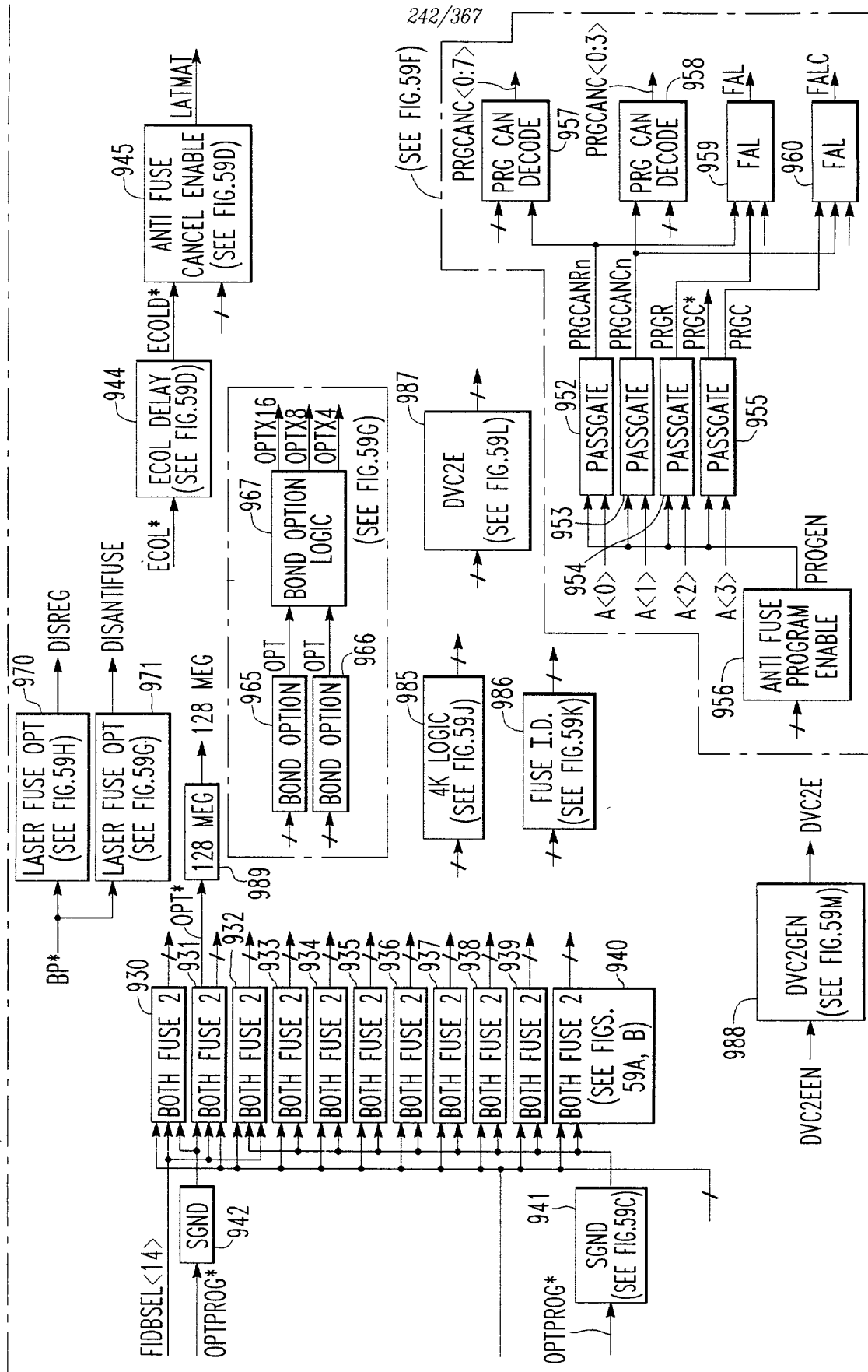
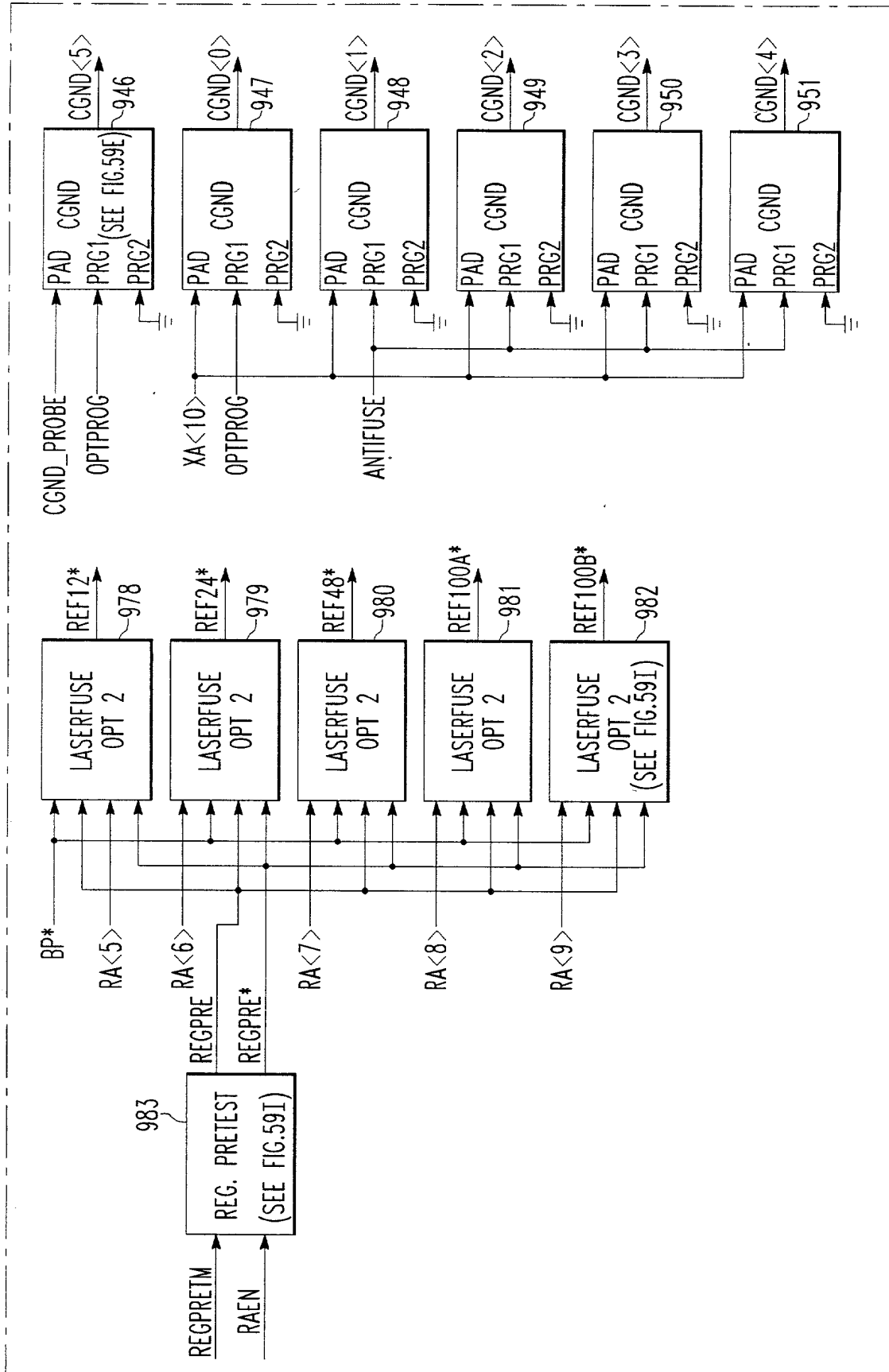
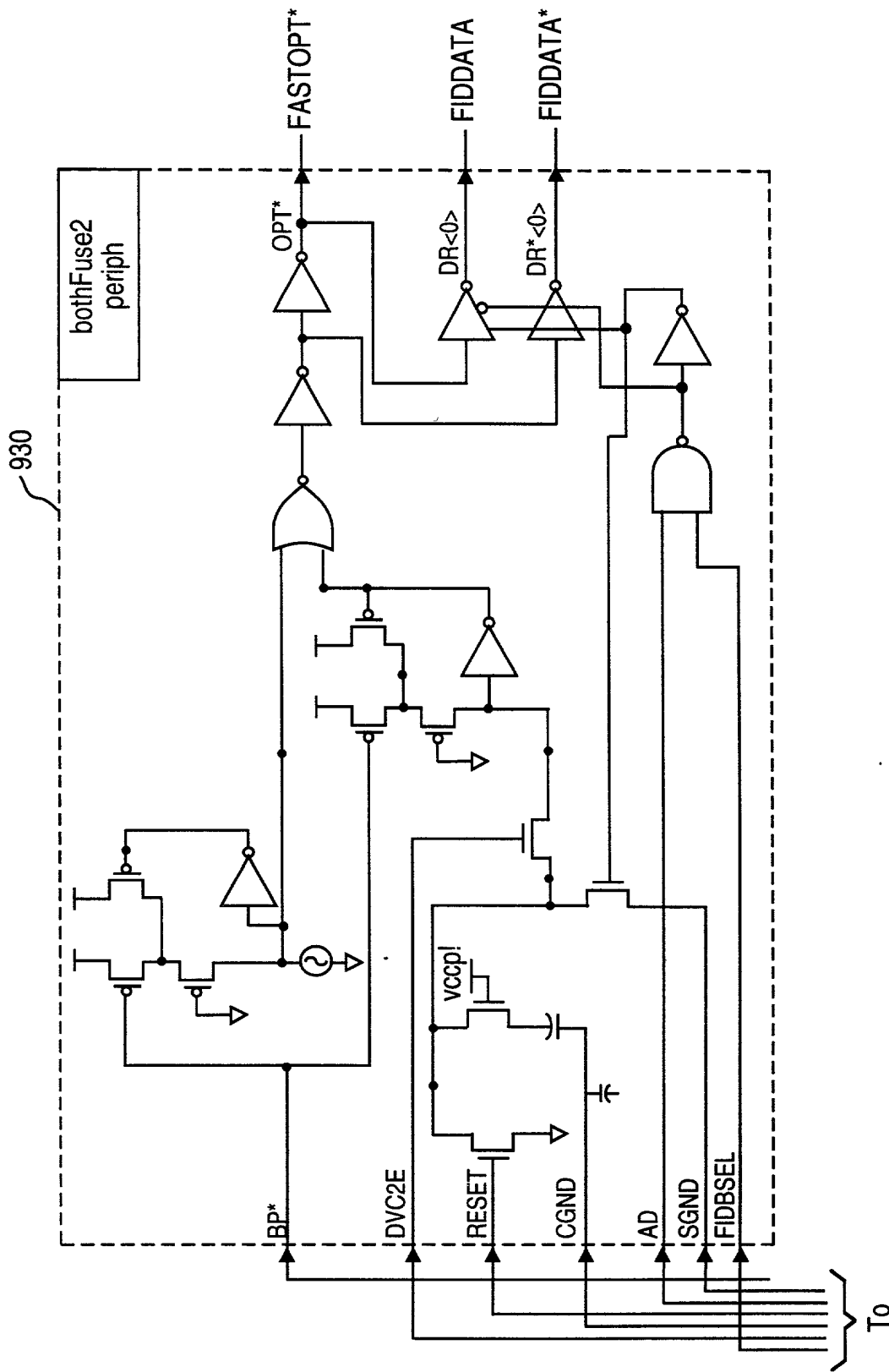


FIG. 58A





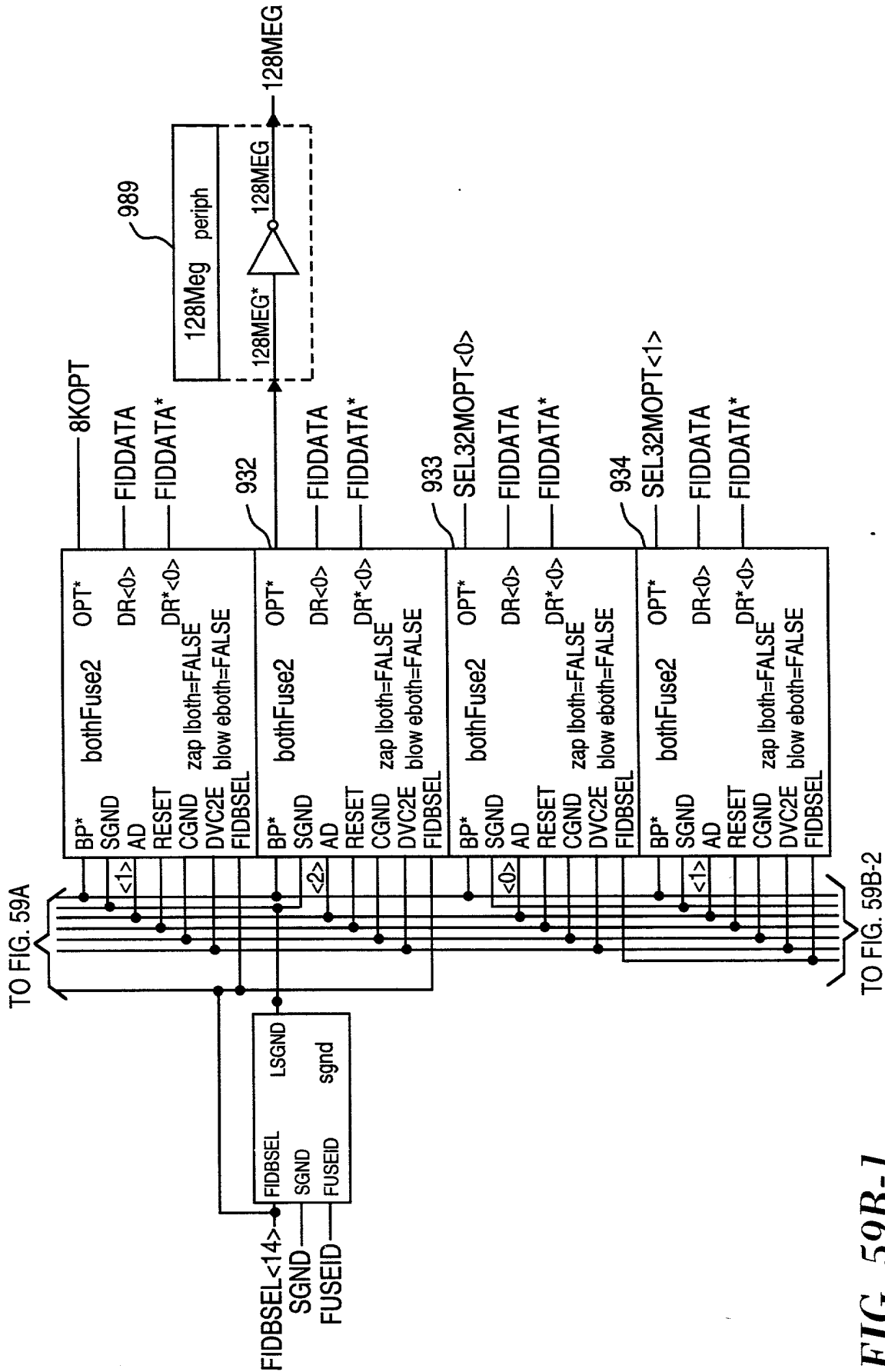


FIG. 59B-1

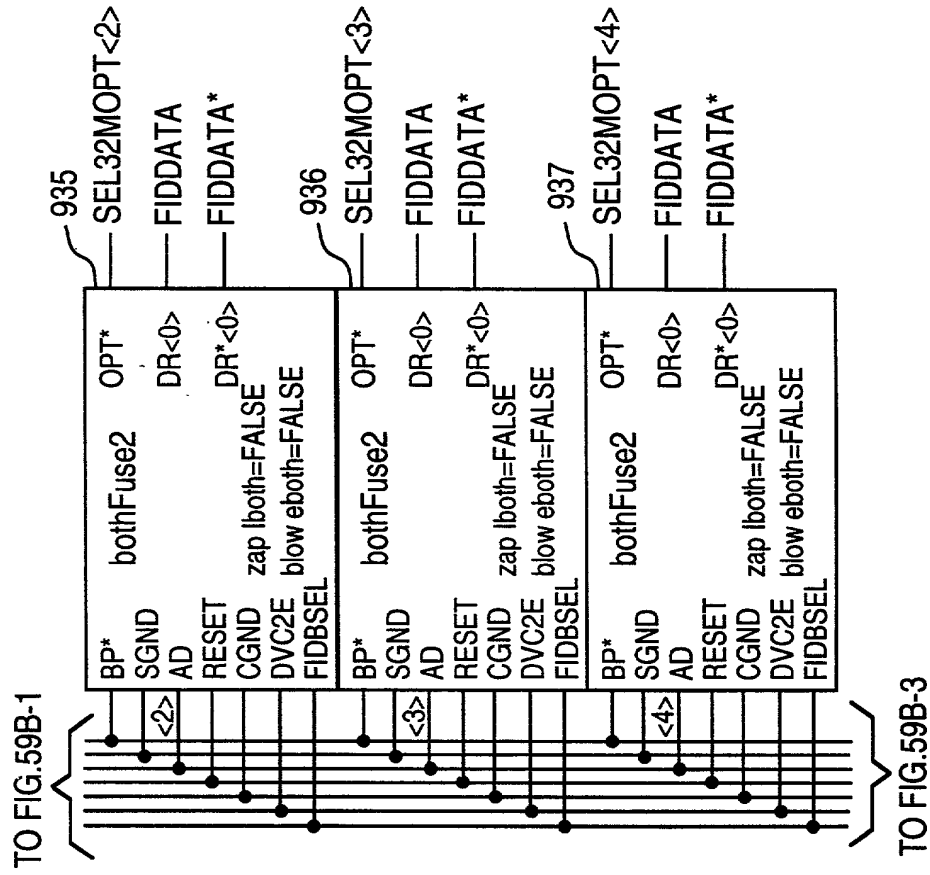


FIG. 59B-2

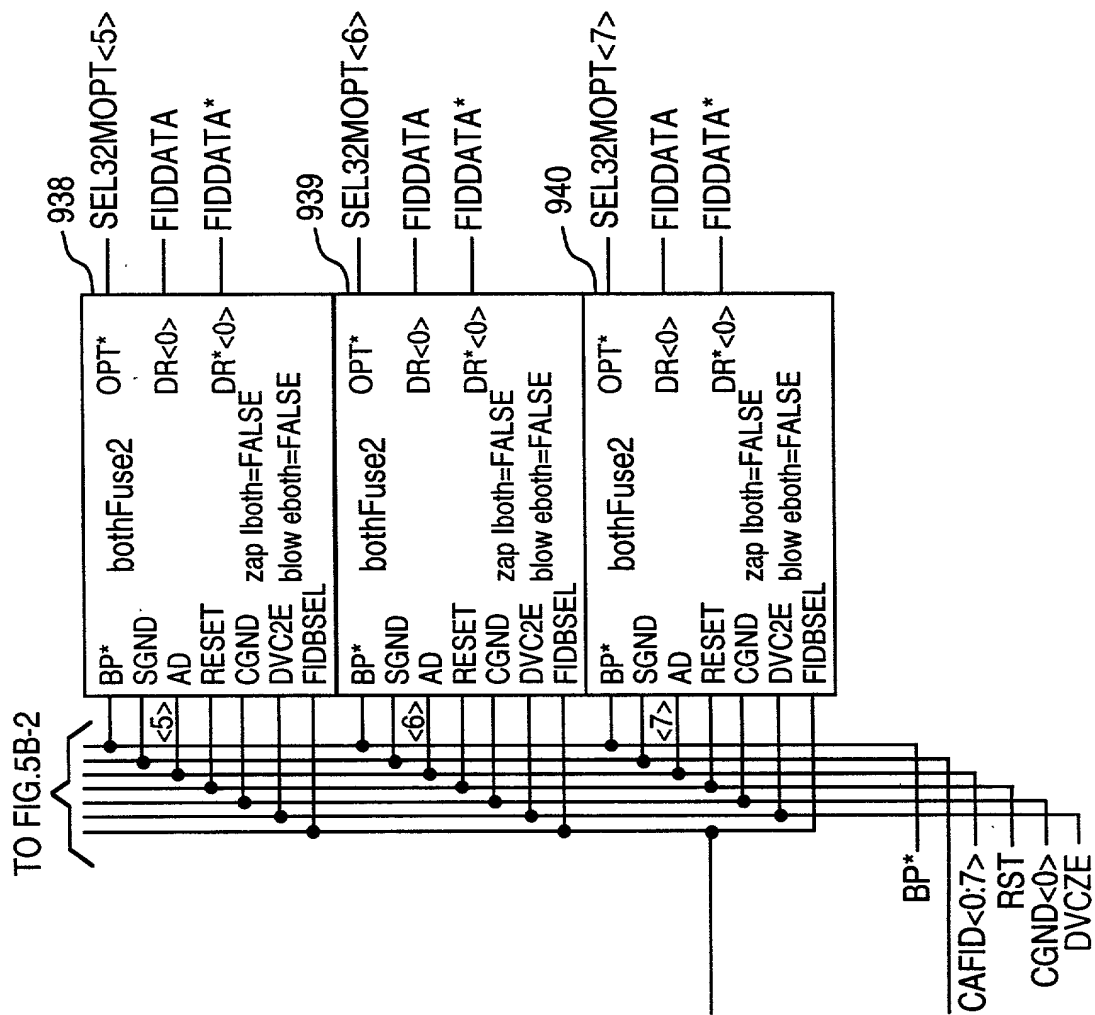
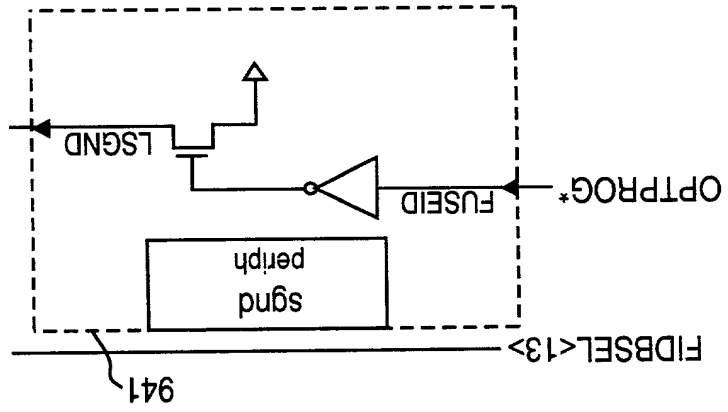


FIG. 59B-3

FIG. 59C



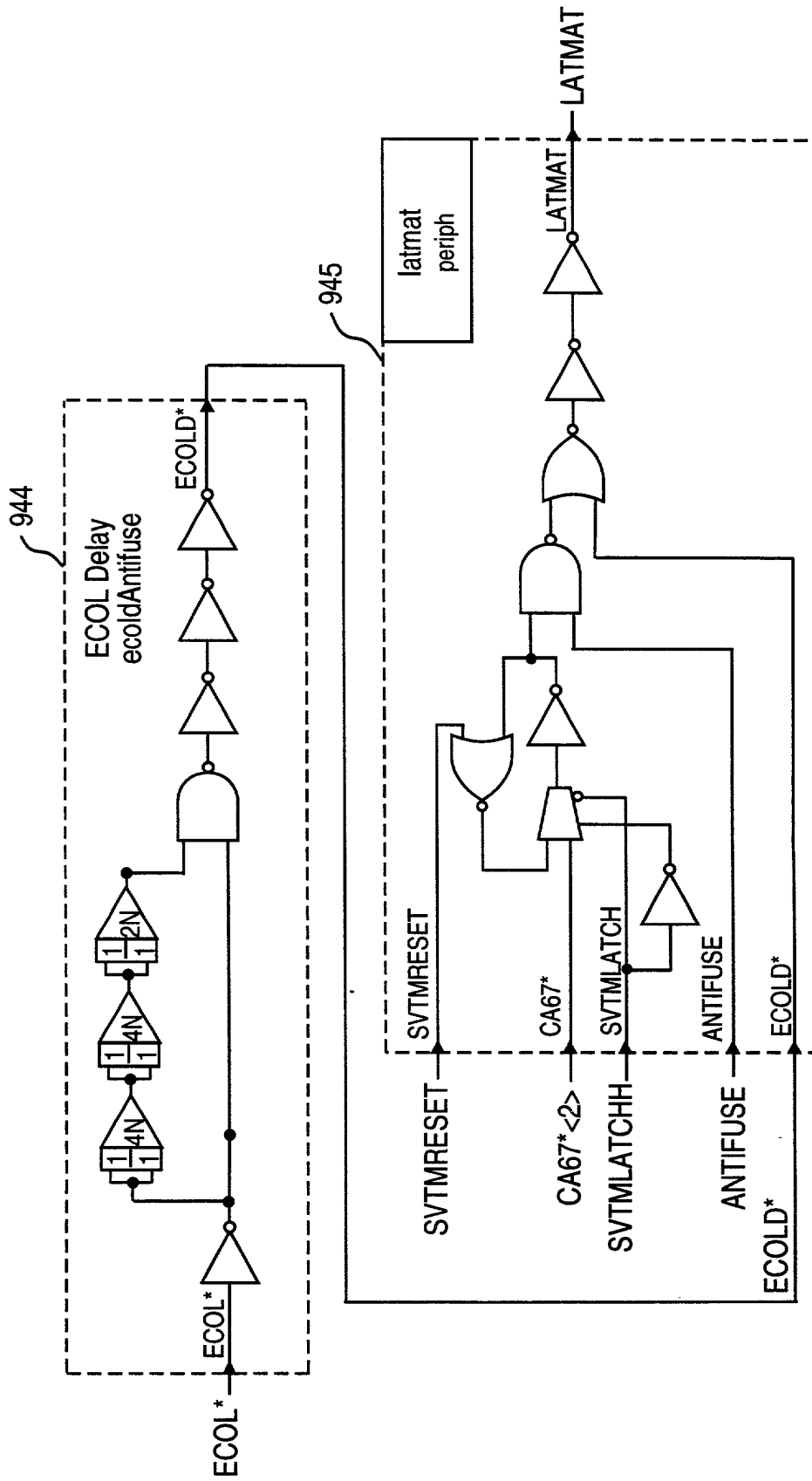


FIG. 59D

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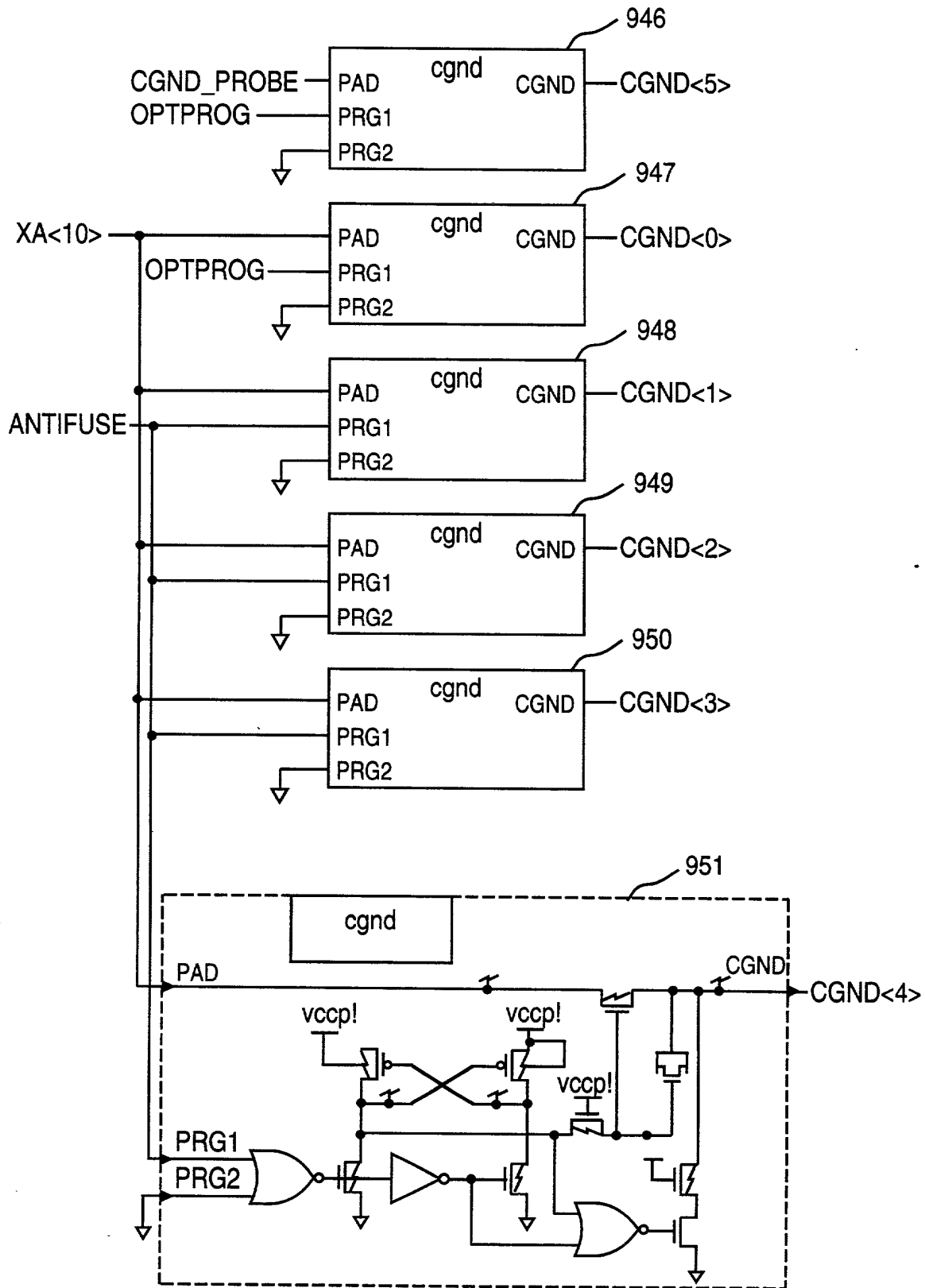


FIG. 59E



FIG. 59F-1

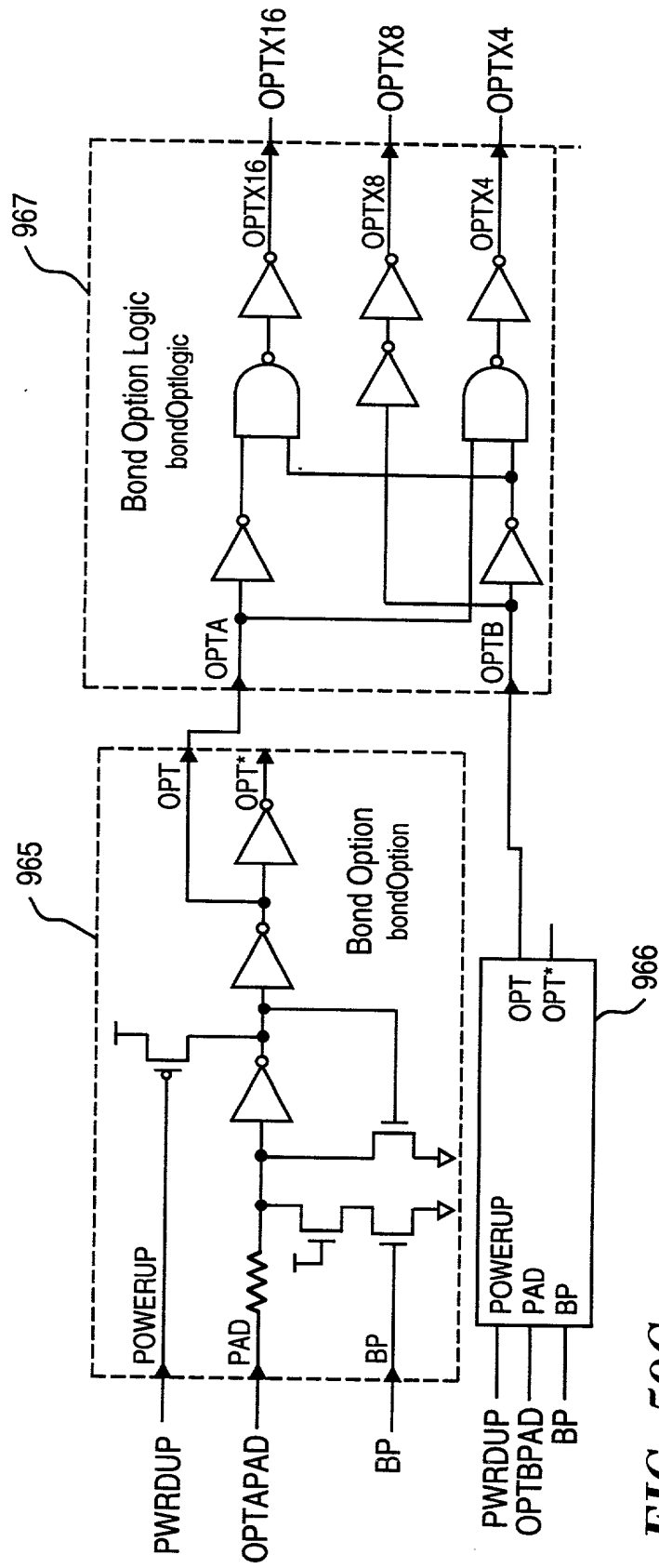
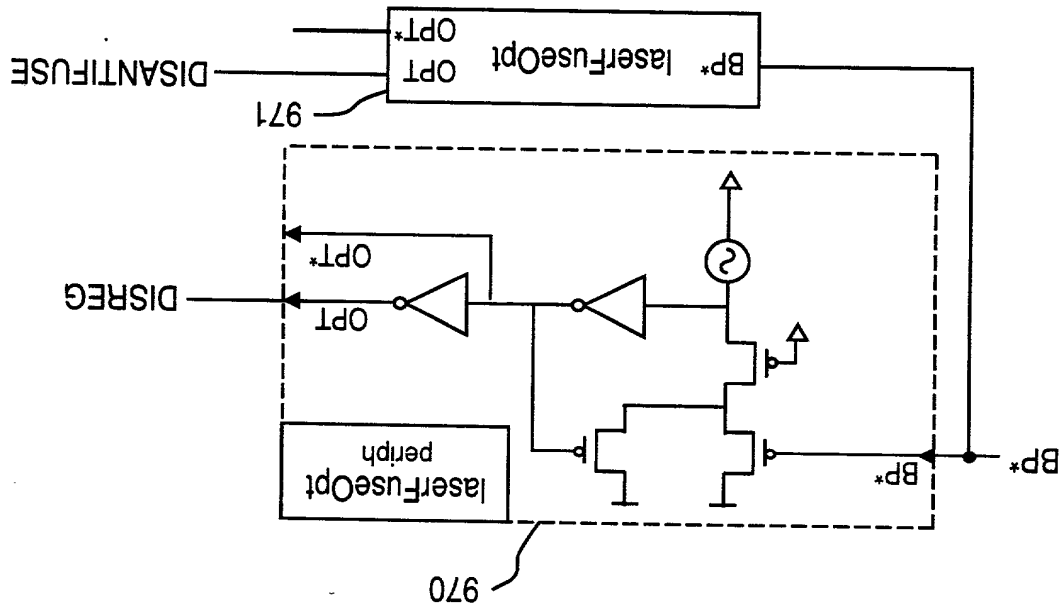


FIG. 59G

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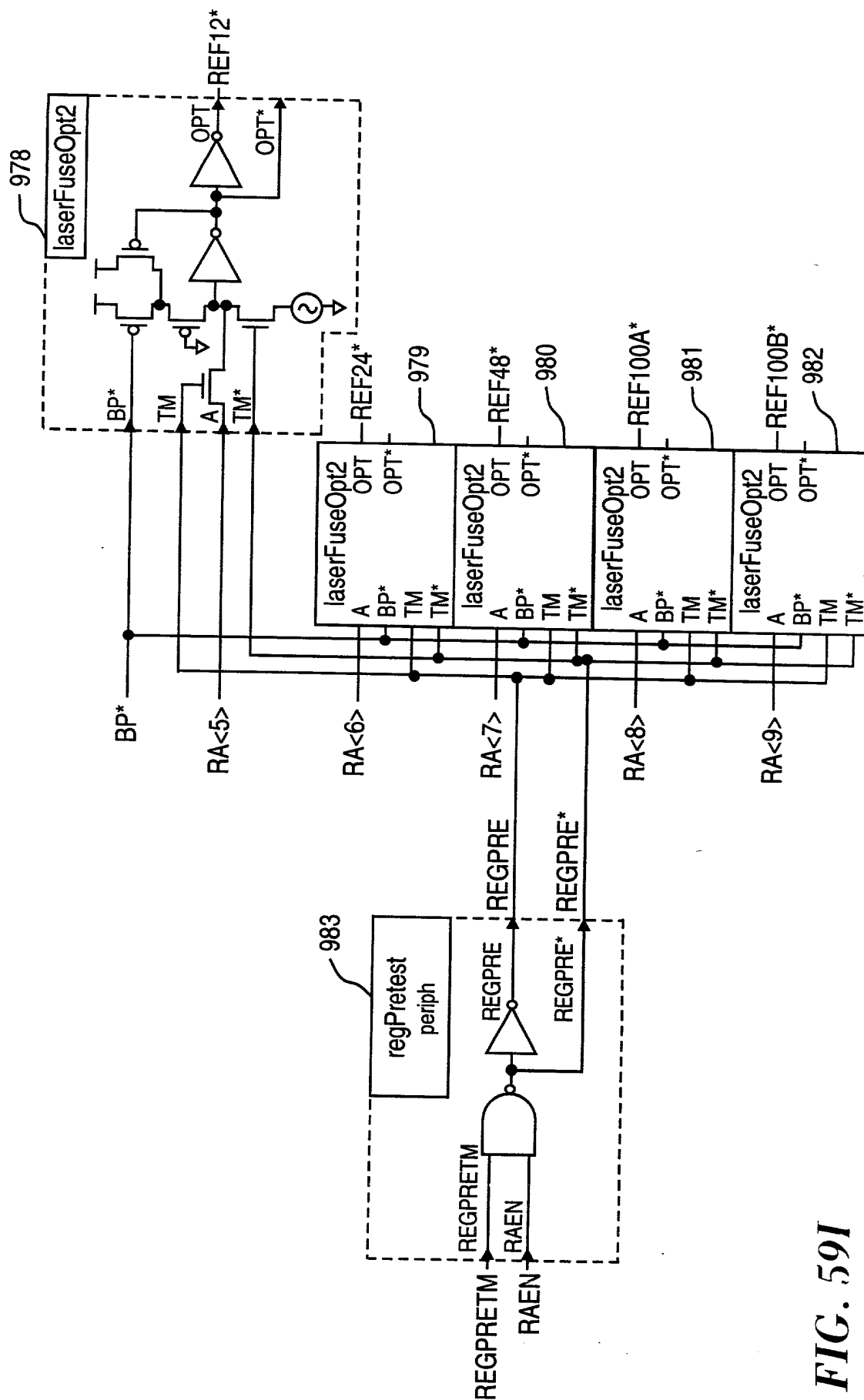
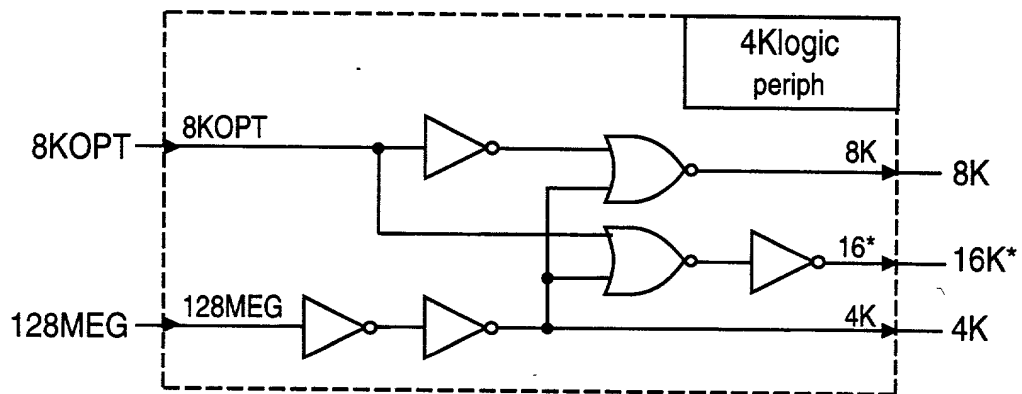


FIG. 59I

**FIG. 59J**

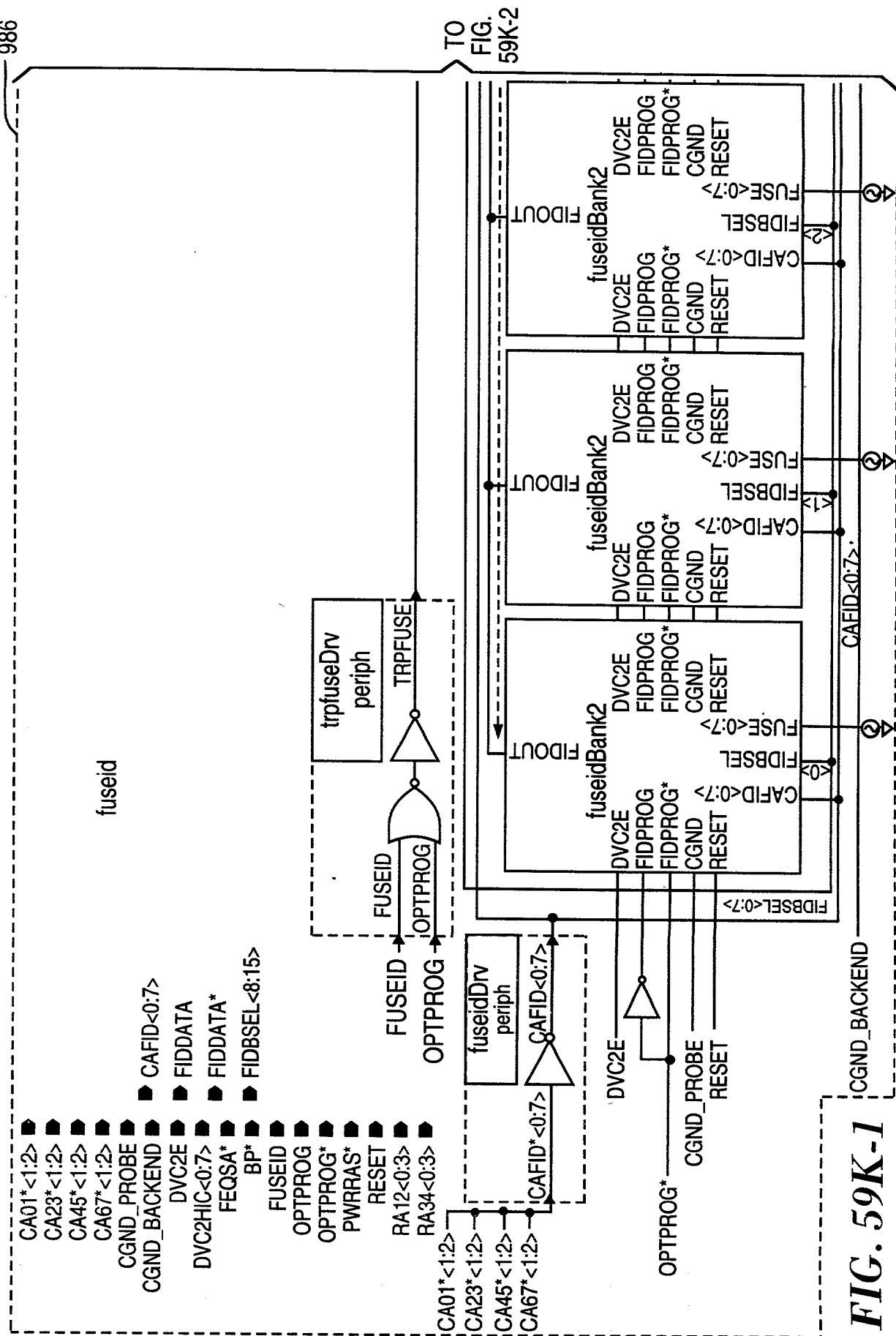


FIG. 59K-1

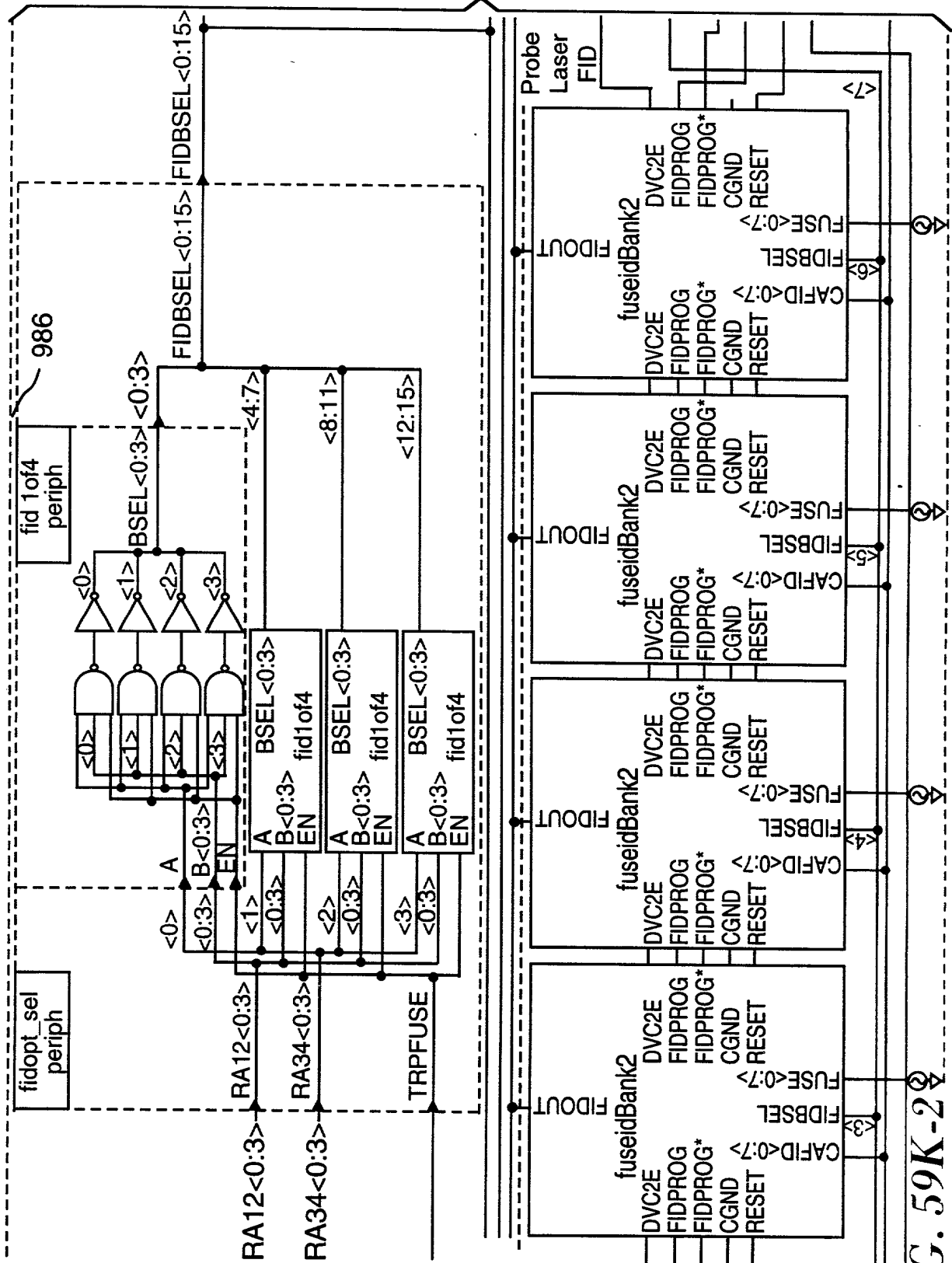
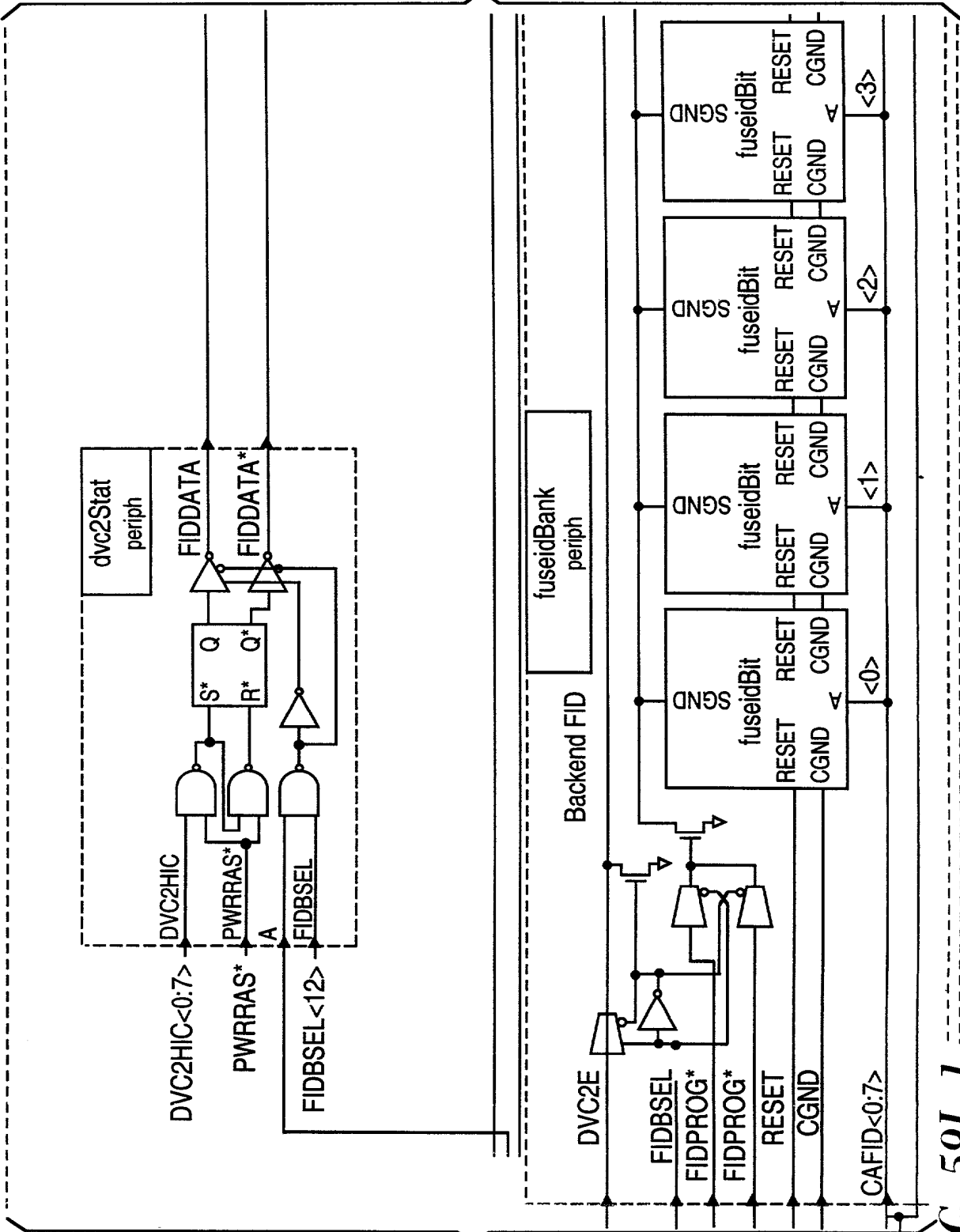
TO
FIG.
59L-1

FIG. 59K-2

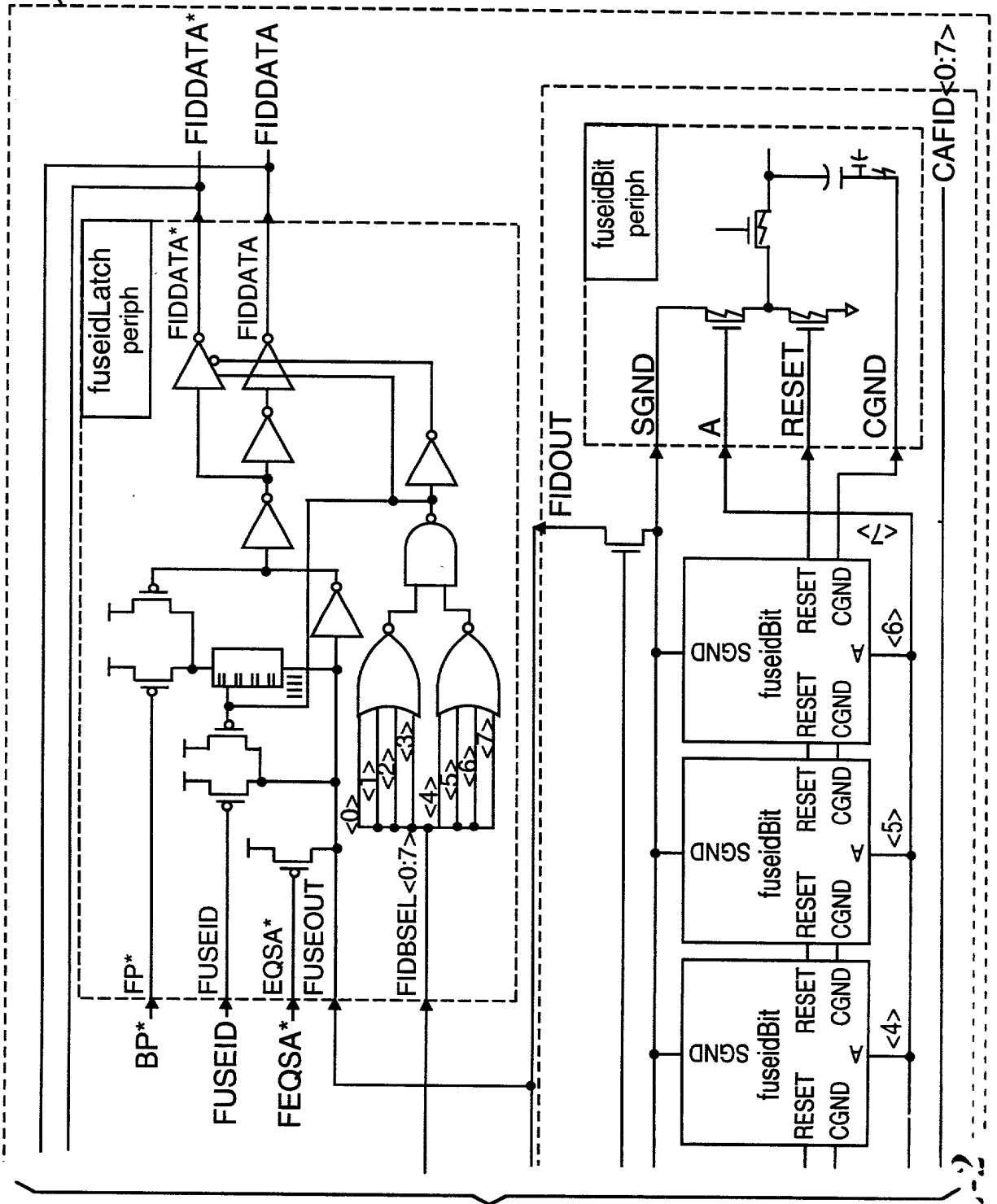
TO
FIG.
59L-2



TO
FIG.
59K-1

FIG. 59L-1

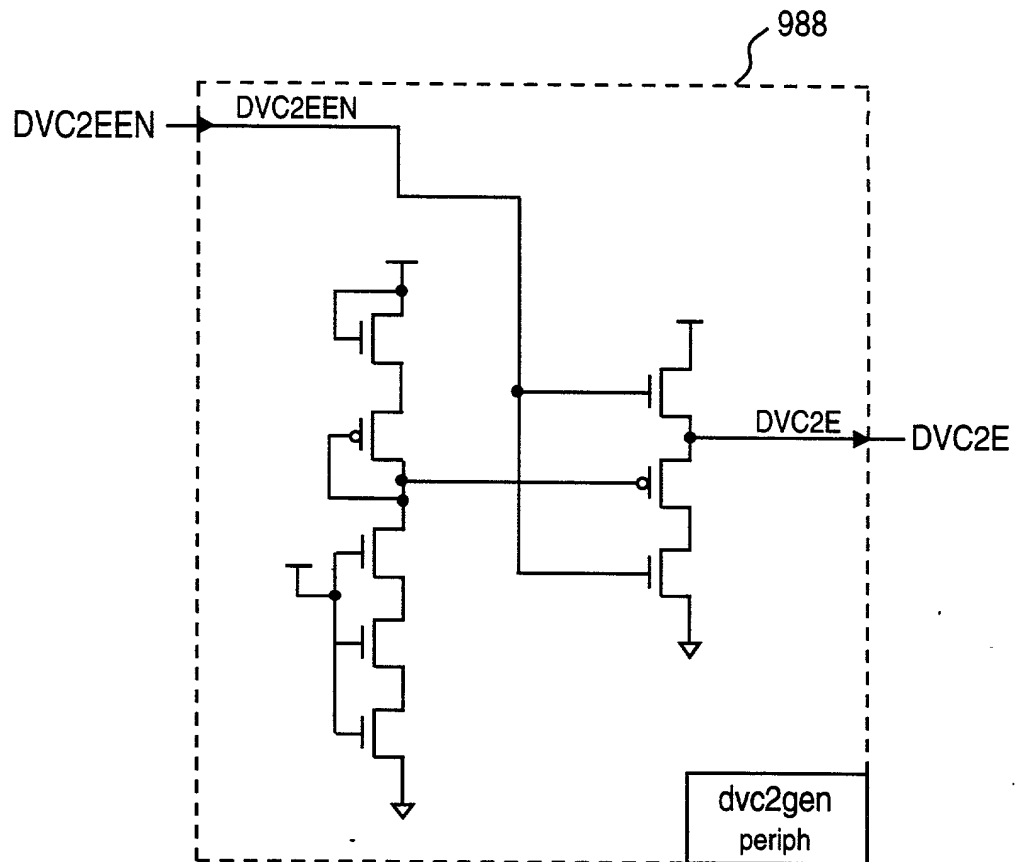
986

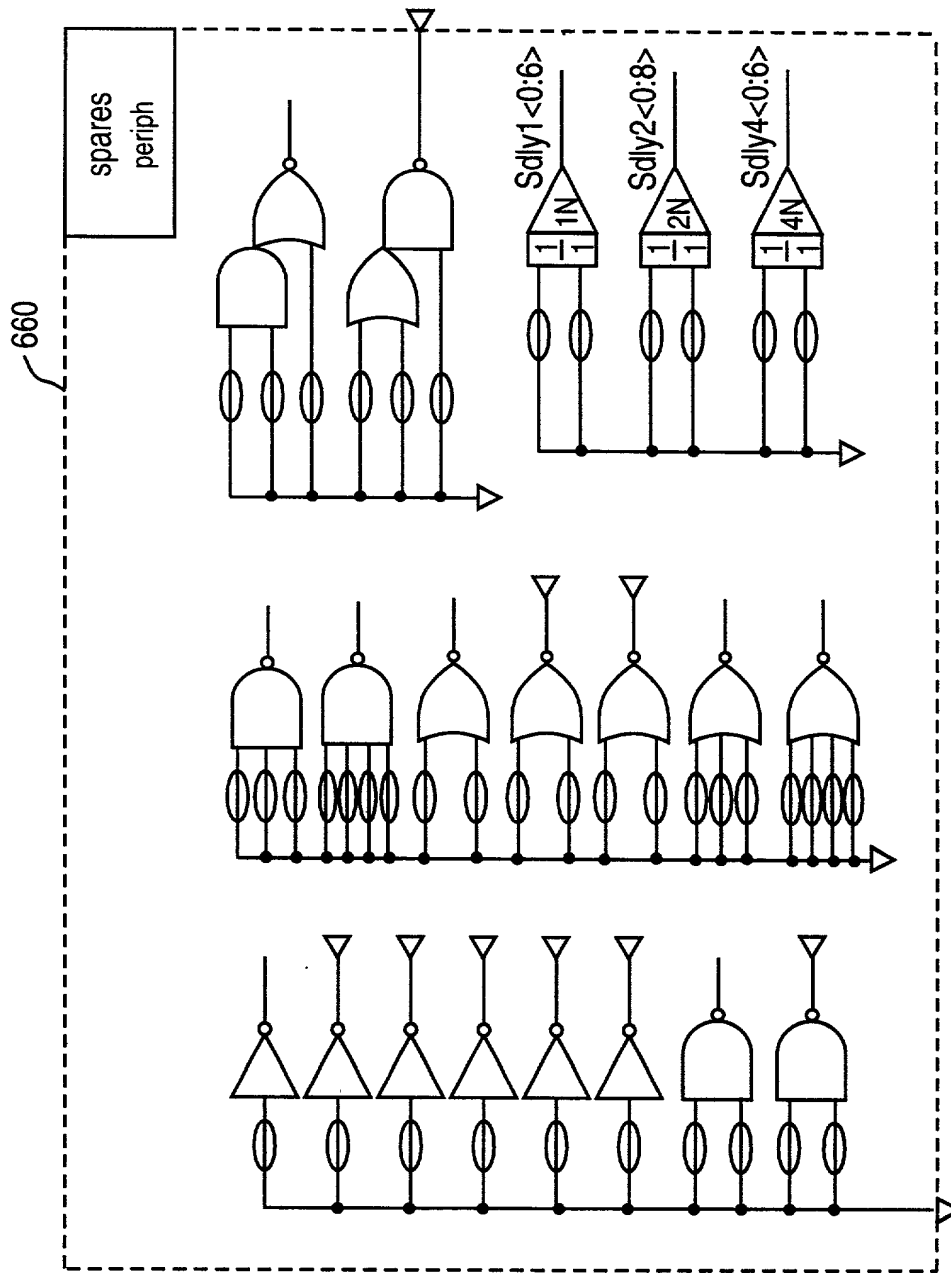


TO
FIG.
59L-1

FIG. 59L-2

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**FIG. 59N**



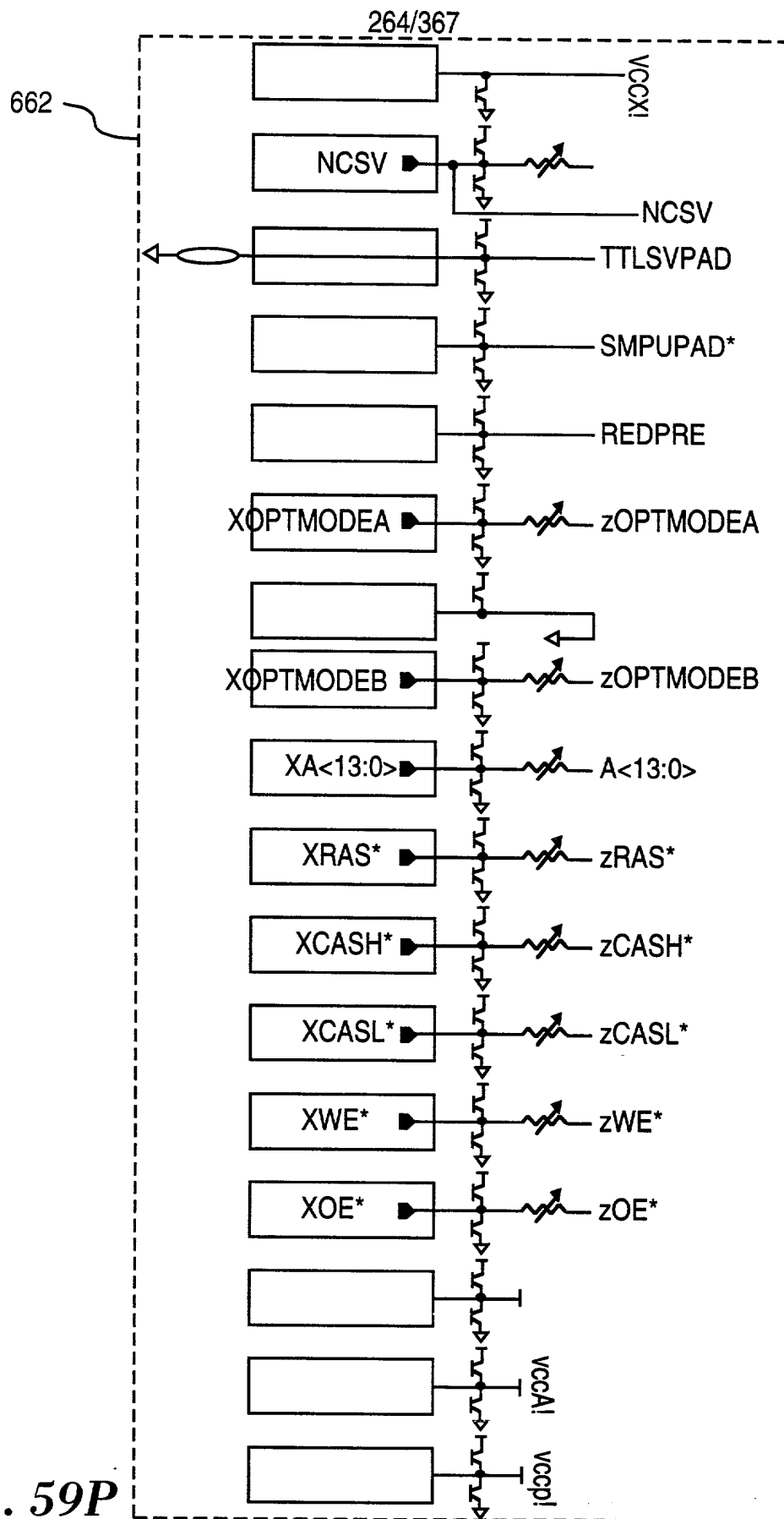


FIG. 59P

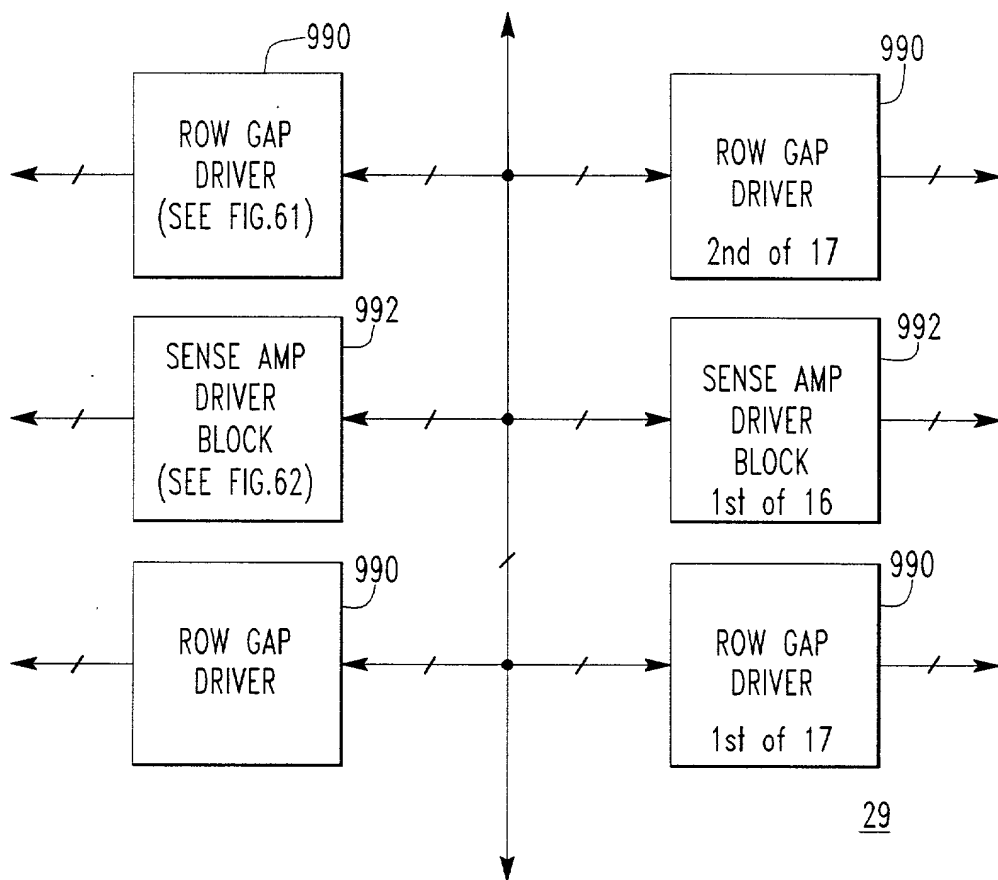


FIG. 60

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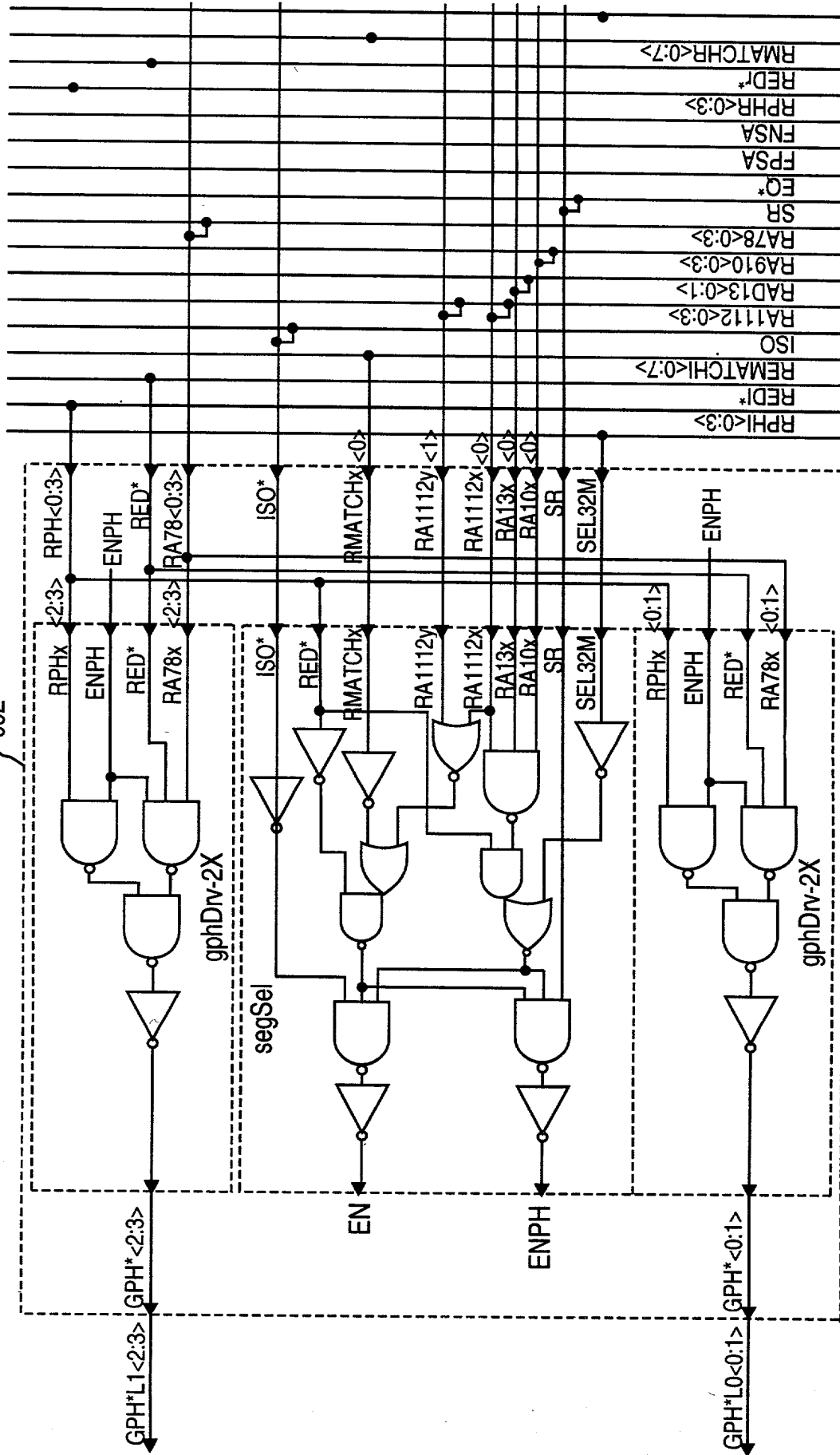


FIG. 61

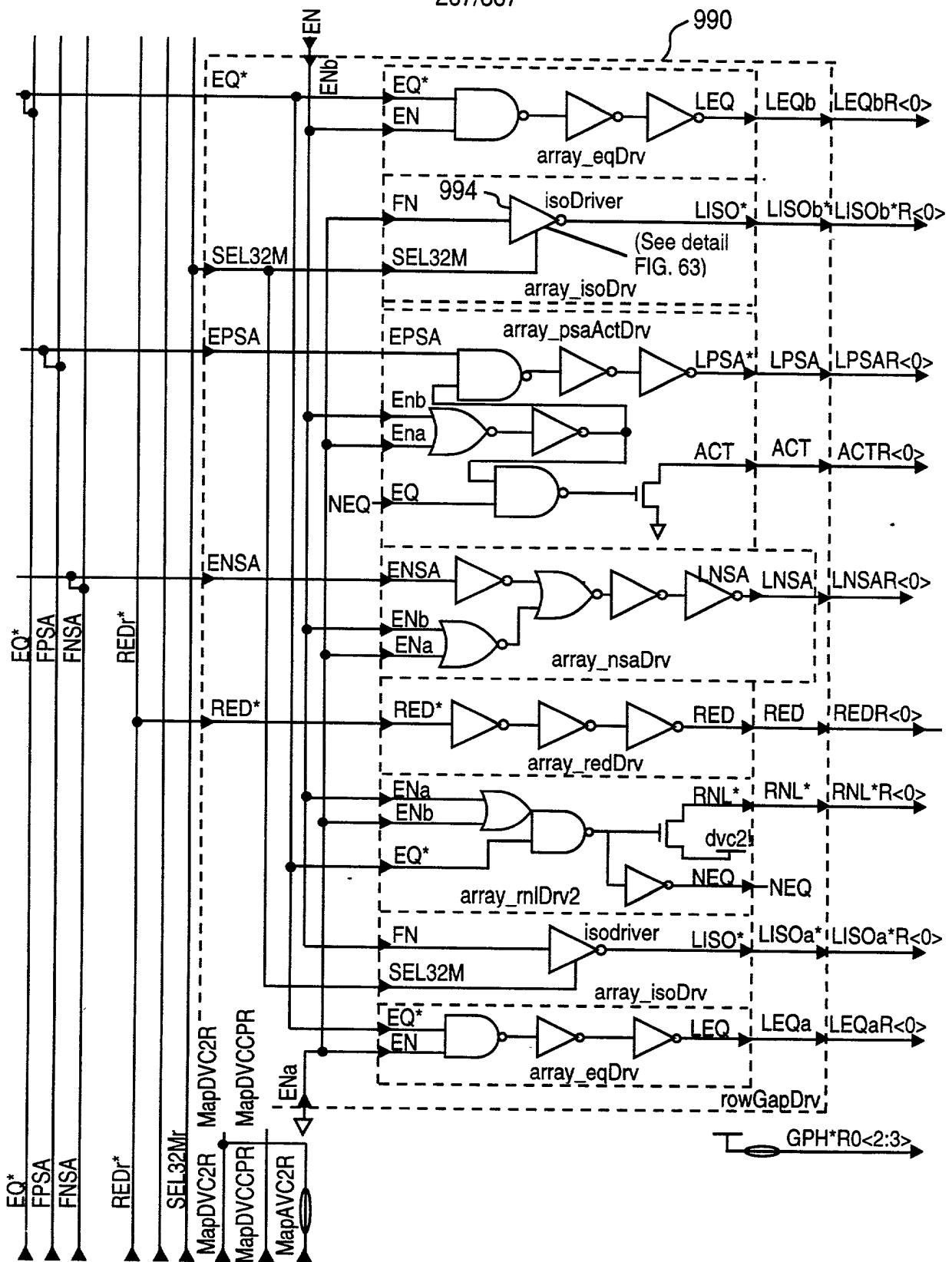


FIG. 62

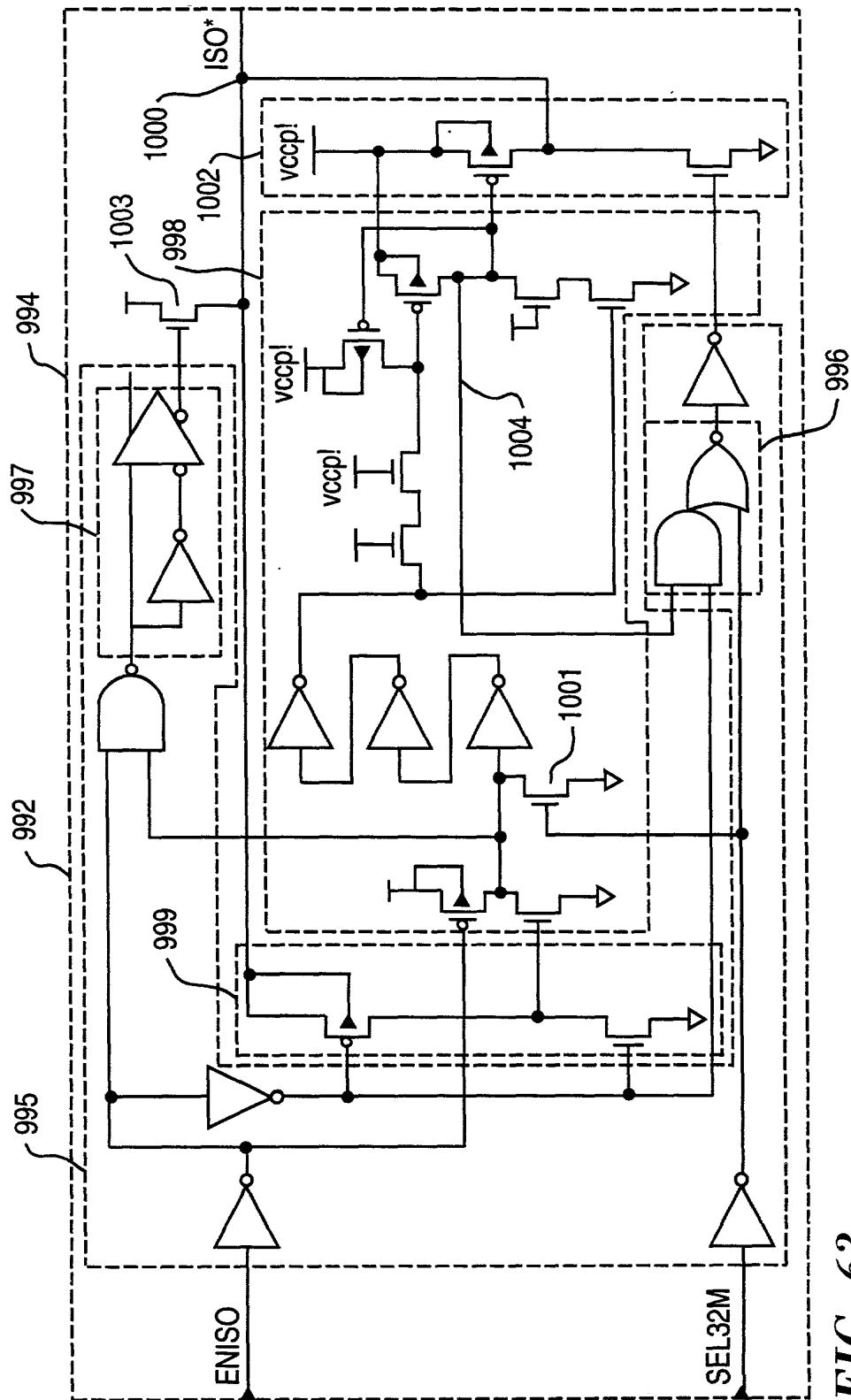


FIG. 63

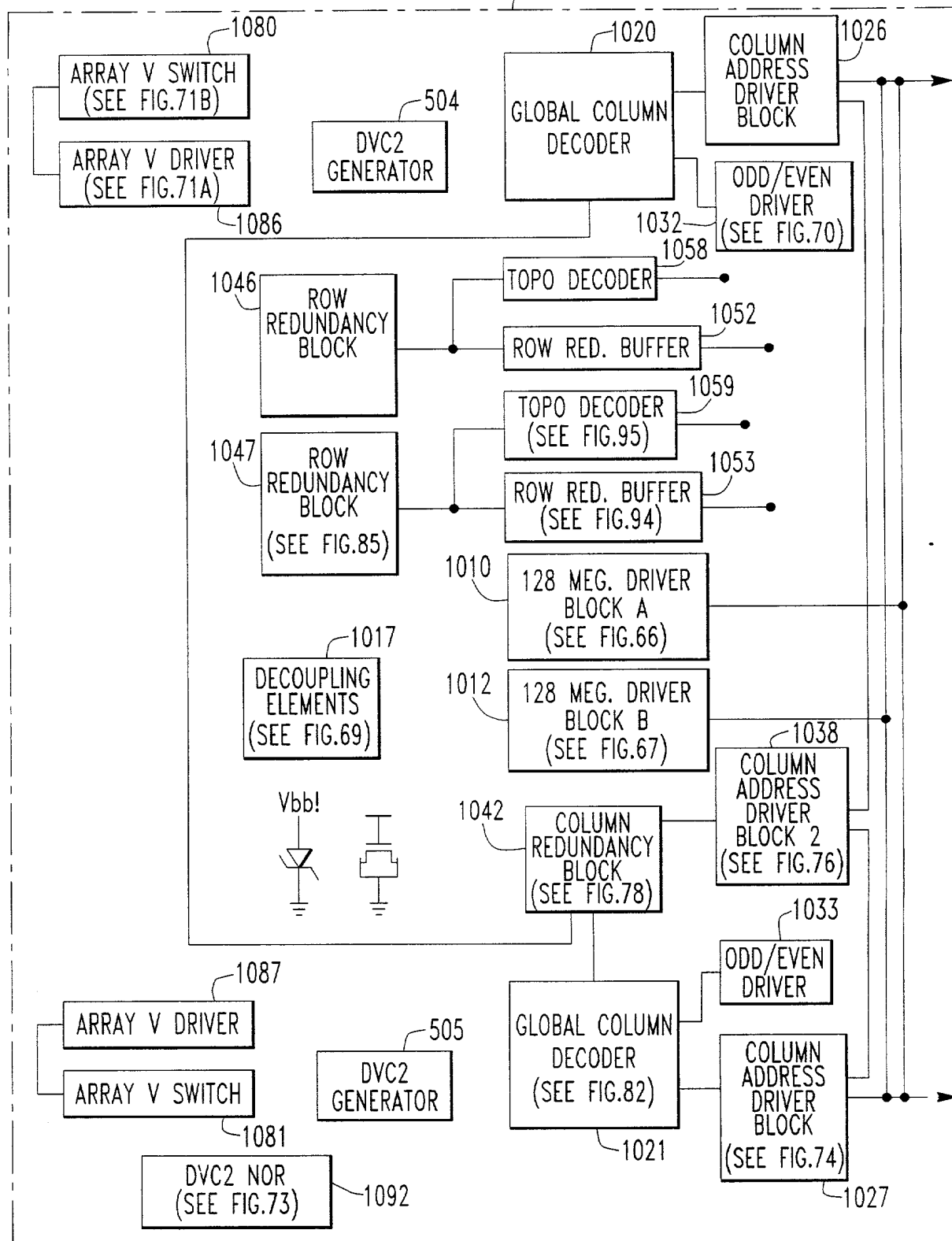


FIG. 64A

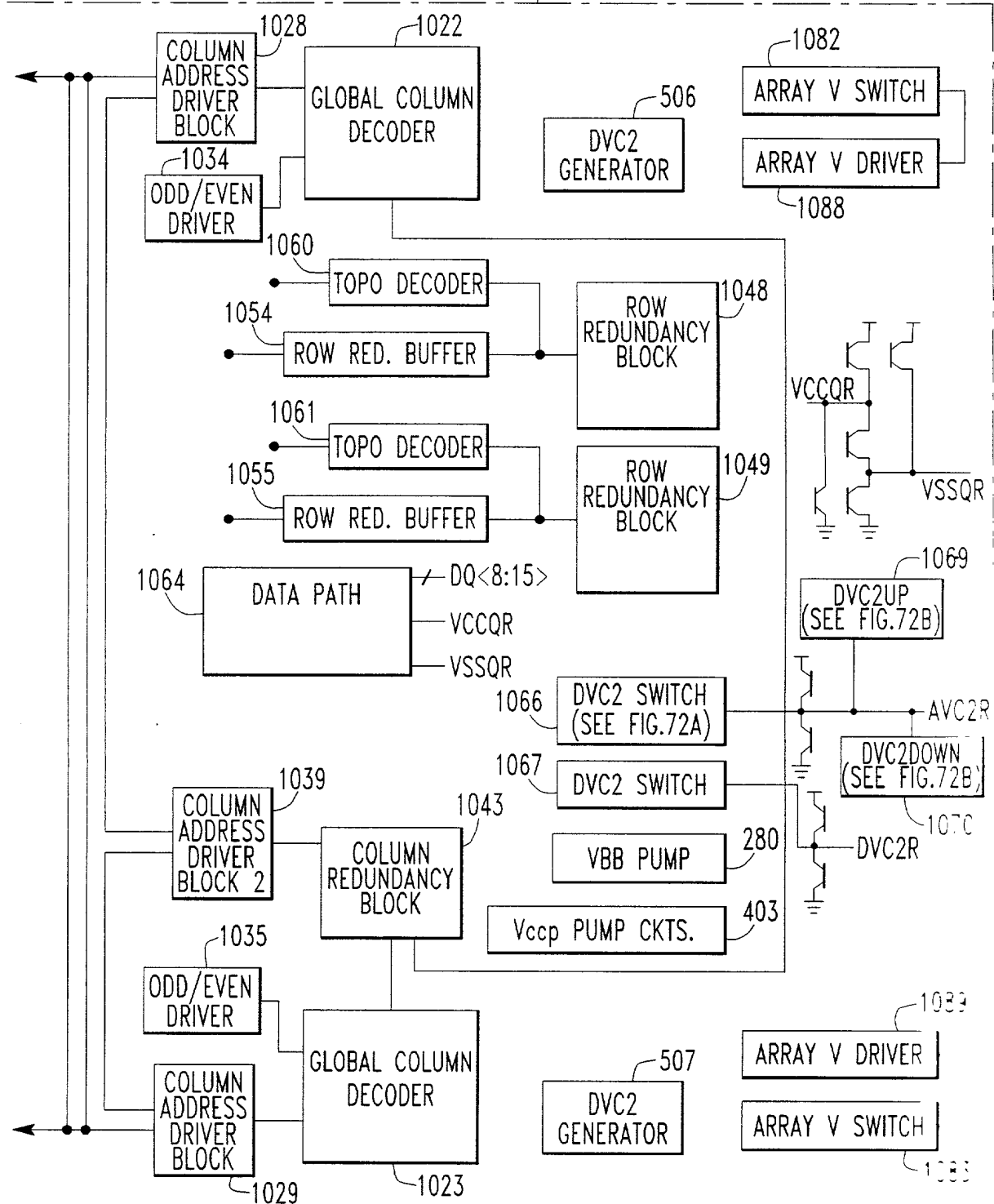


FIG. 64B

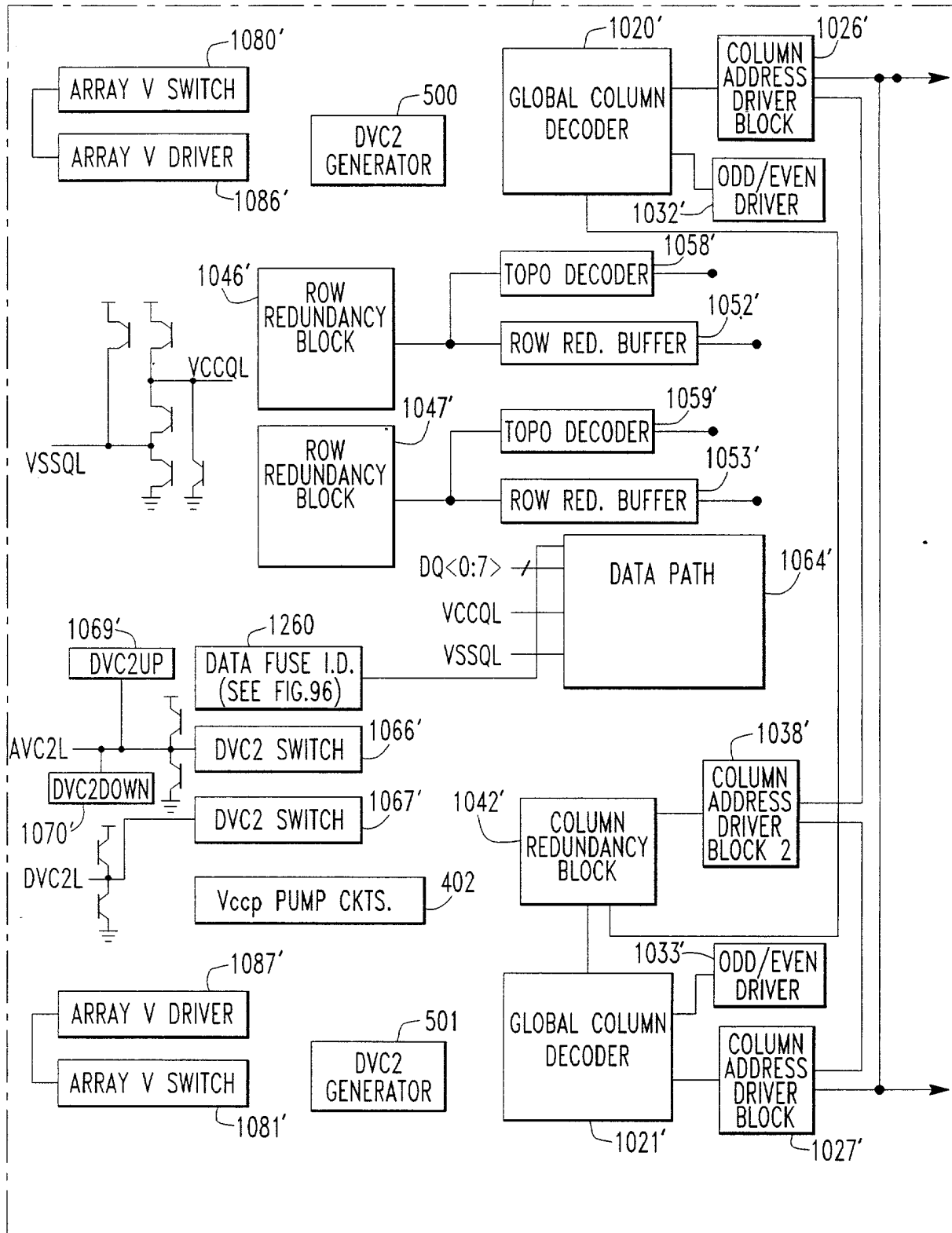


FIG. 65A

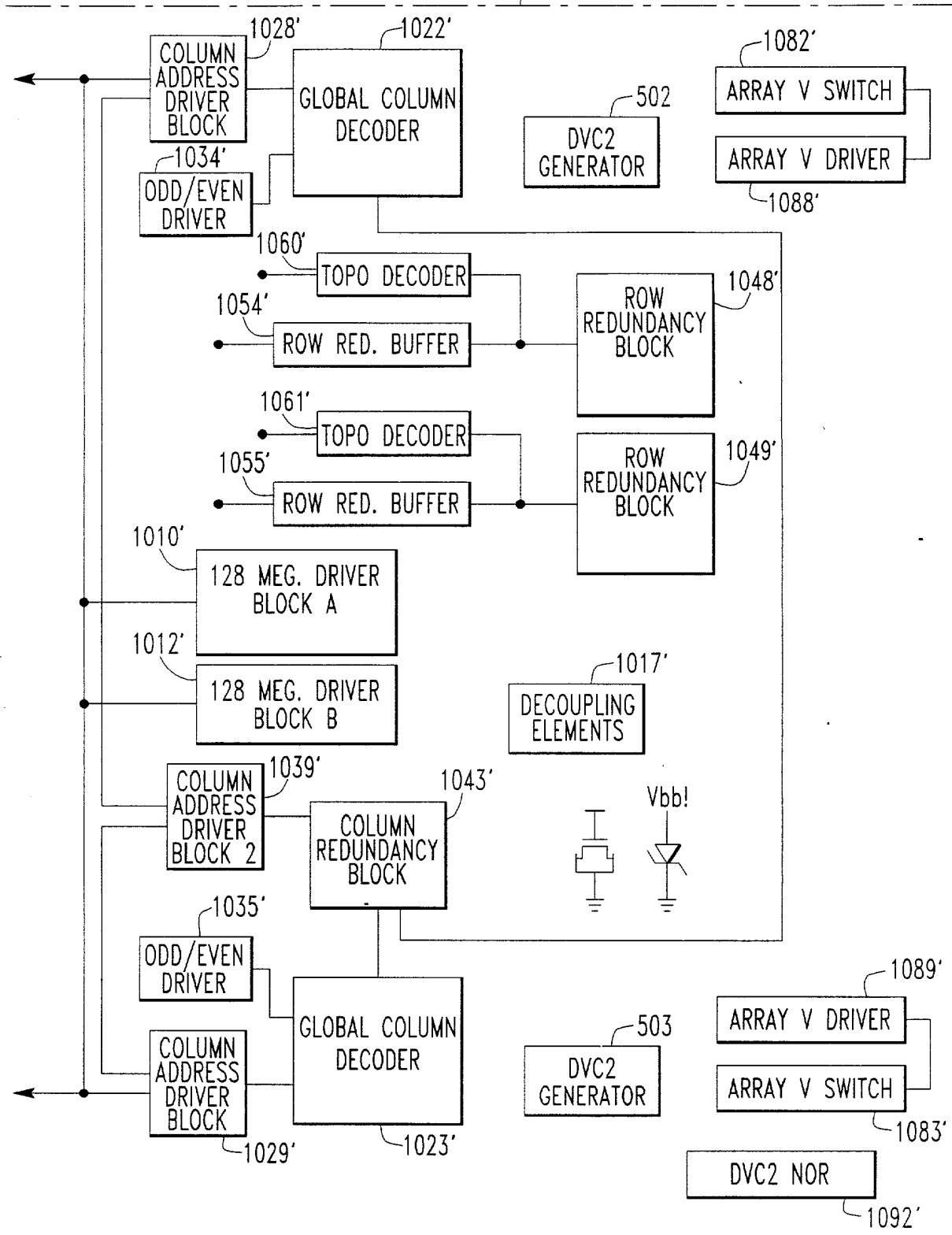
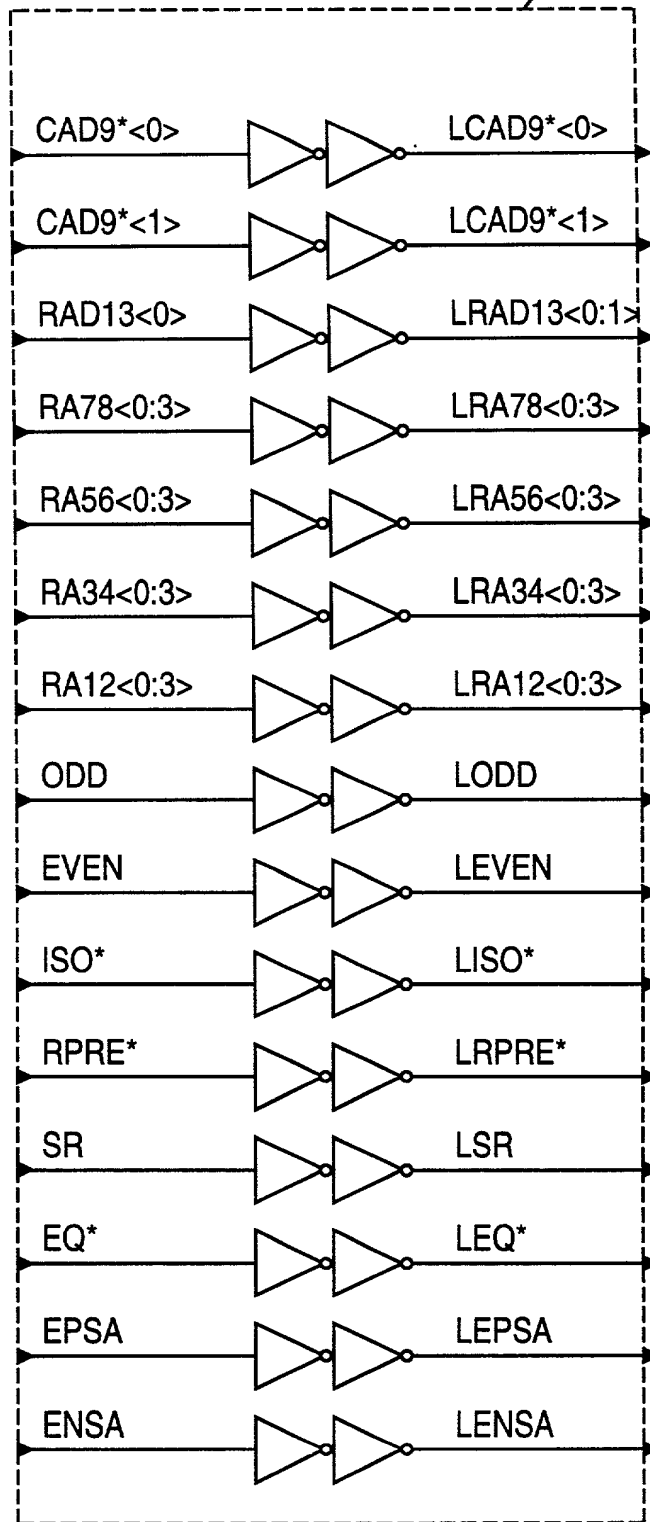


FIG. 65B

**FIG. 66**

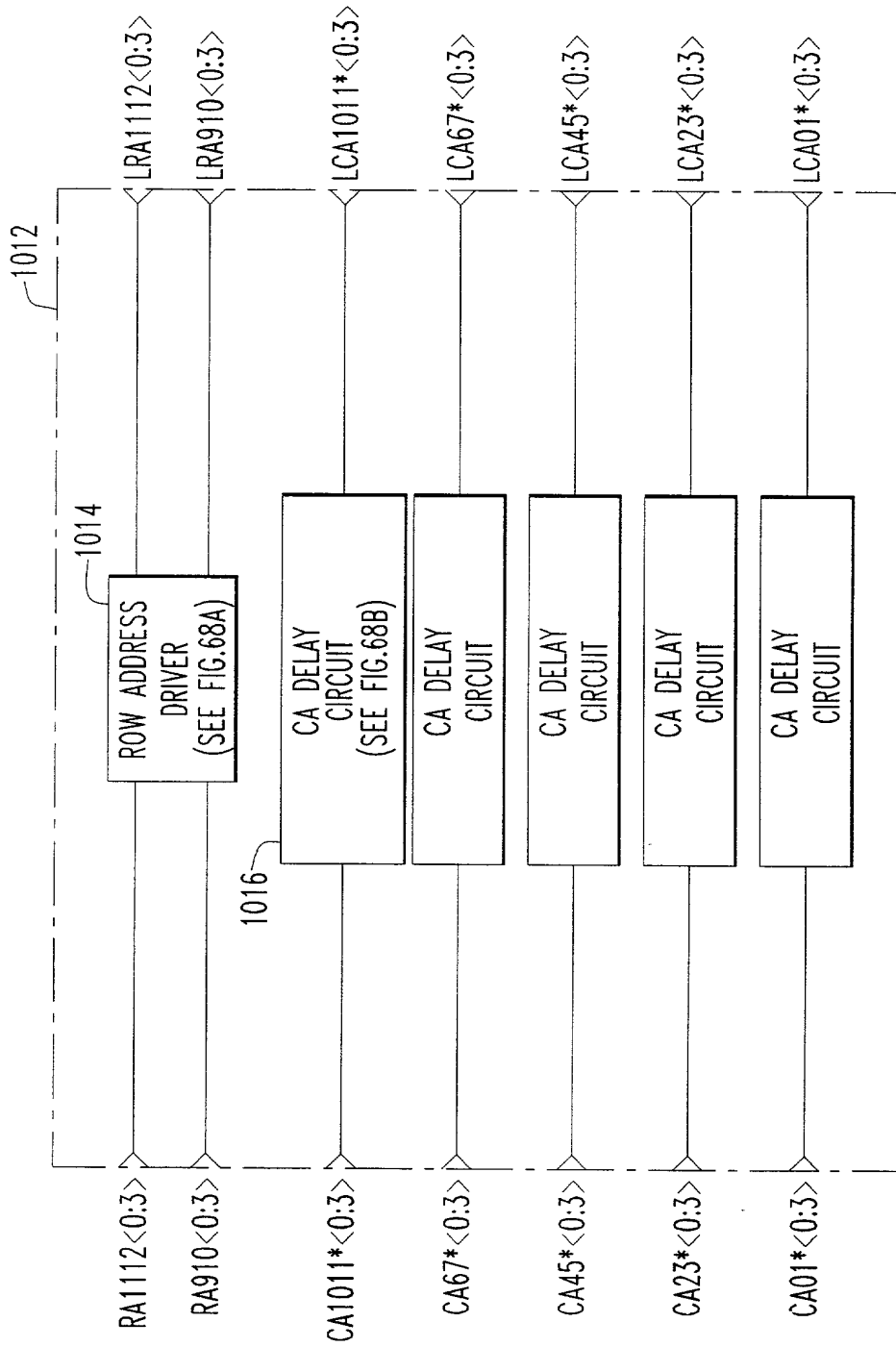
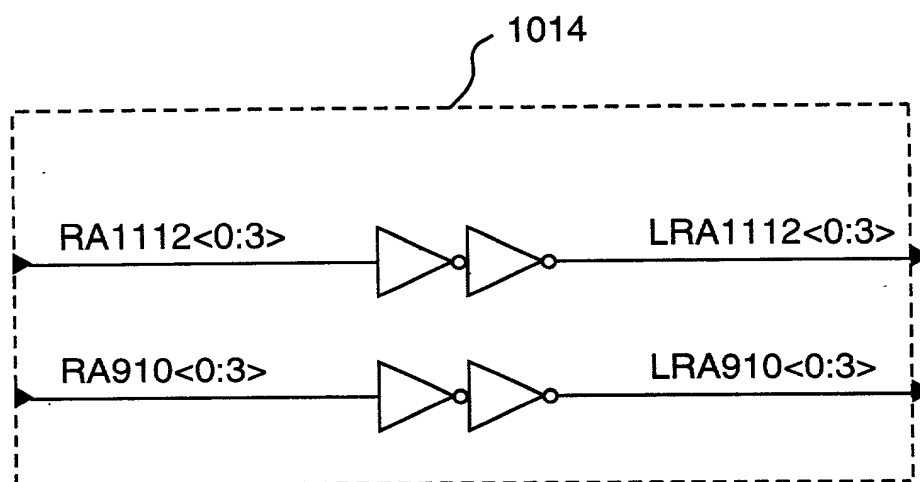


FIG. 67

**FIG. 68A**

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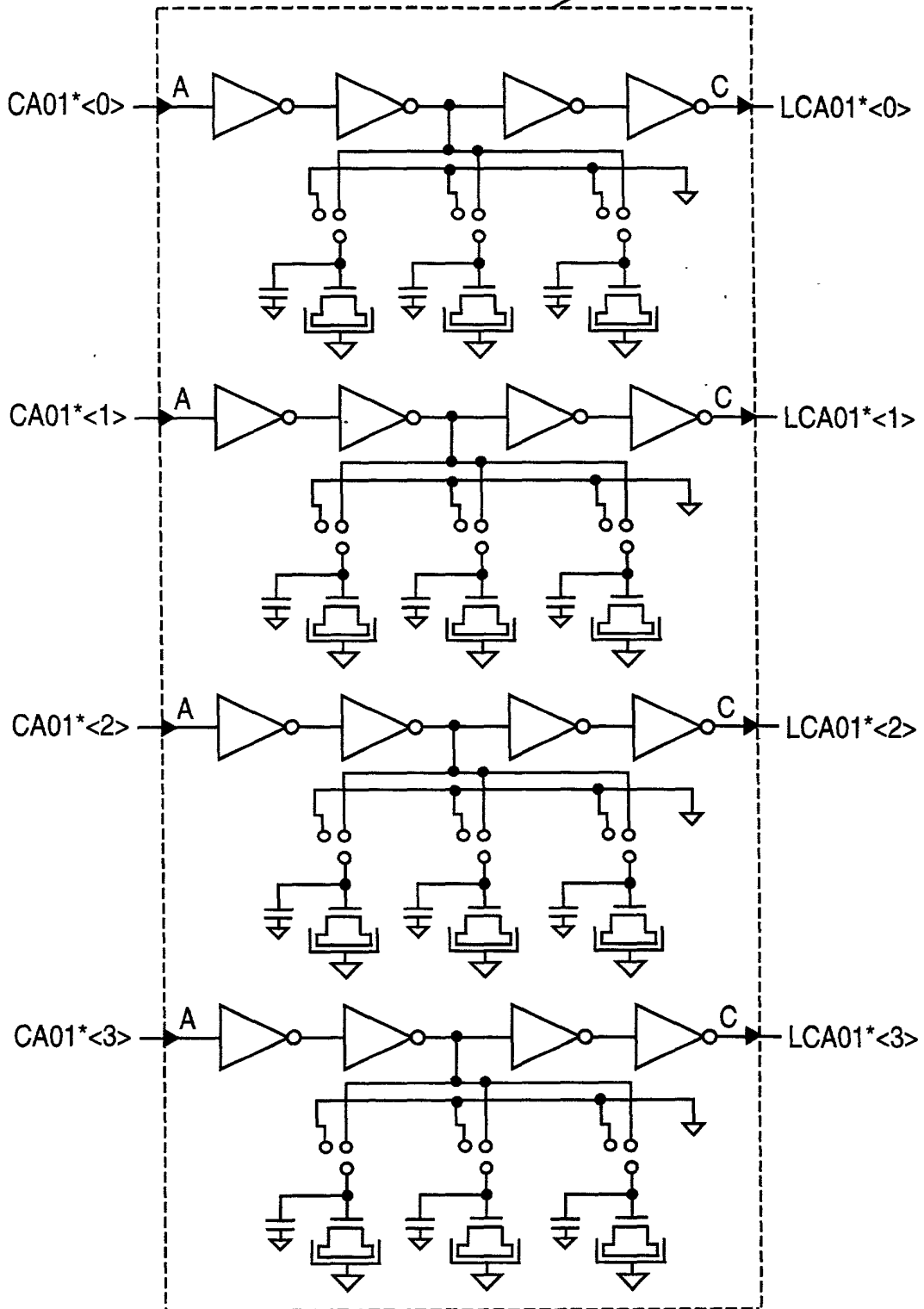


FIG. 68B

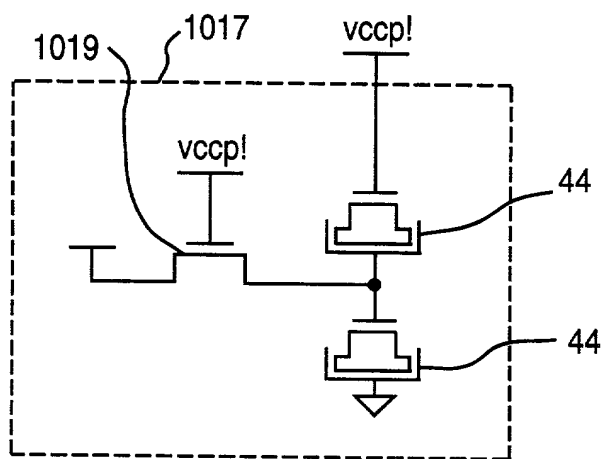


FIG. 69

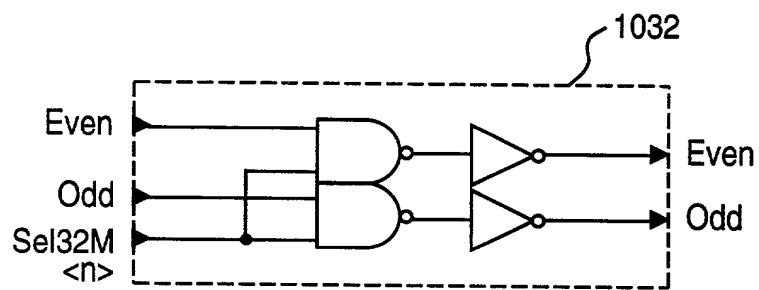


FIG. 70

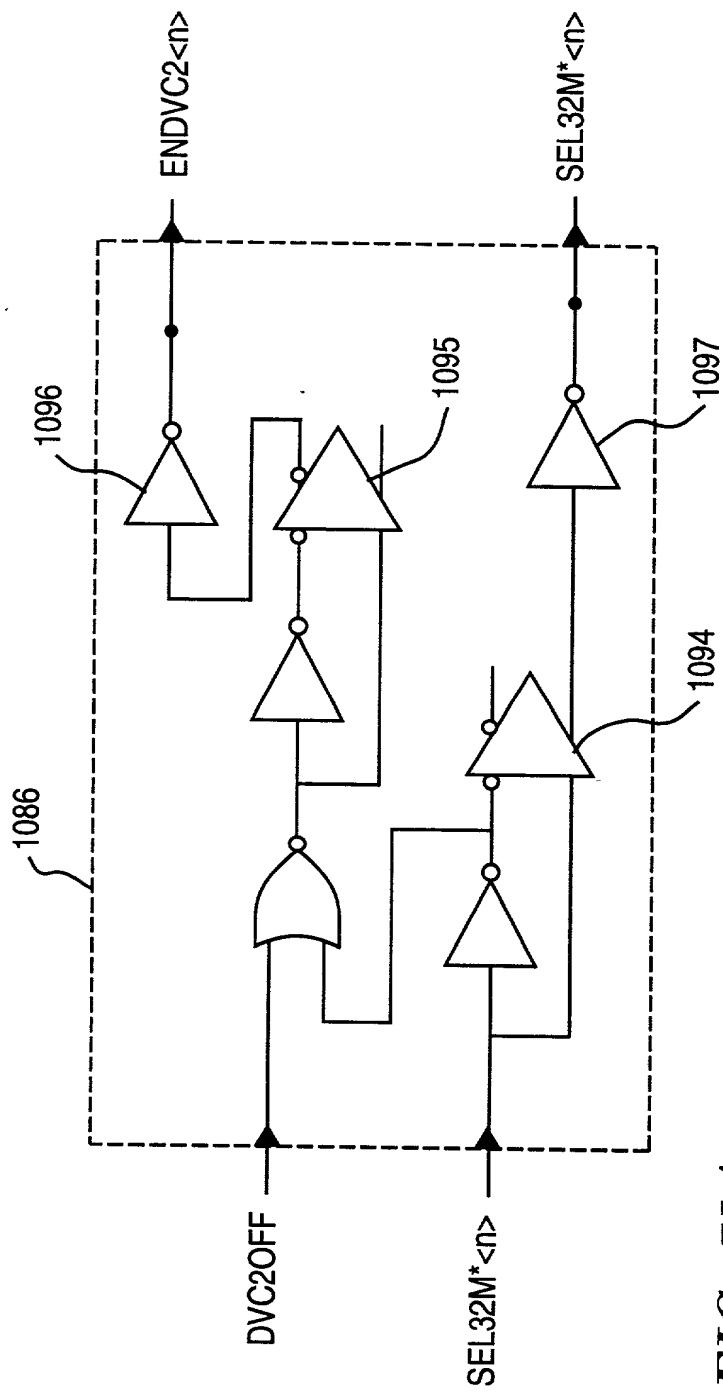
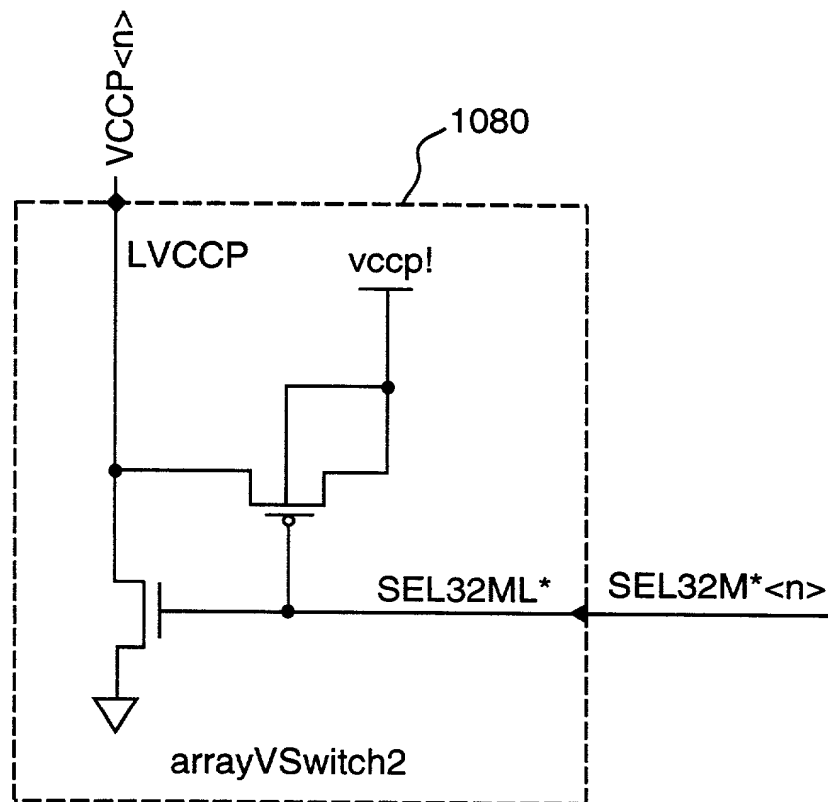
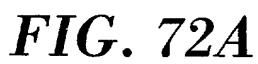
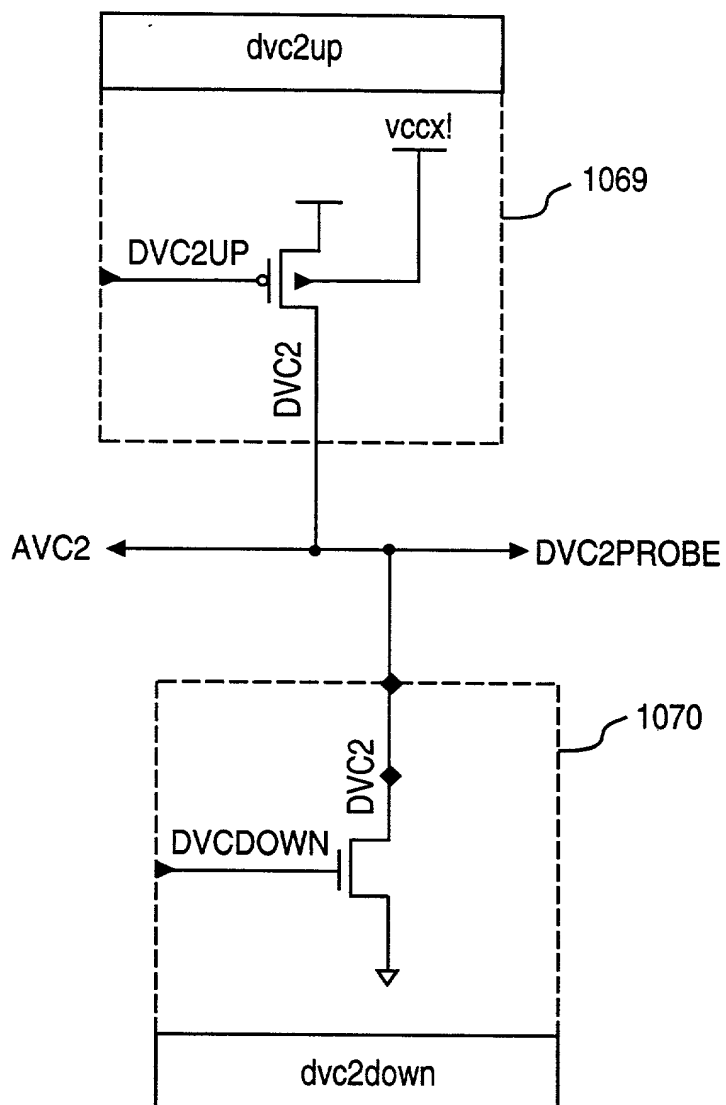
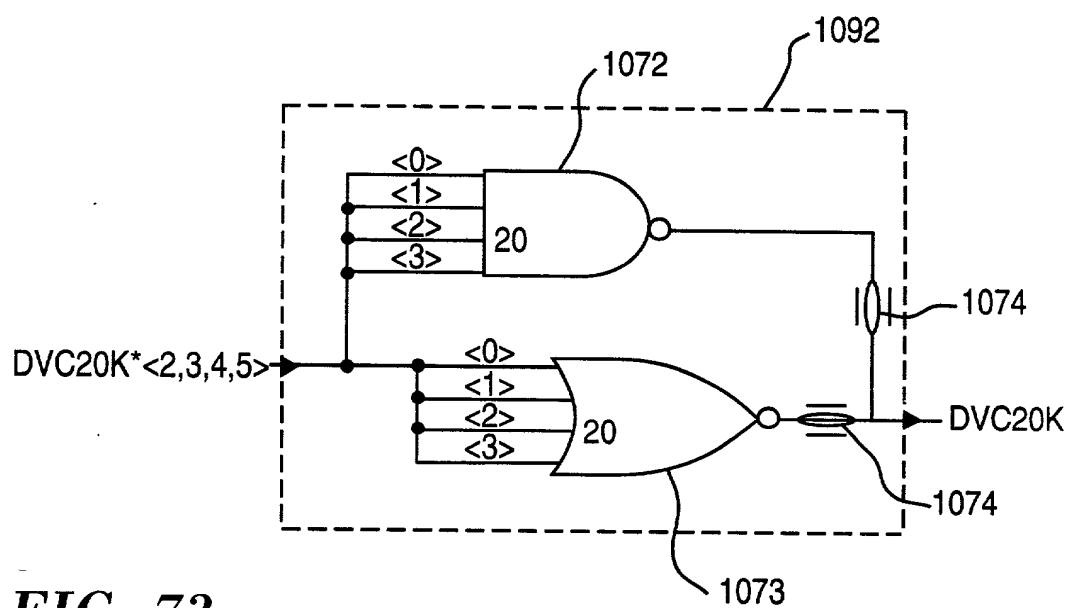


FIG. 71A

**FIG. 71B**



**FIG. 72B**

**FIG. 73**

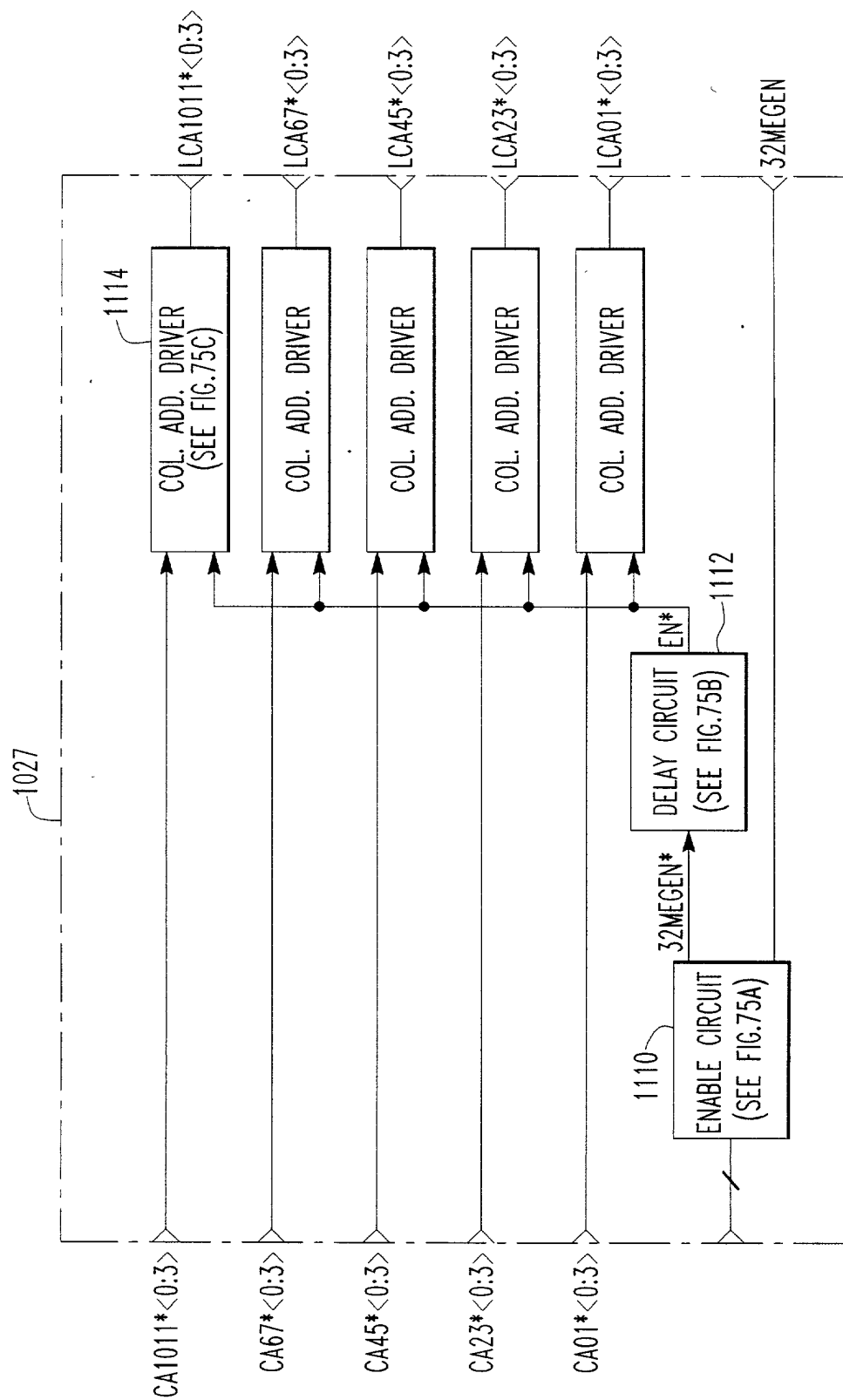


FIG. 74

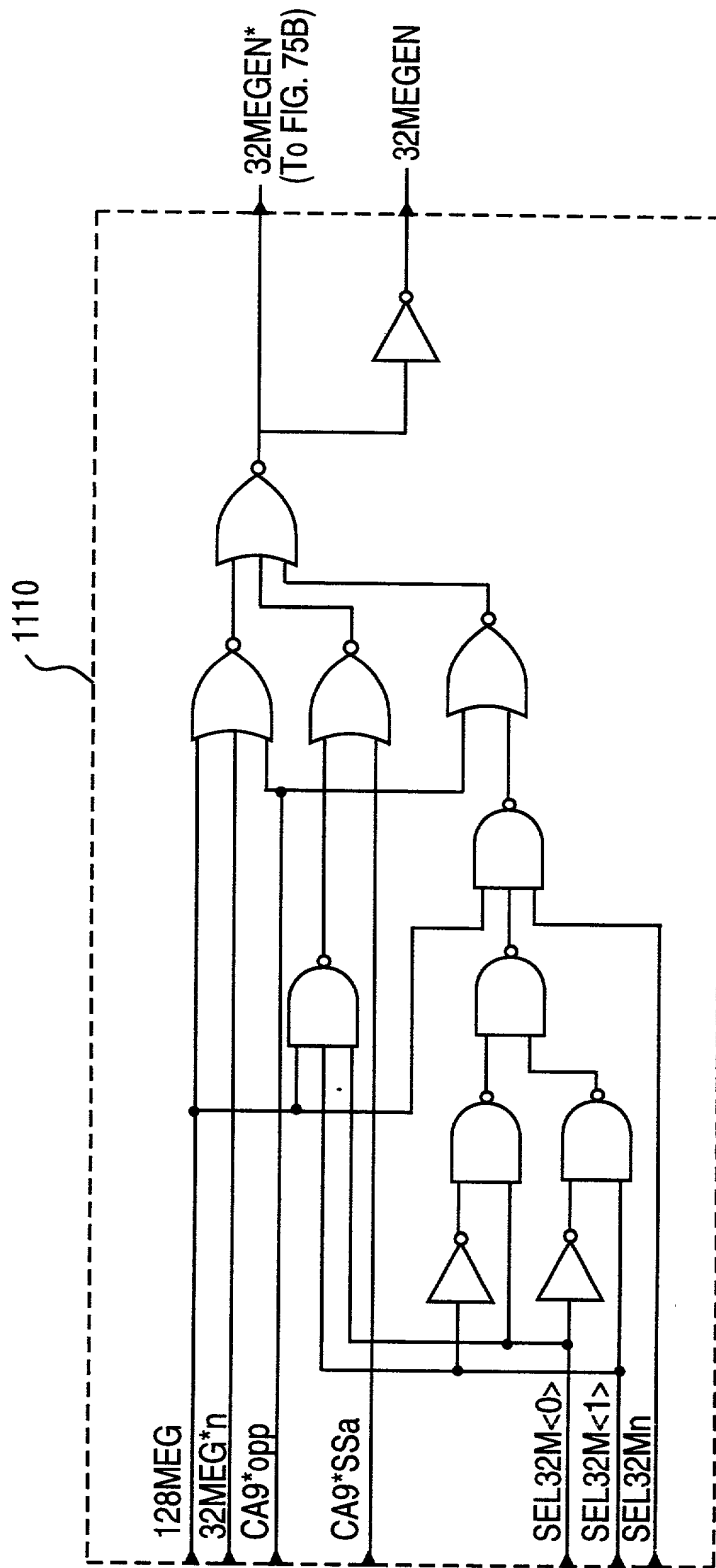


FIG. 75A

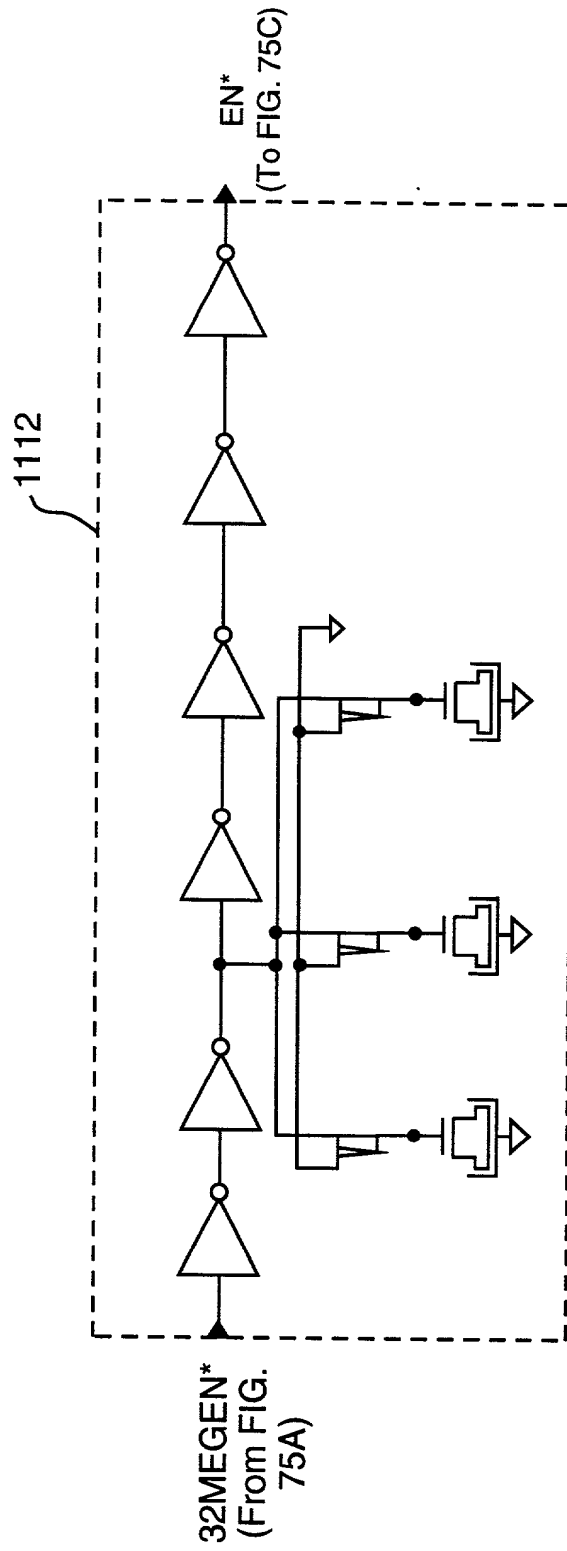


FIG. 75B

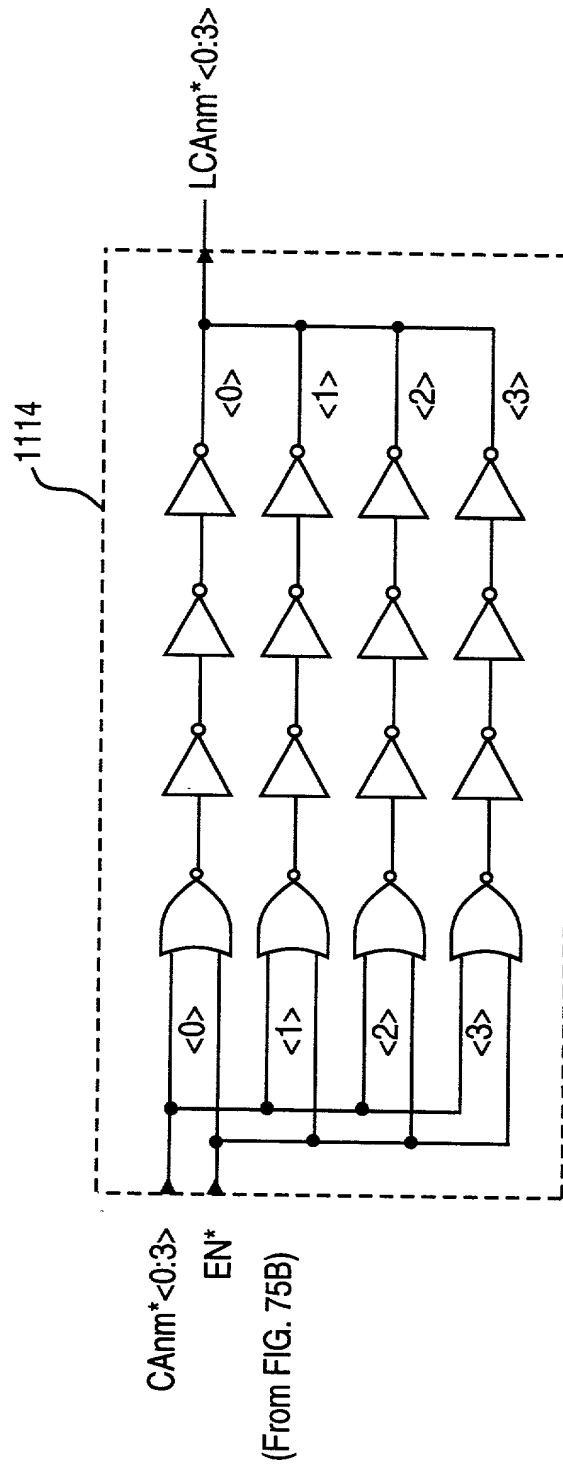


FIG. 75C

(From FIG. 75B)

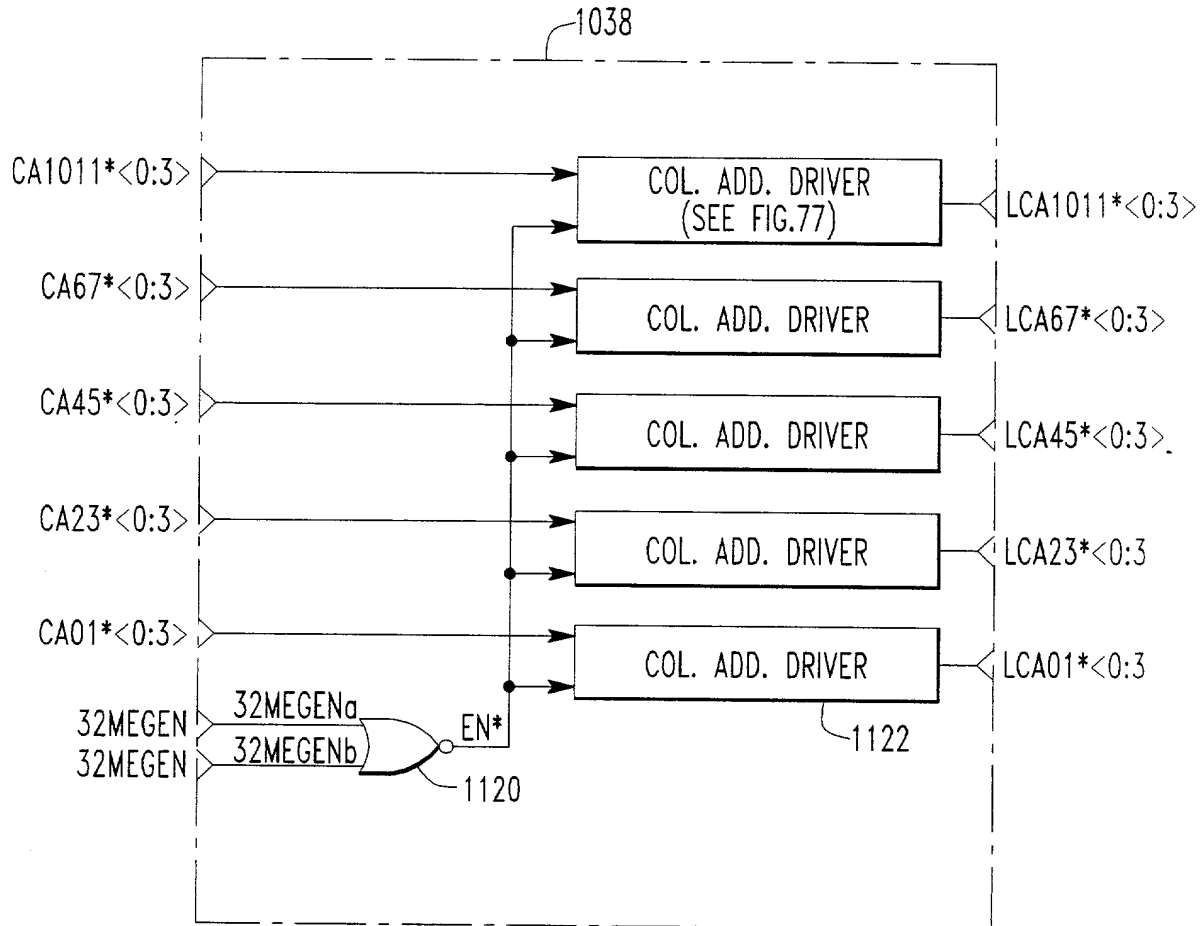


FIG. 76

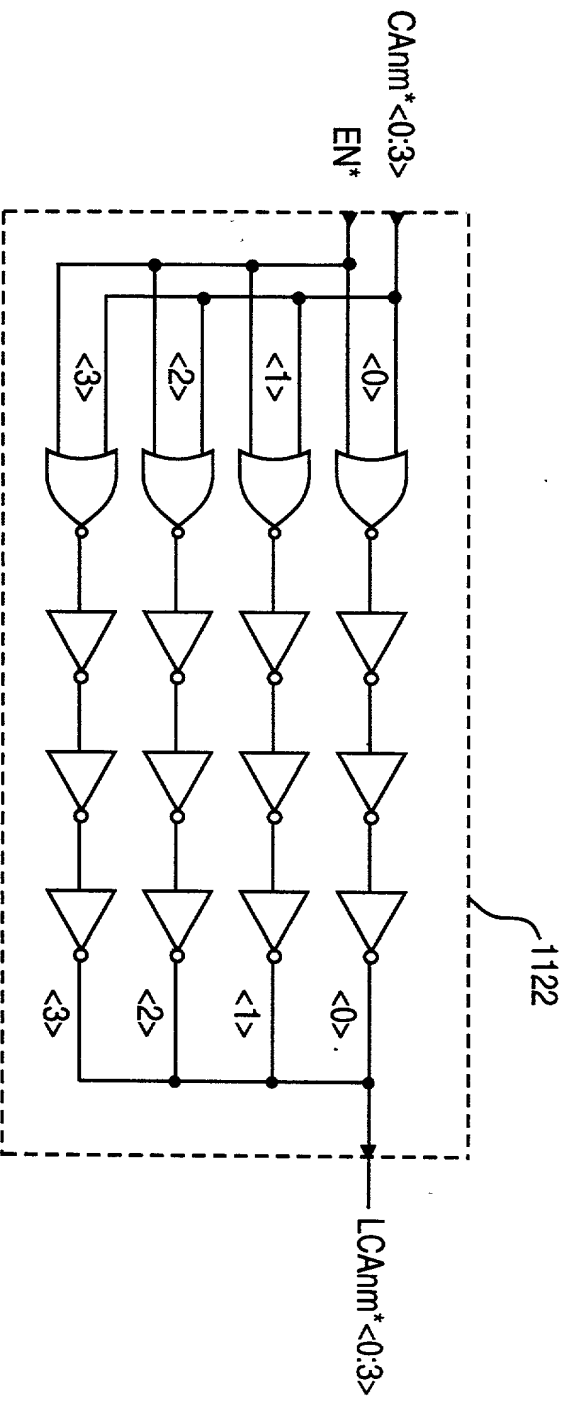


FIG. 77

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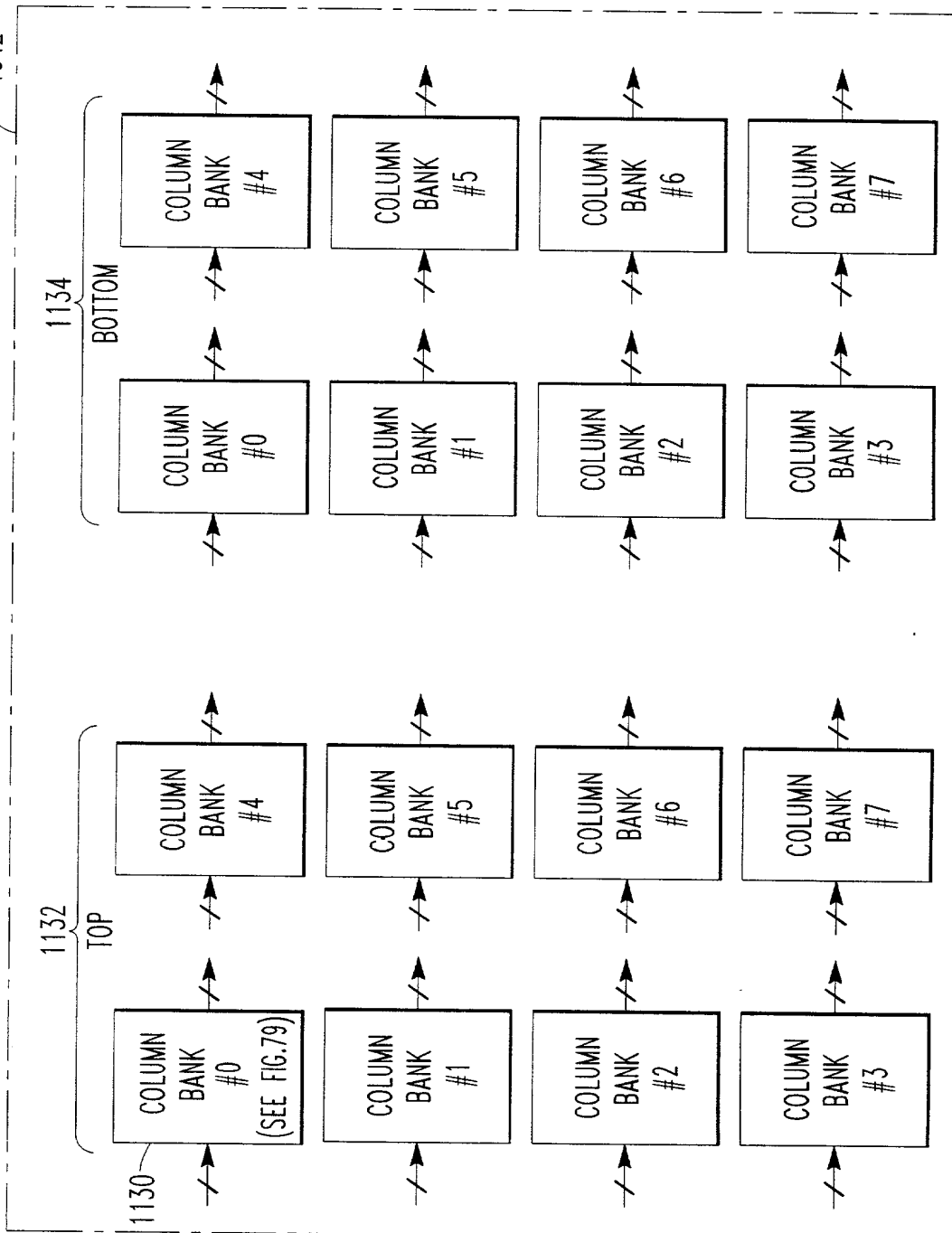


FIG. 78

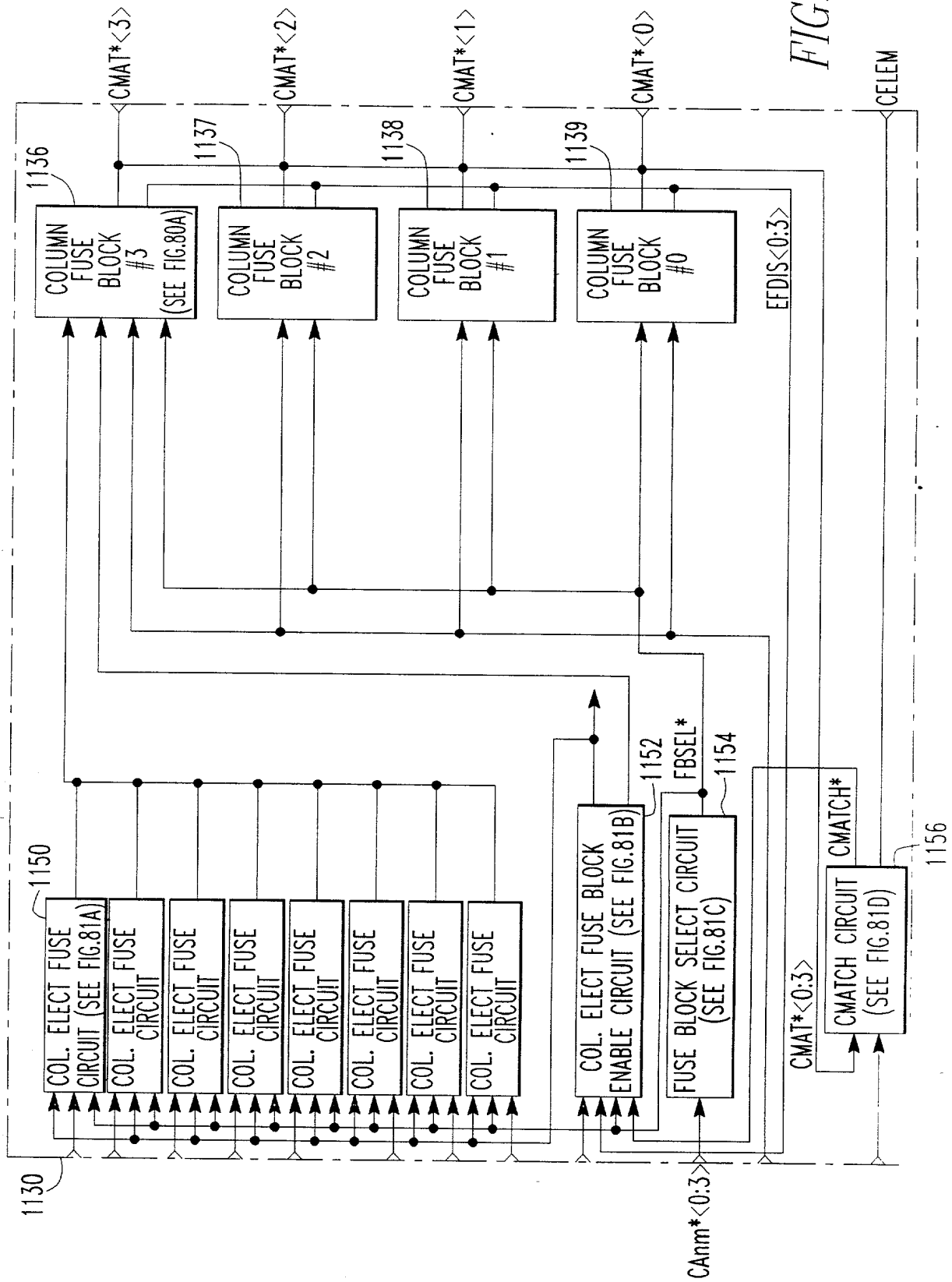


FIG. 79

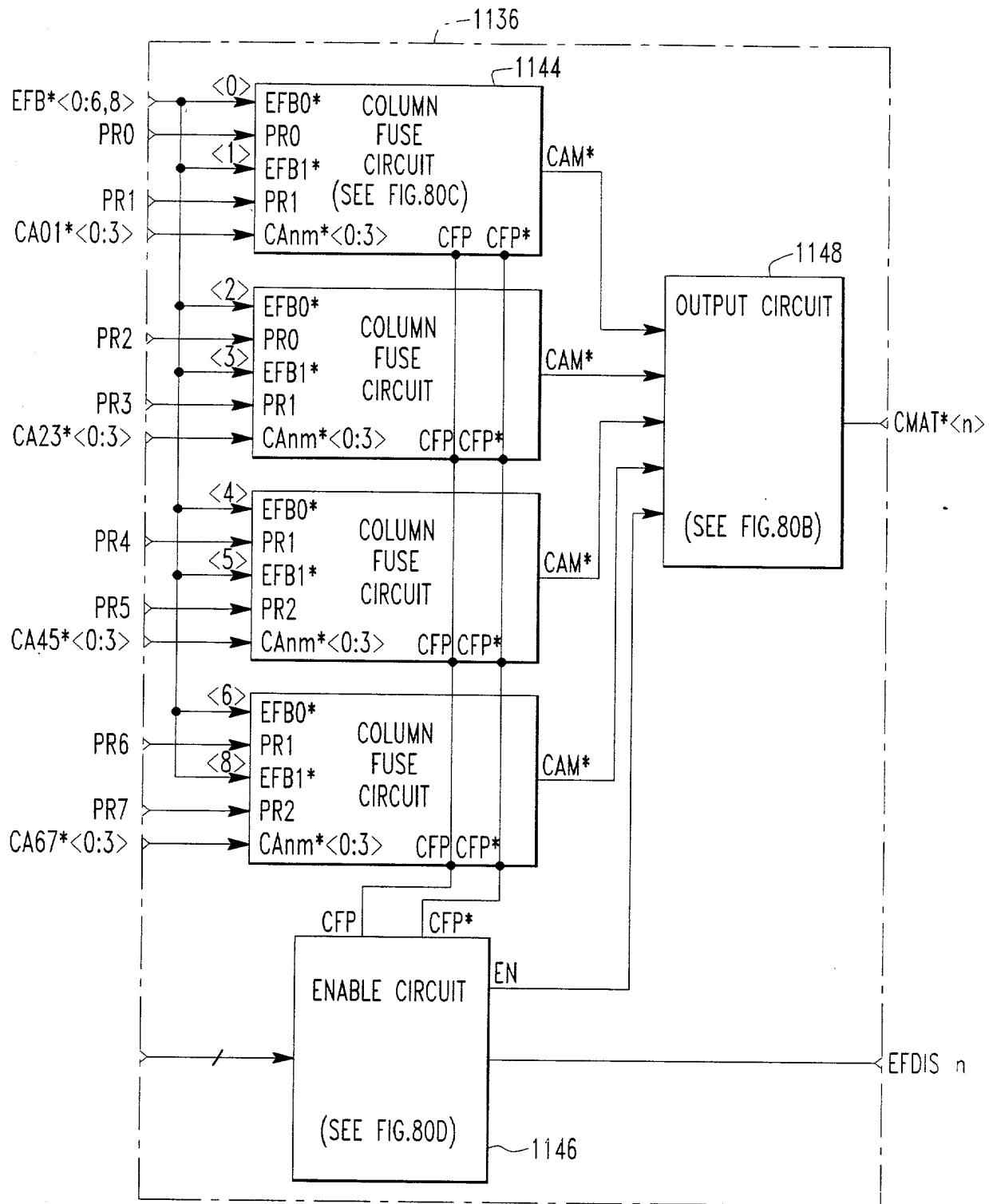
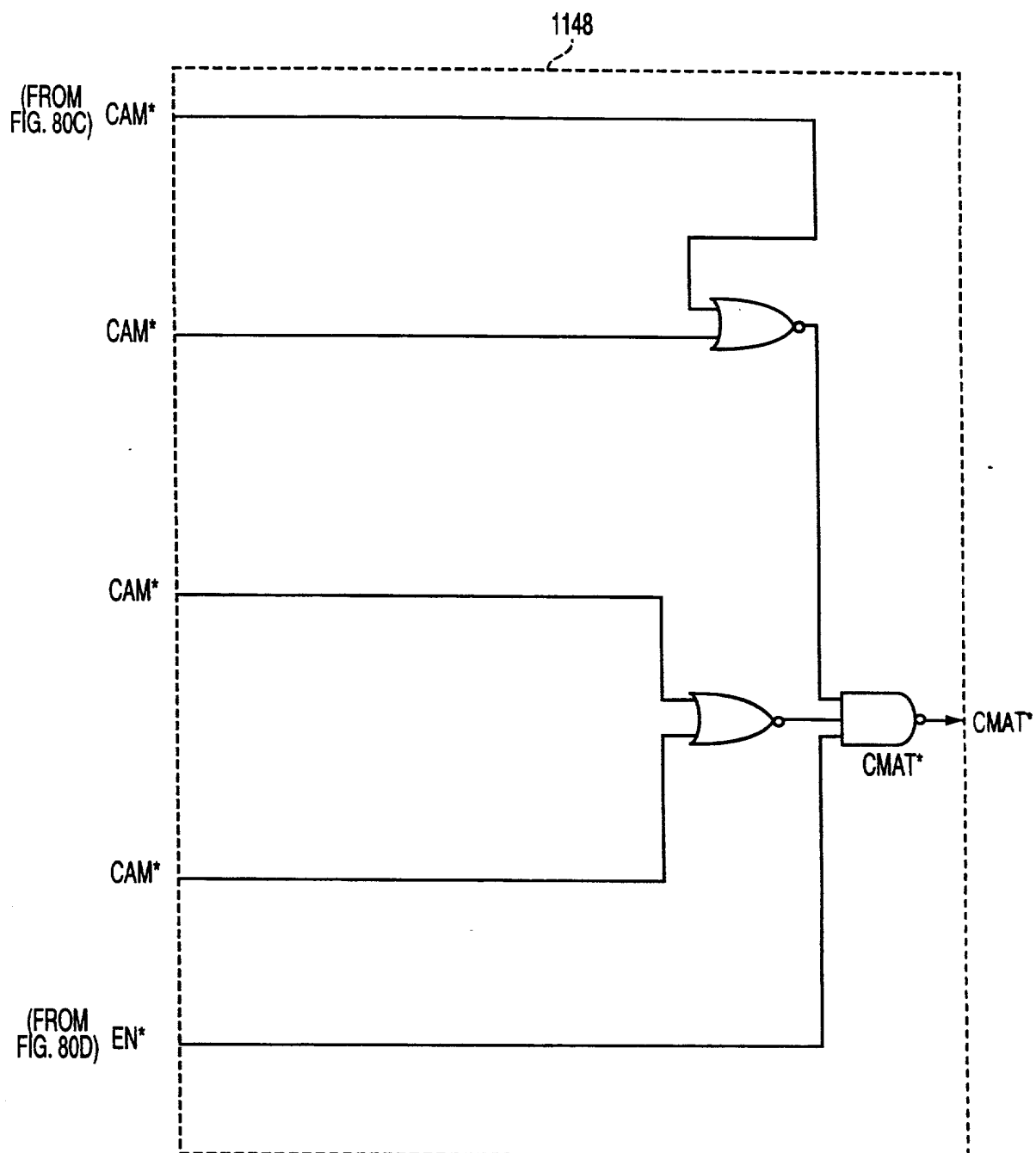


FIG. 80A

**FIG. 80B**

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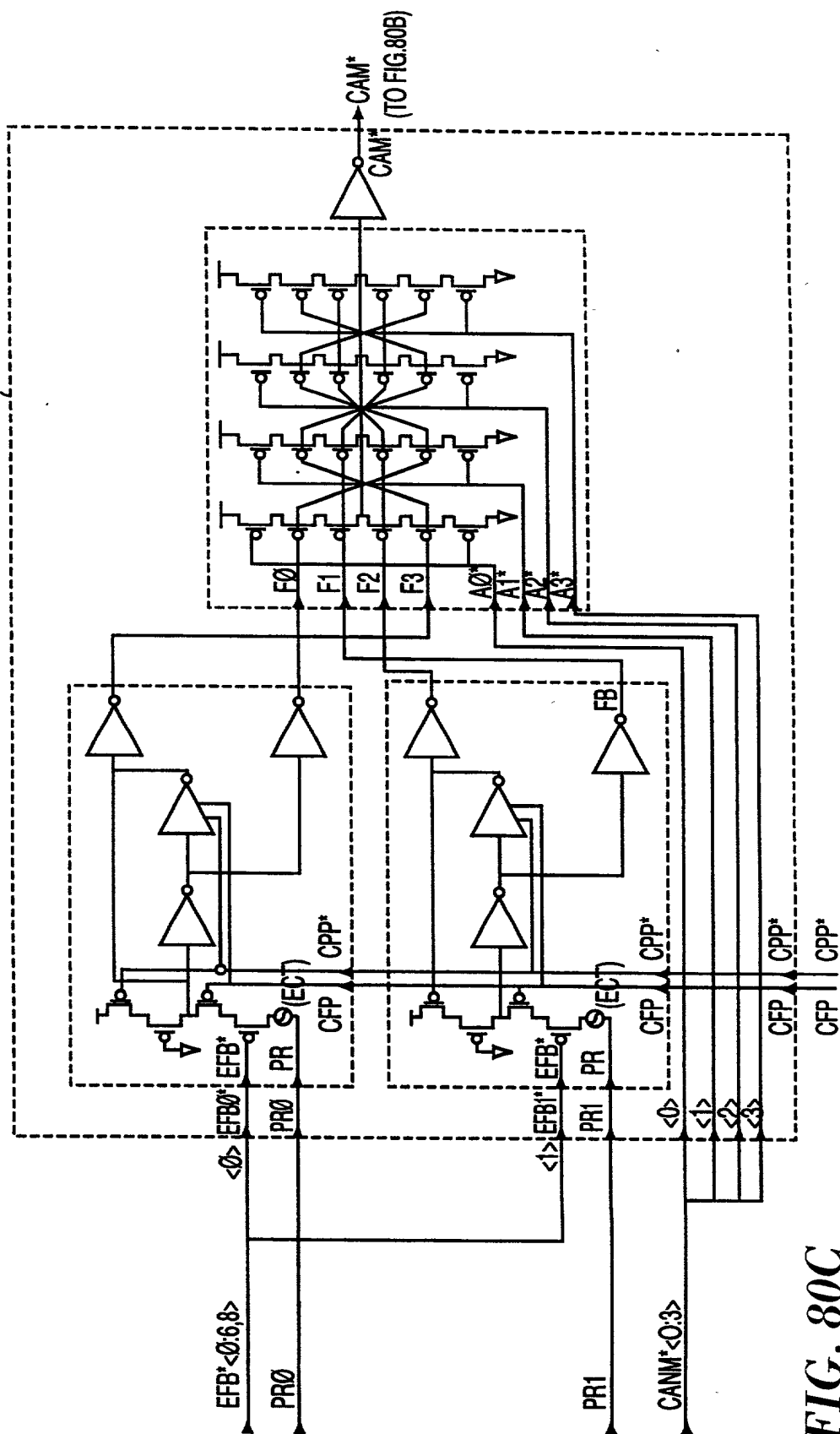


FIG. 80C

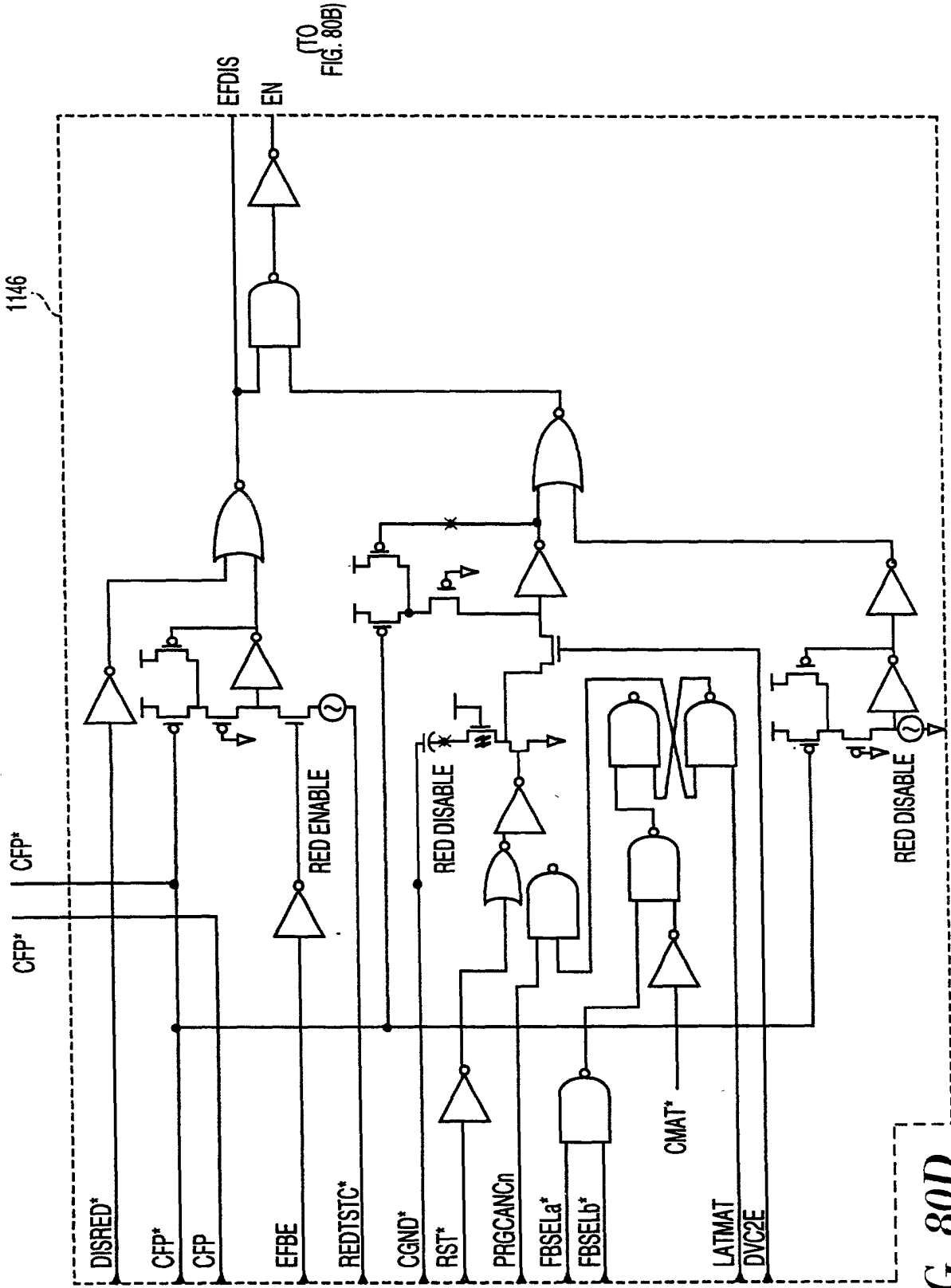


FIG. 80D

FIG. 80D

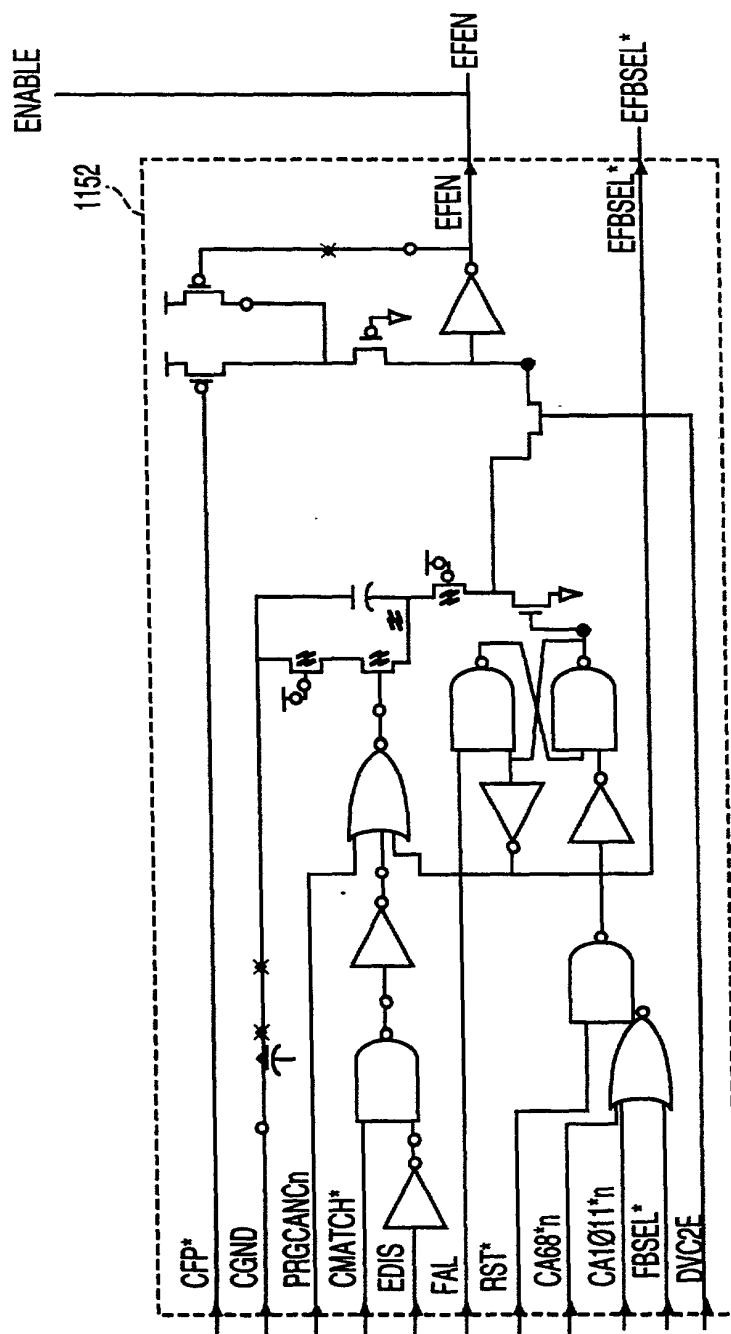


FIG. 81B

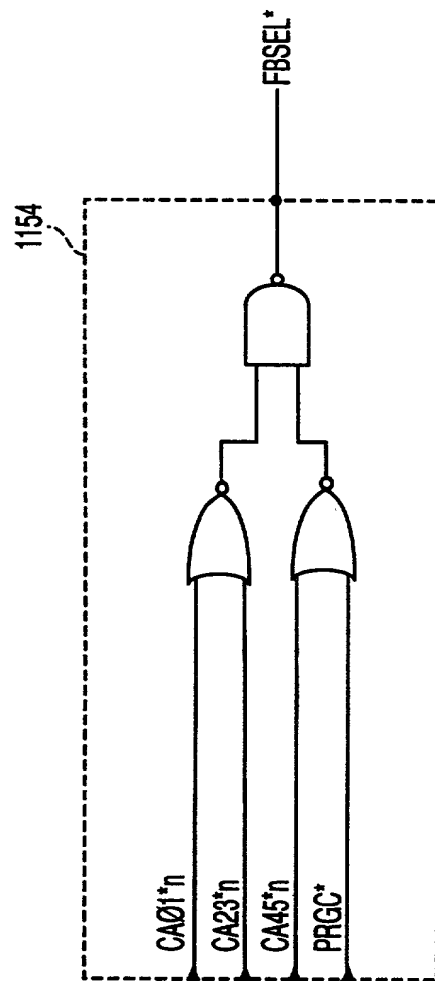


FIG. 81C

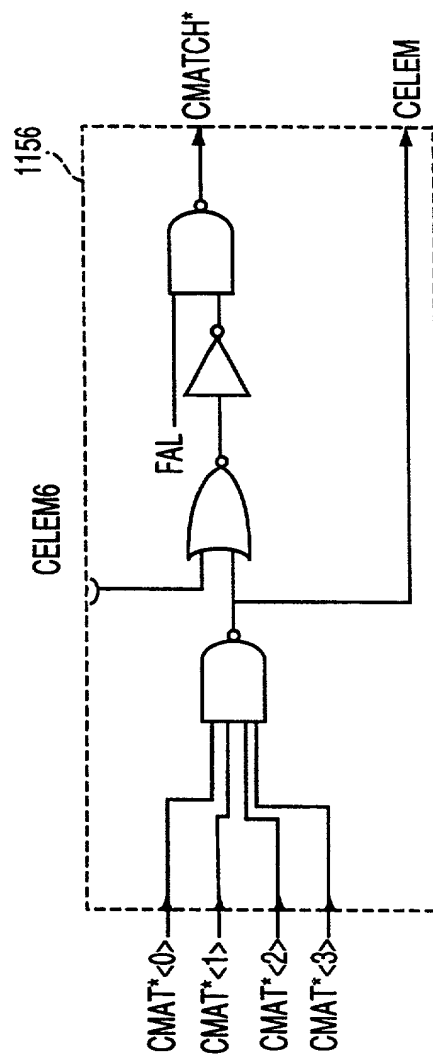


FIG. 81D

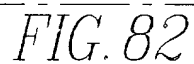


FIG. 82

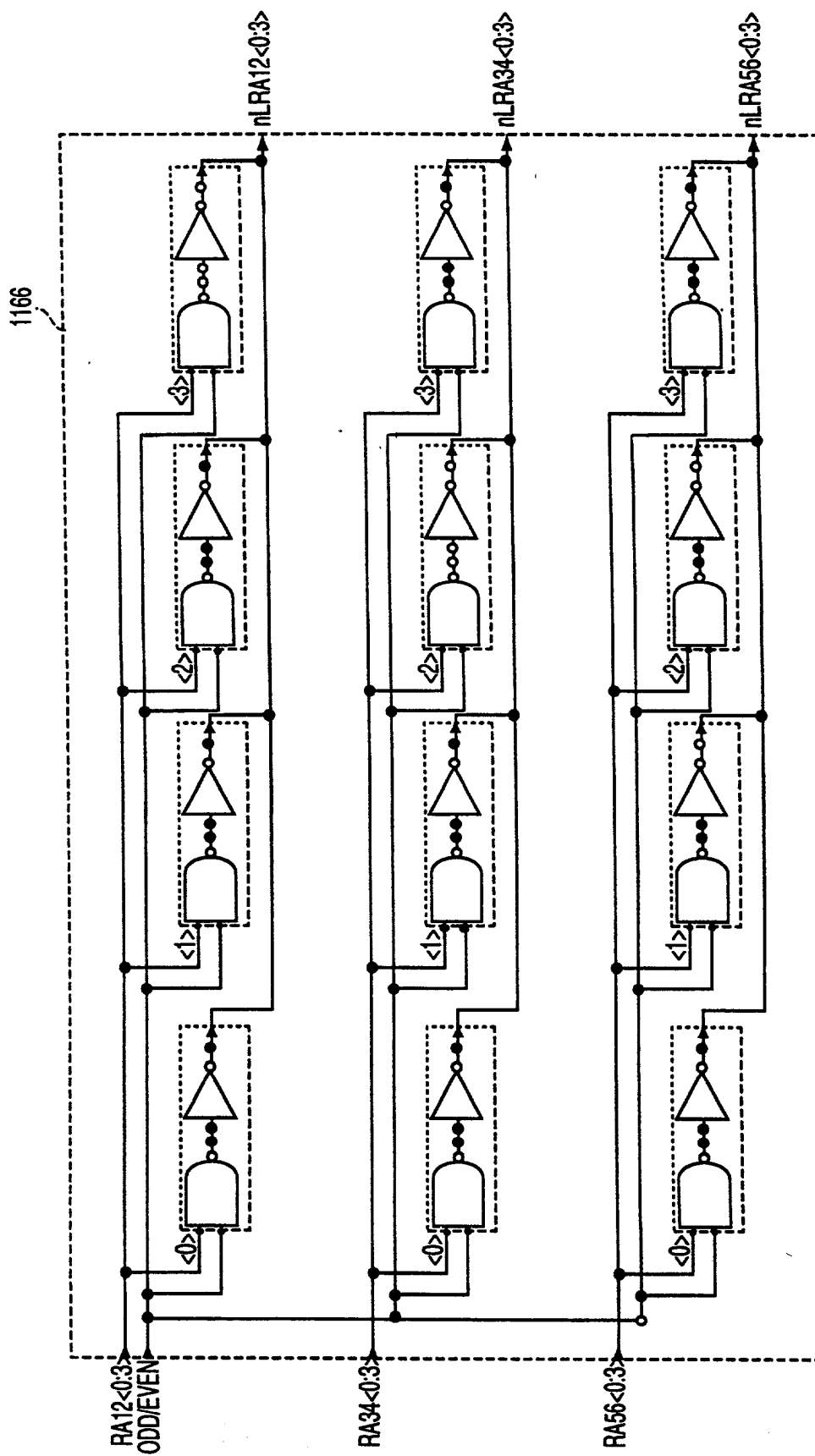


FIG. 83A

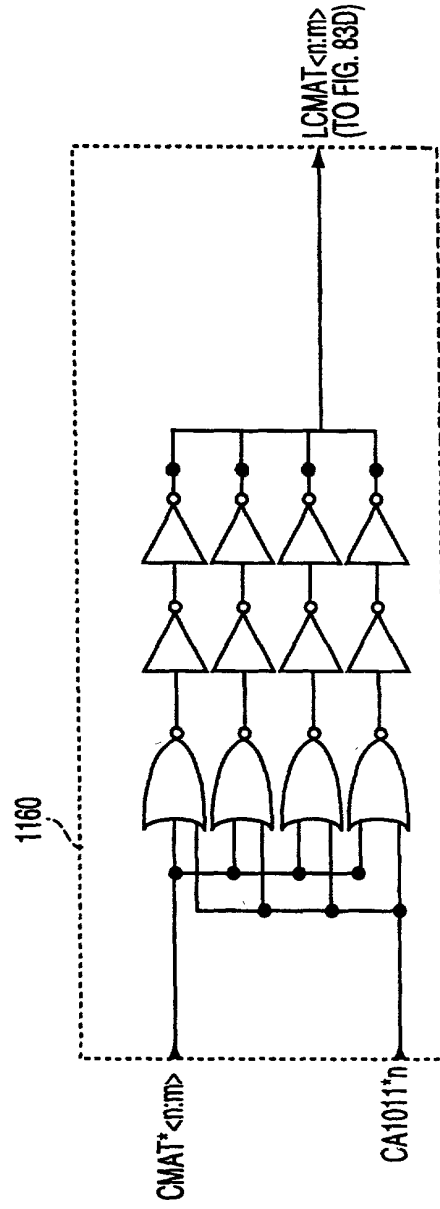


FIG. 83B

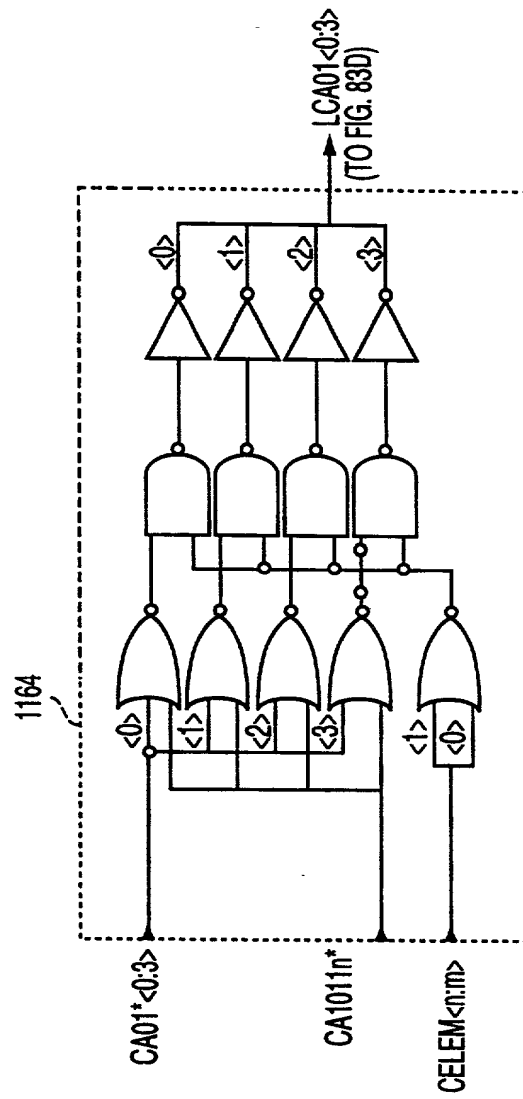
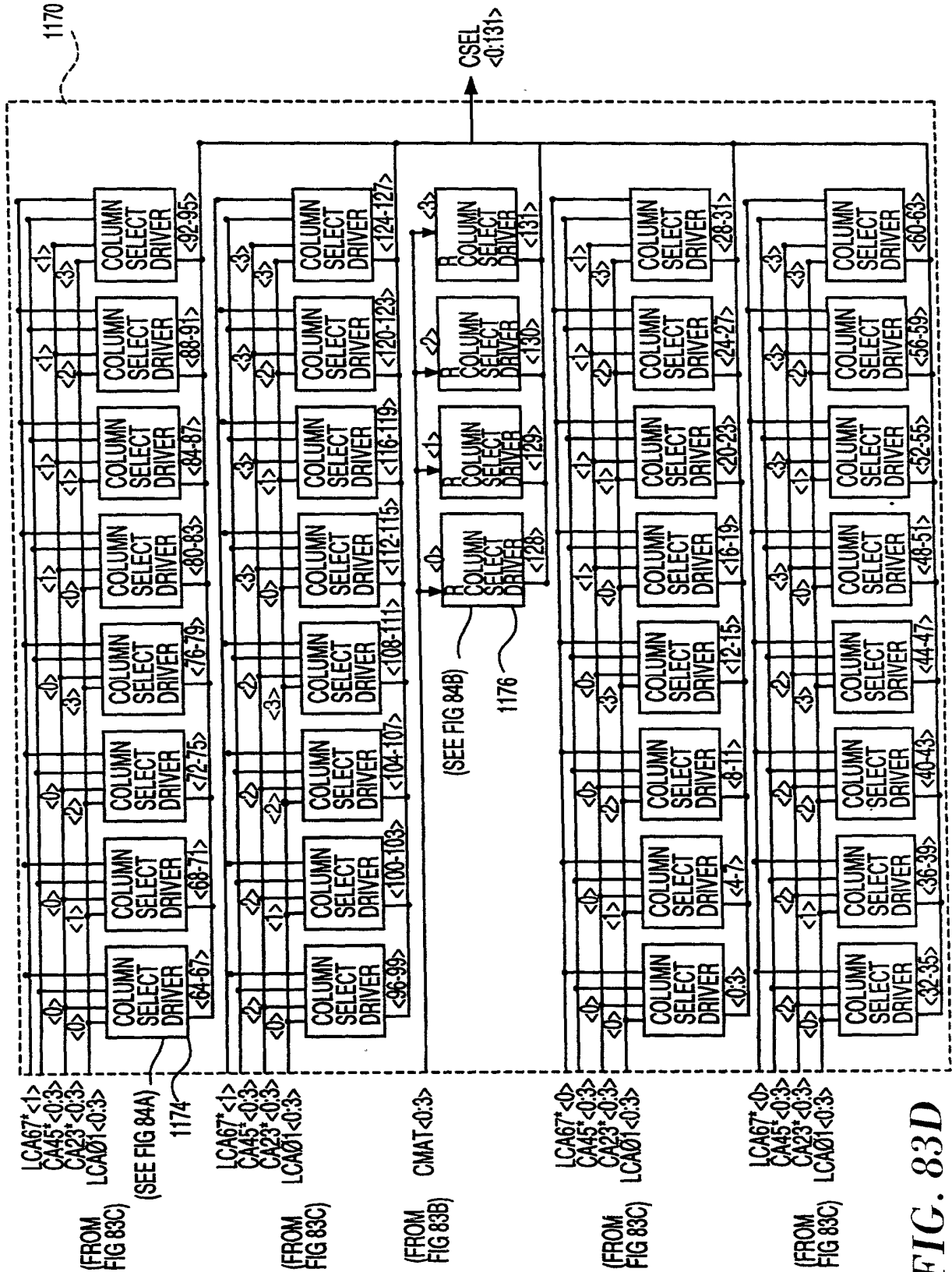
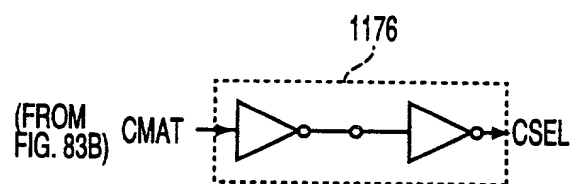


FIG. 83C



**FIG. 84B**

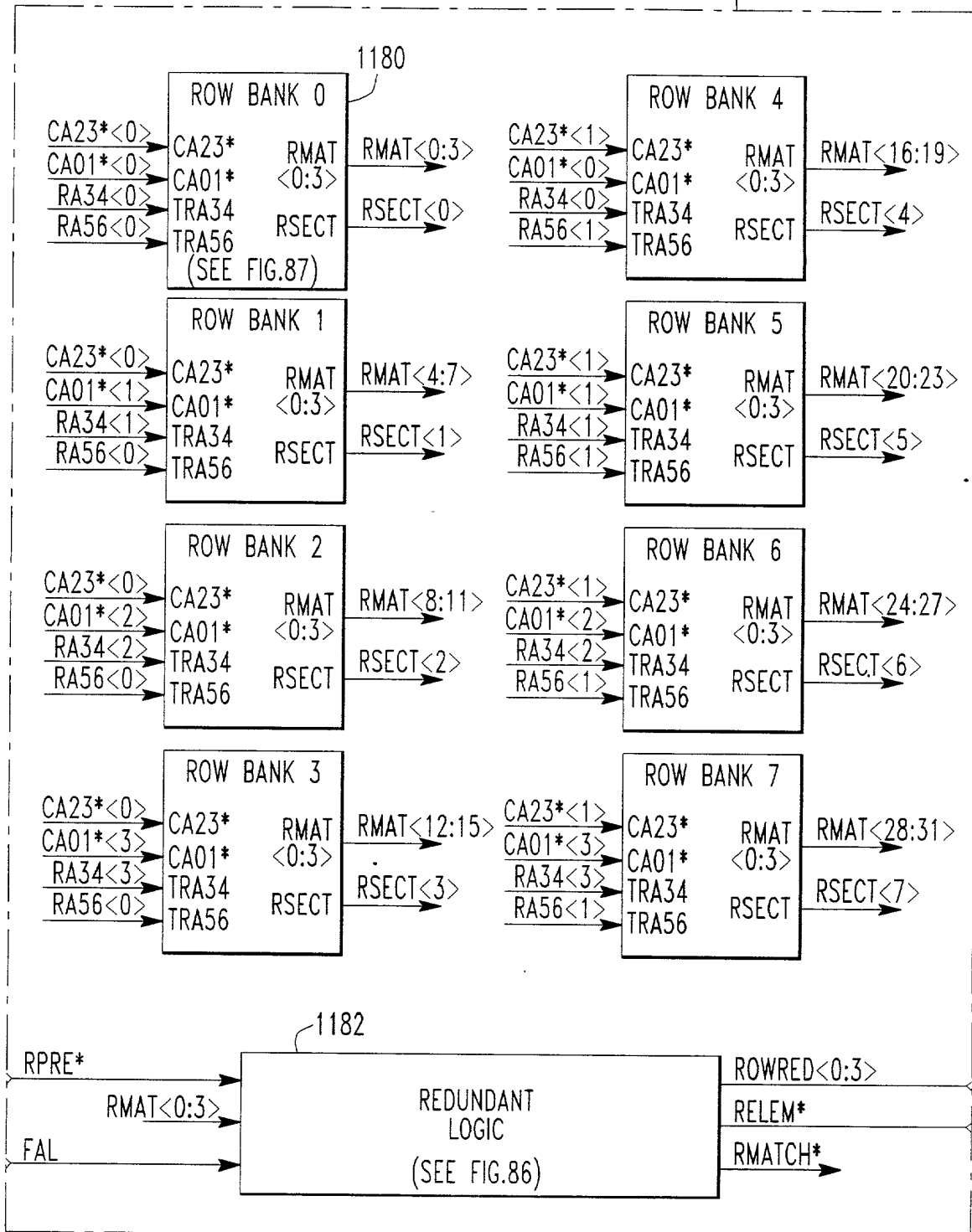


FIG. 85

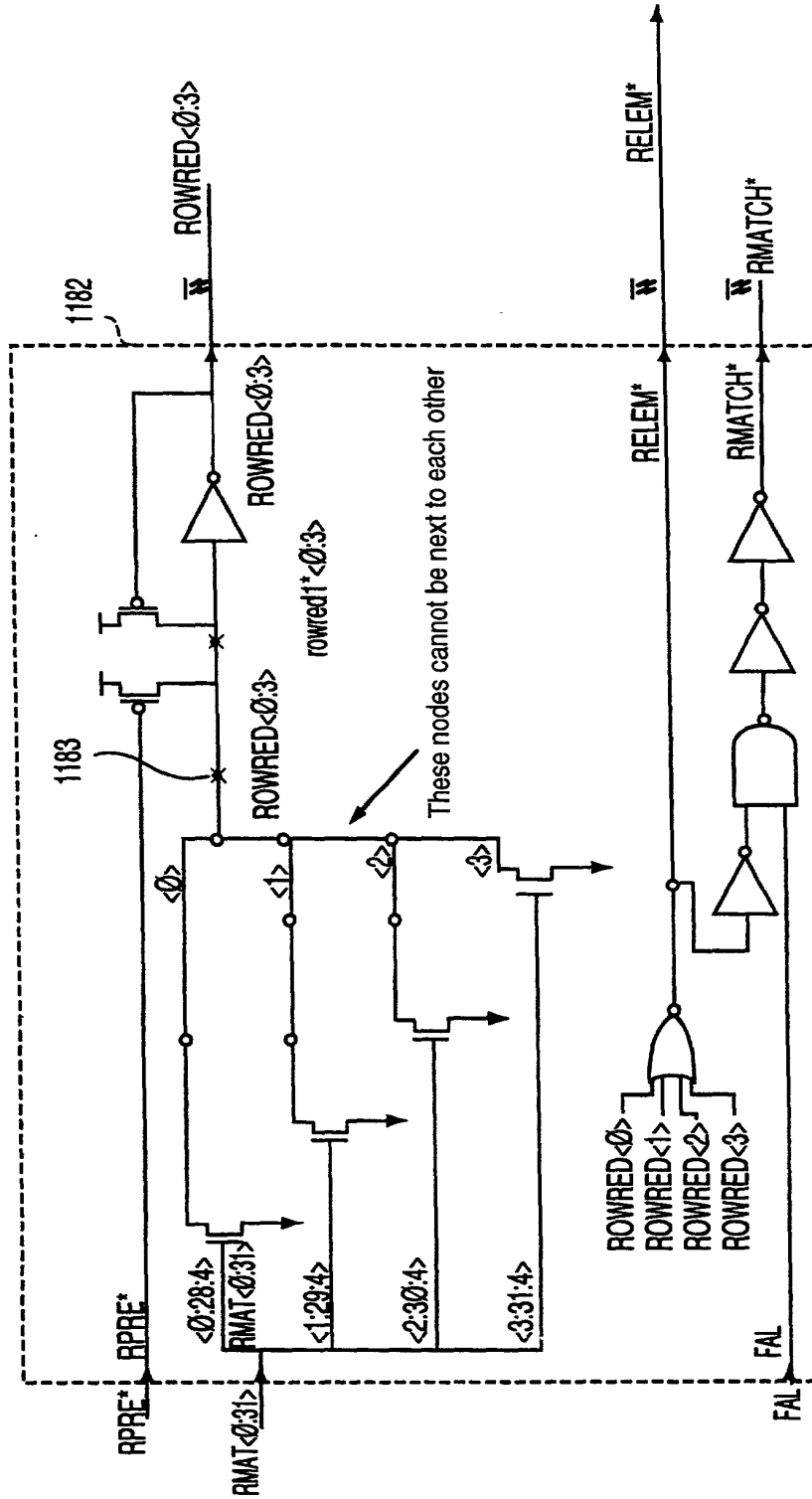


FIG. 86

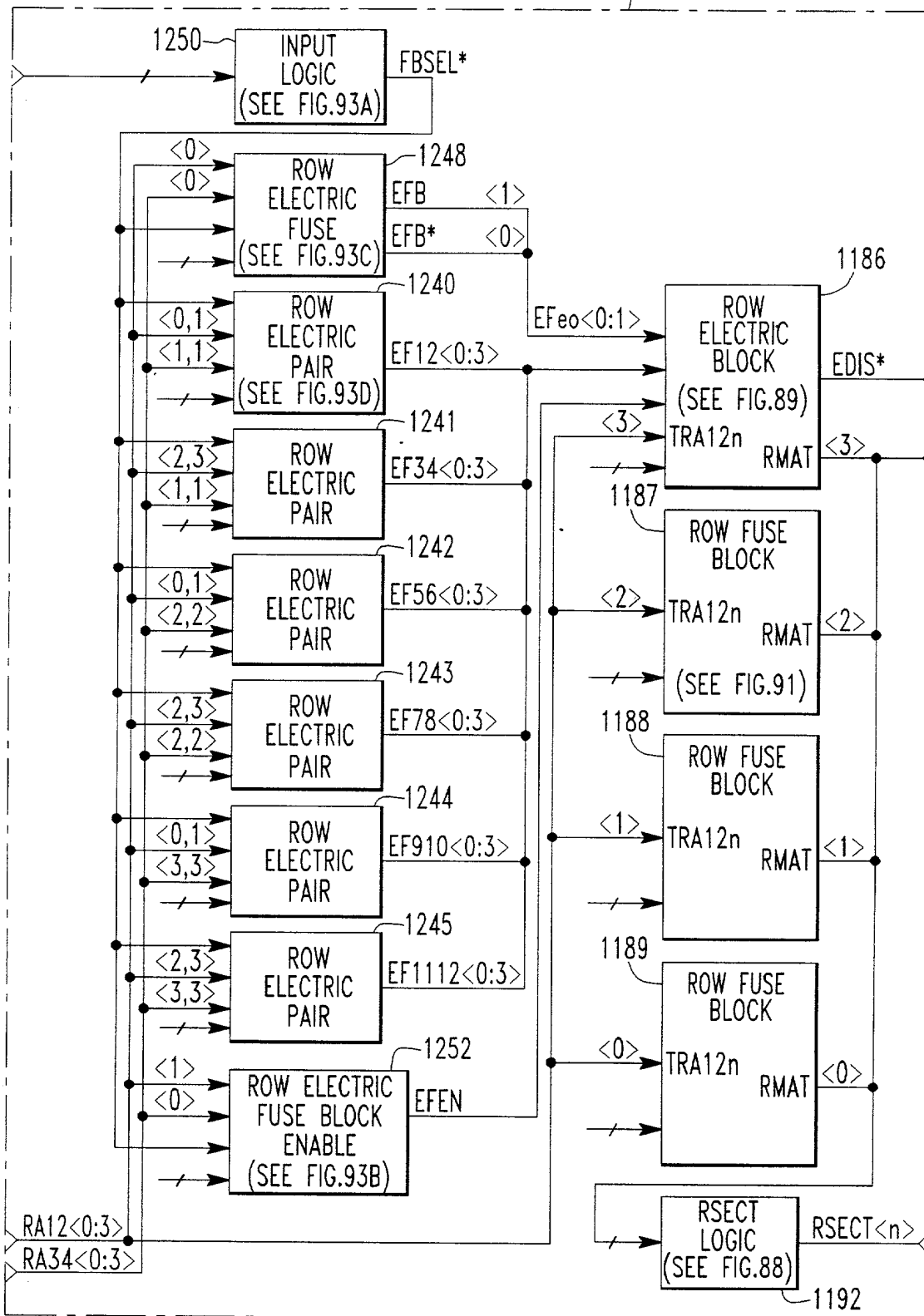
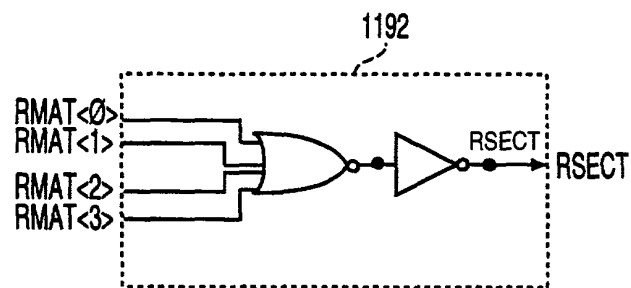


FIG. 87

**FIG. 88**

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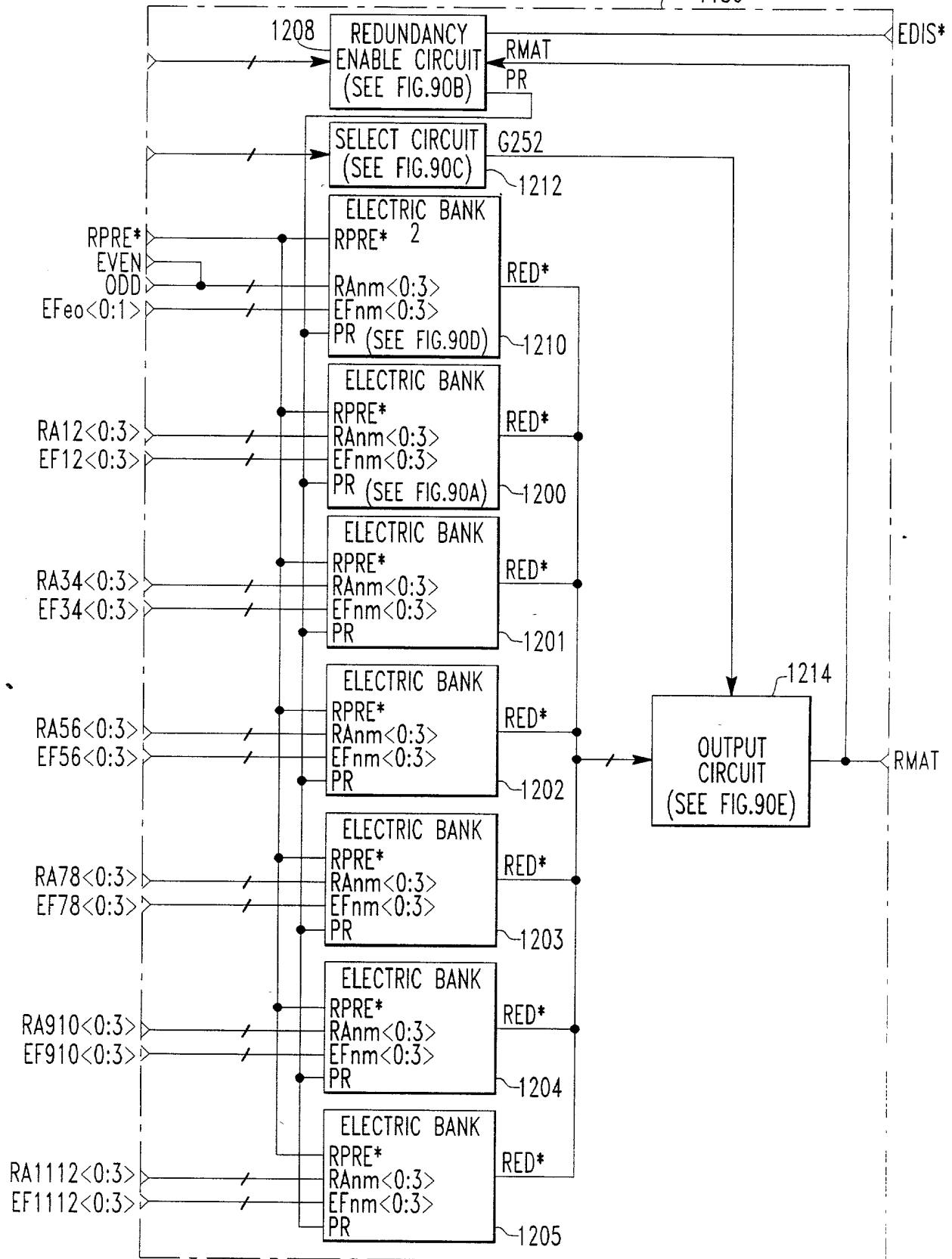
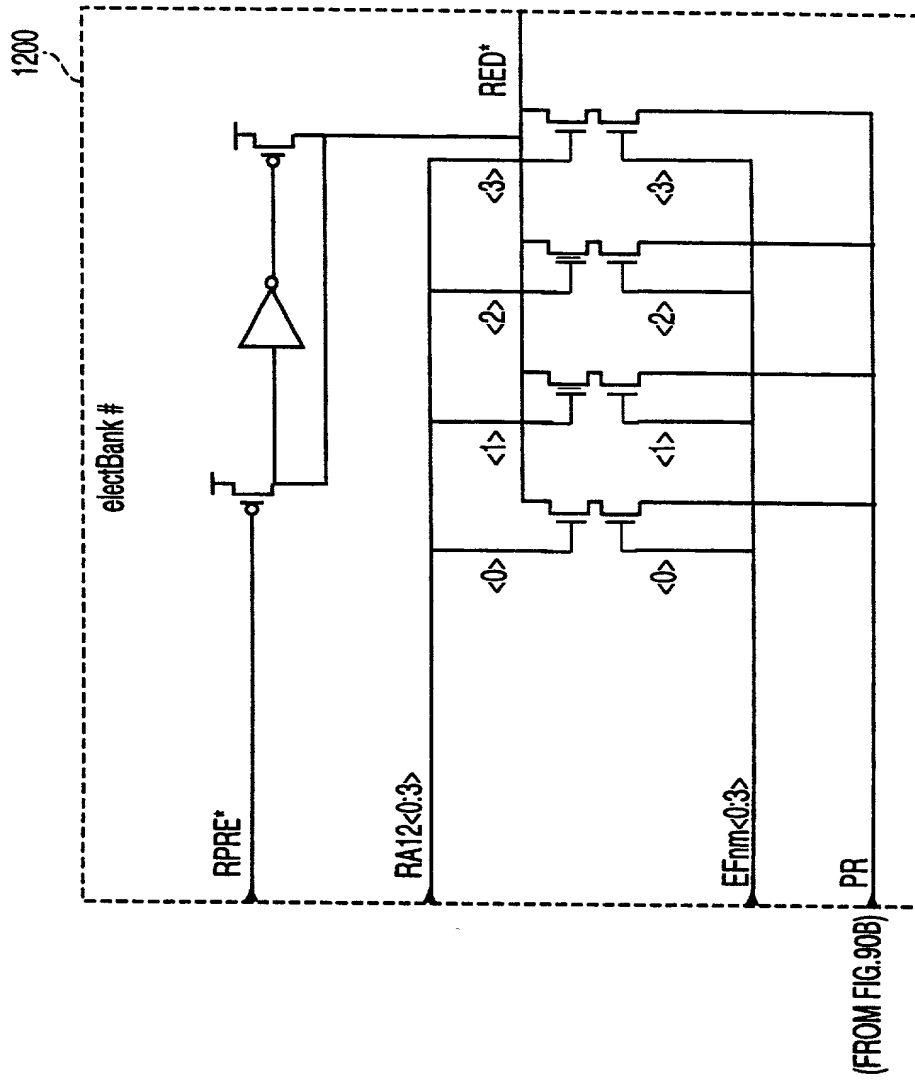


FIG. 89



(FROM FIG. 90B)

FIG. 90A

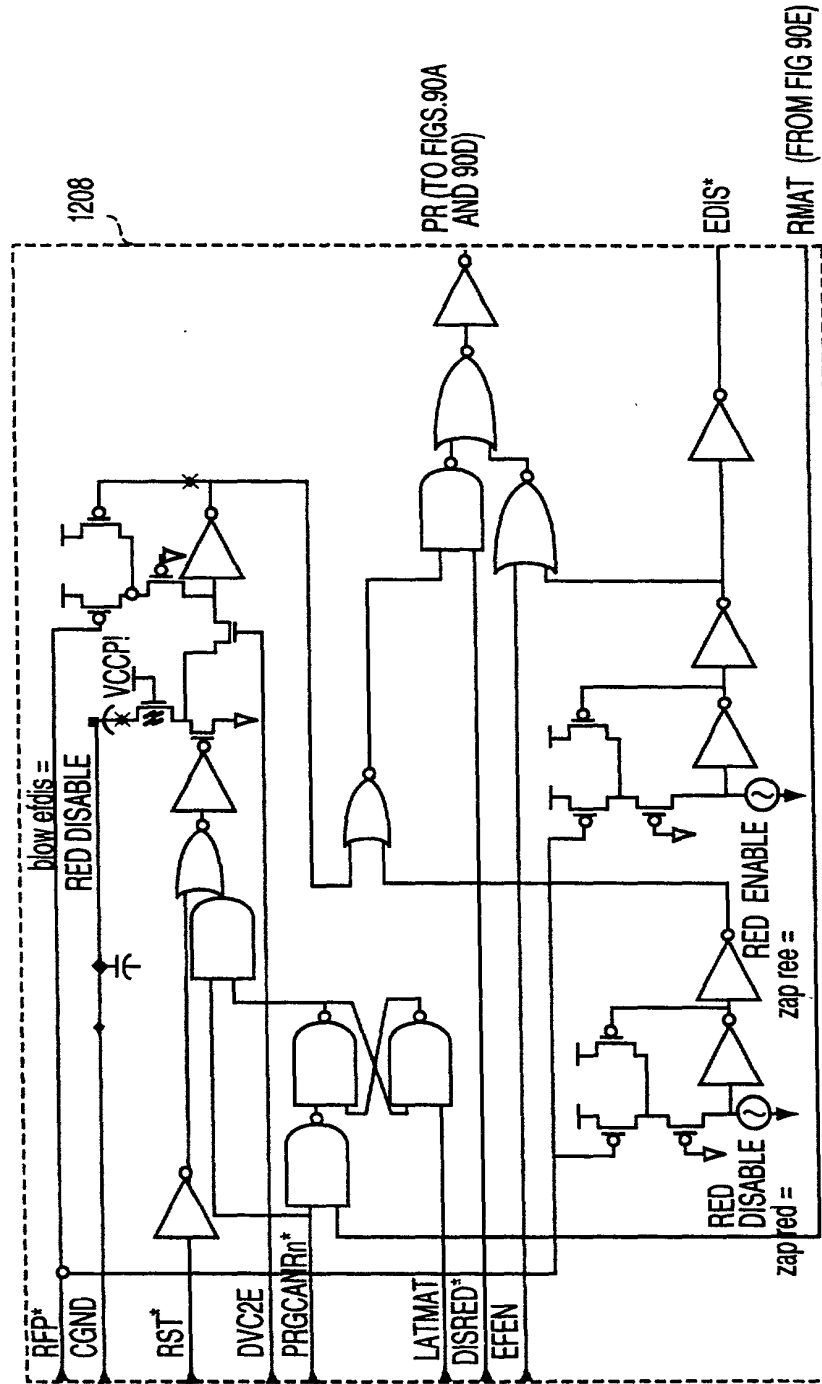


FIG. 90B

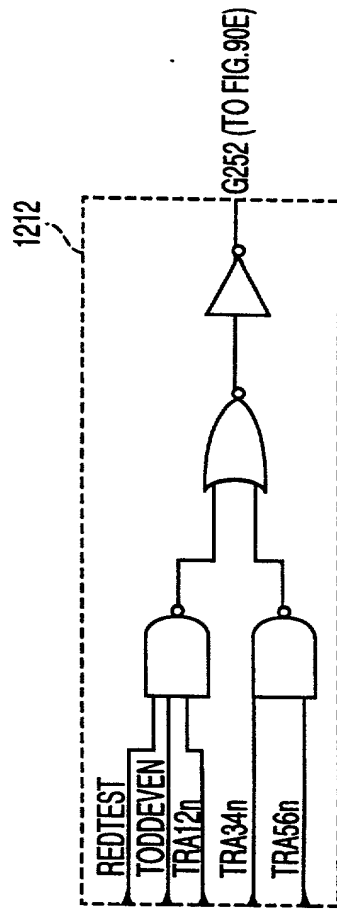


FIG. 90C

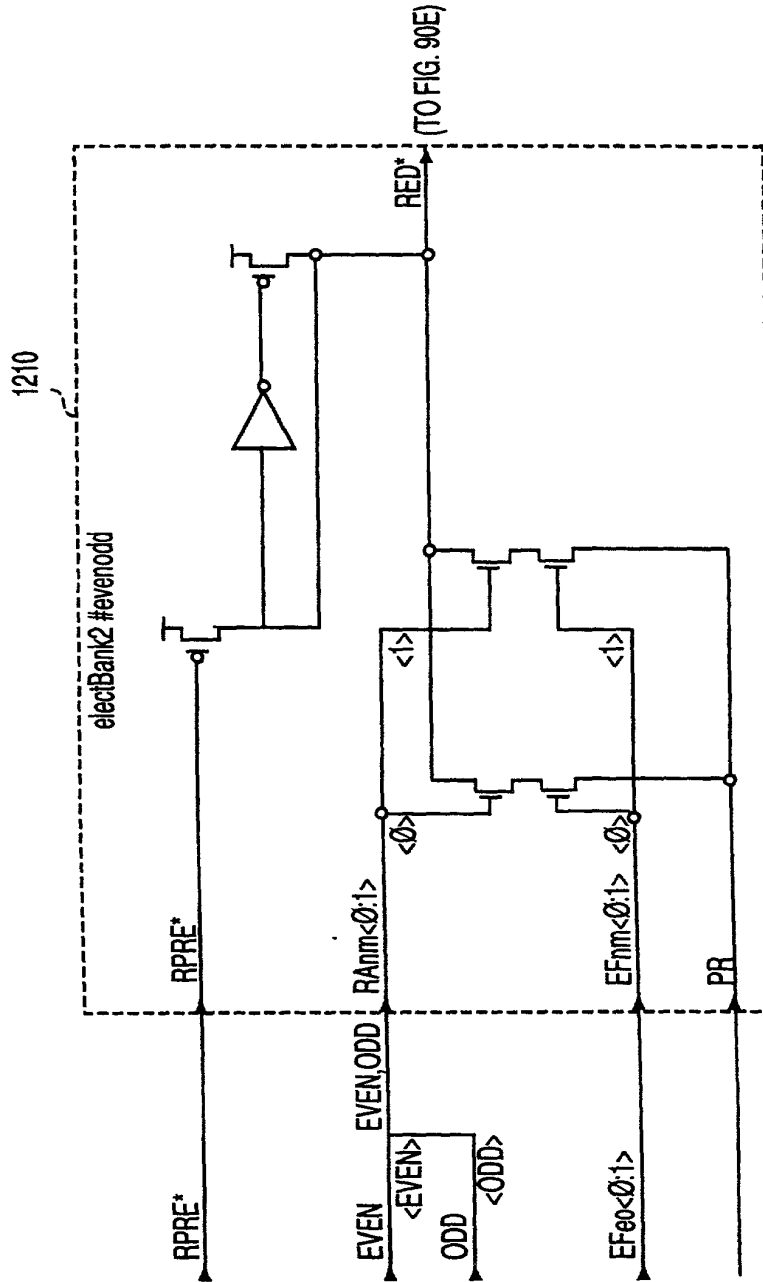


FIG. 90D

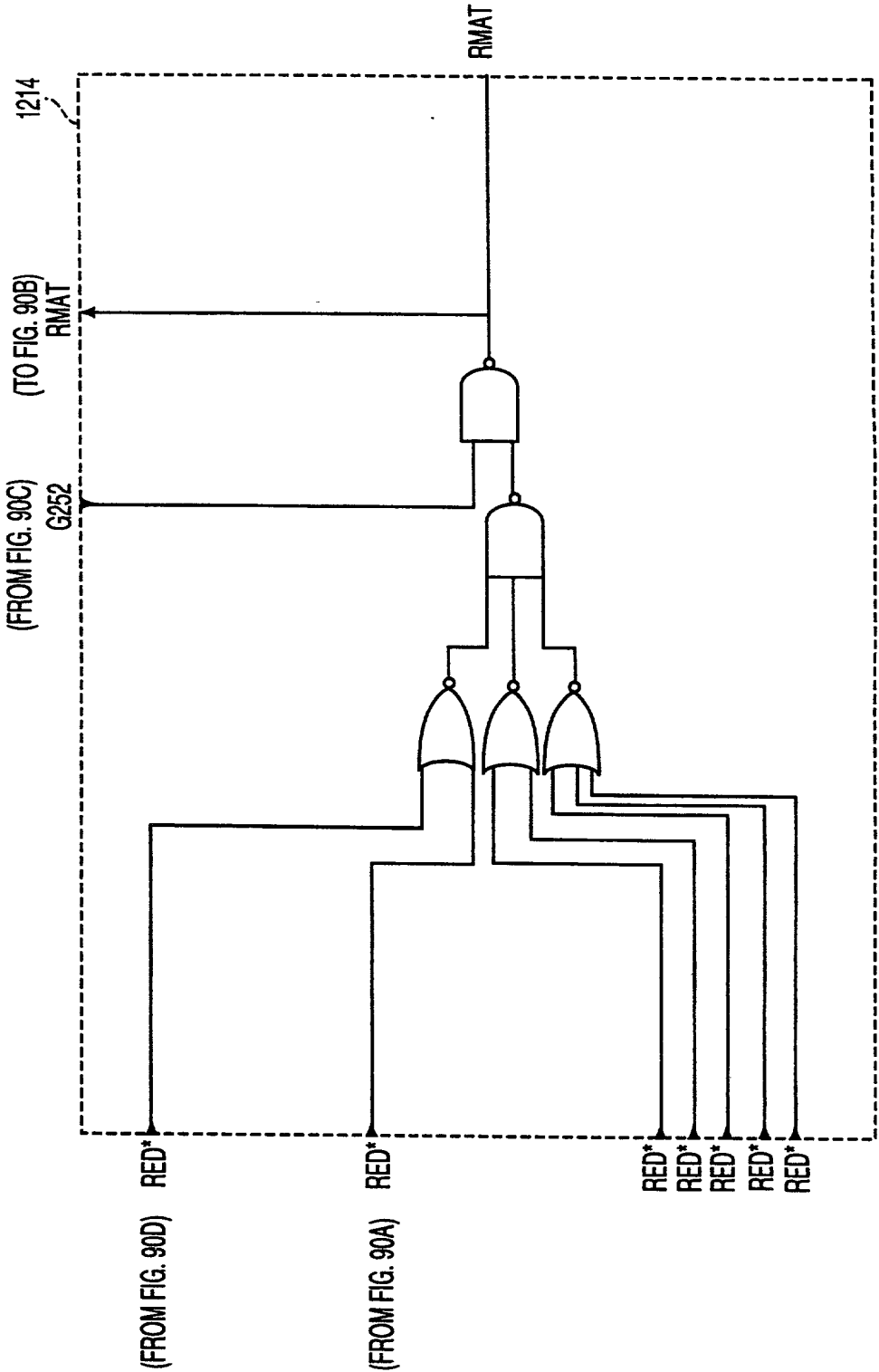
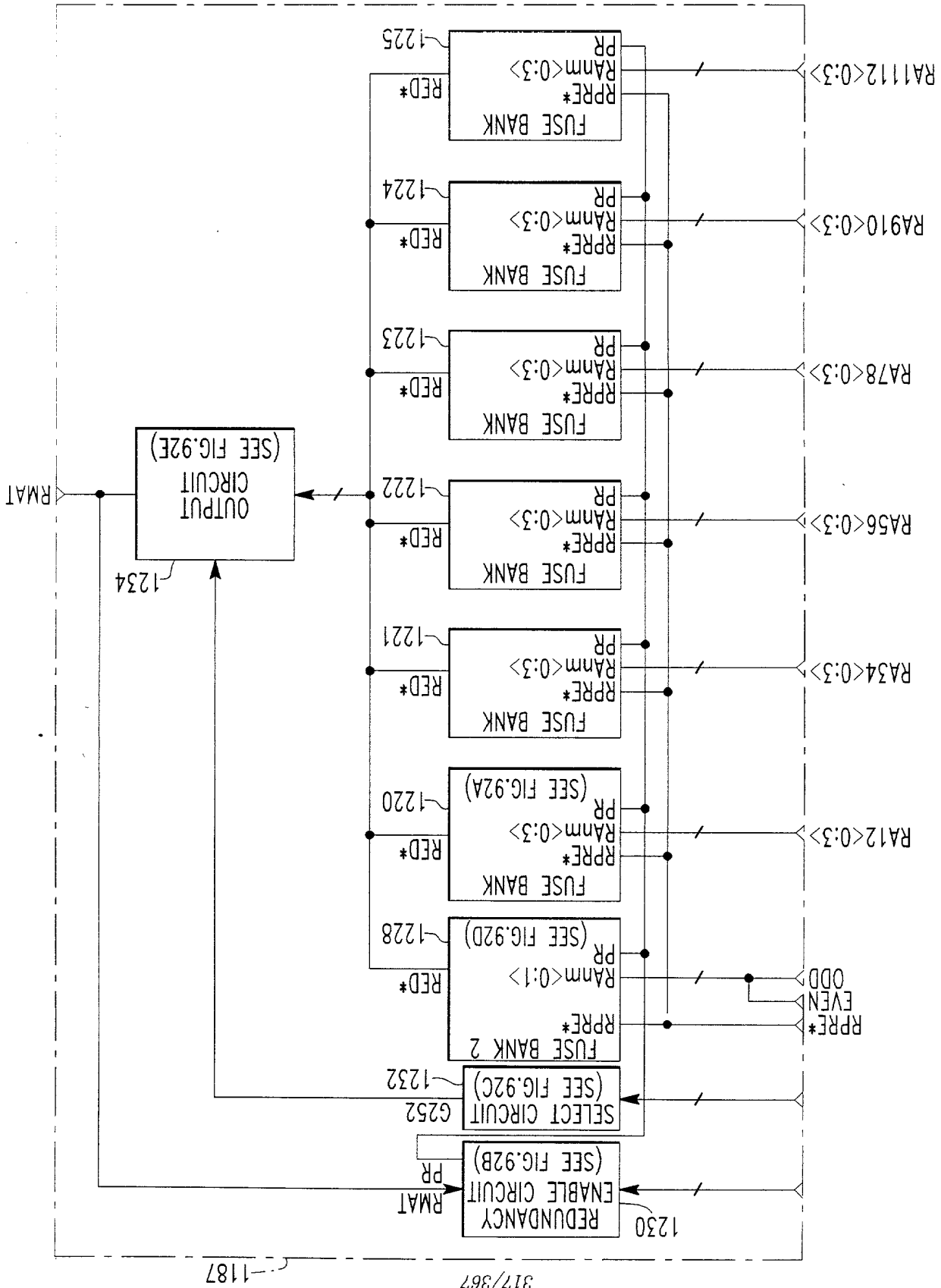


FIG. 90E

FIG. 91



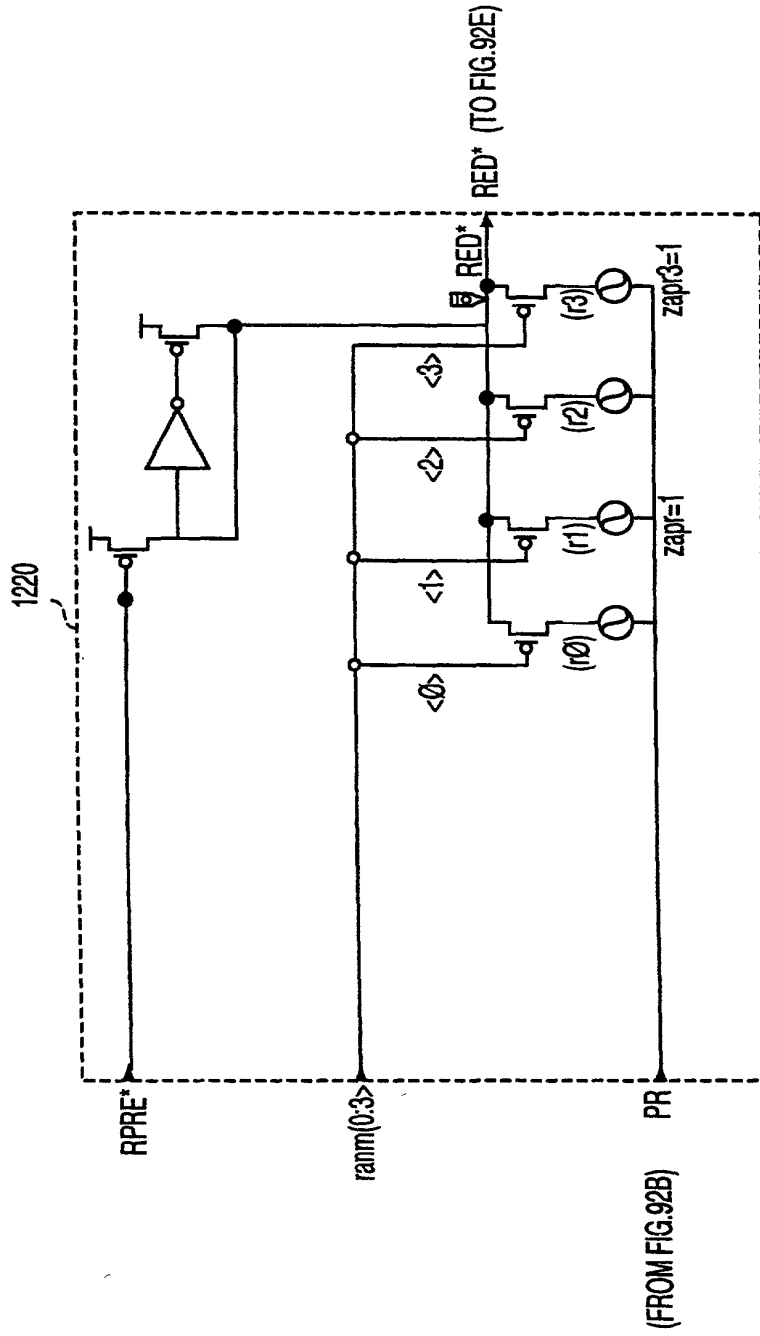


FIG. 92A

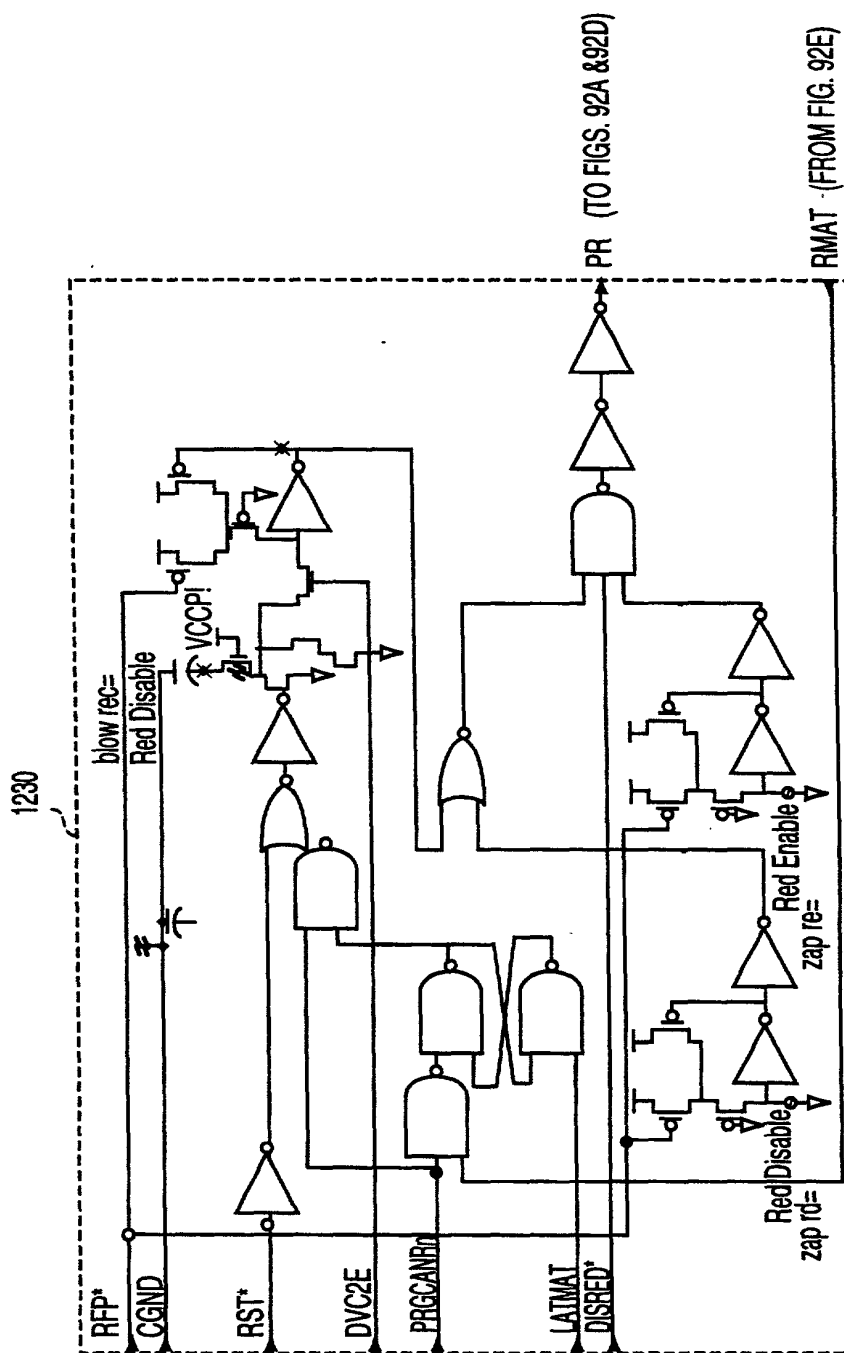
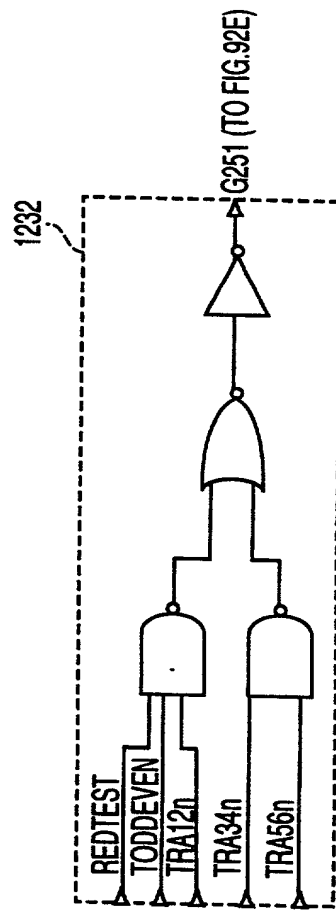


FIG. 92B

**FIG. 92C**

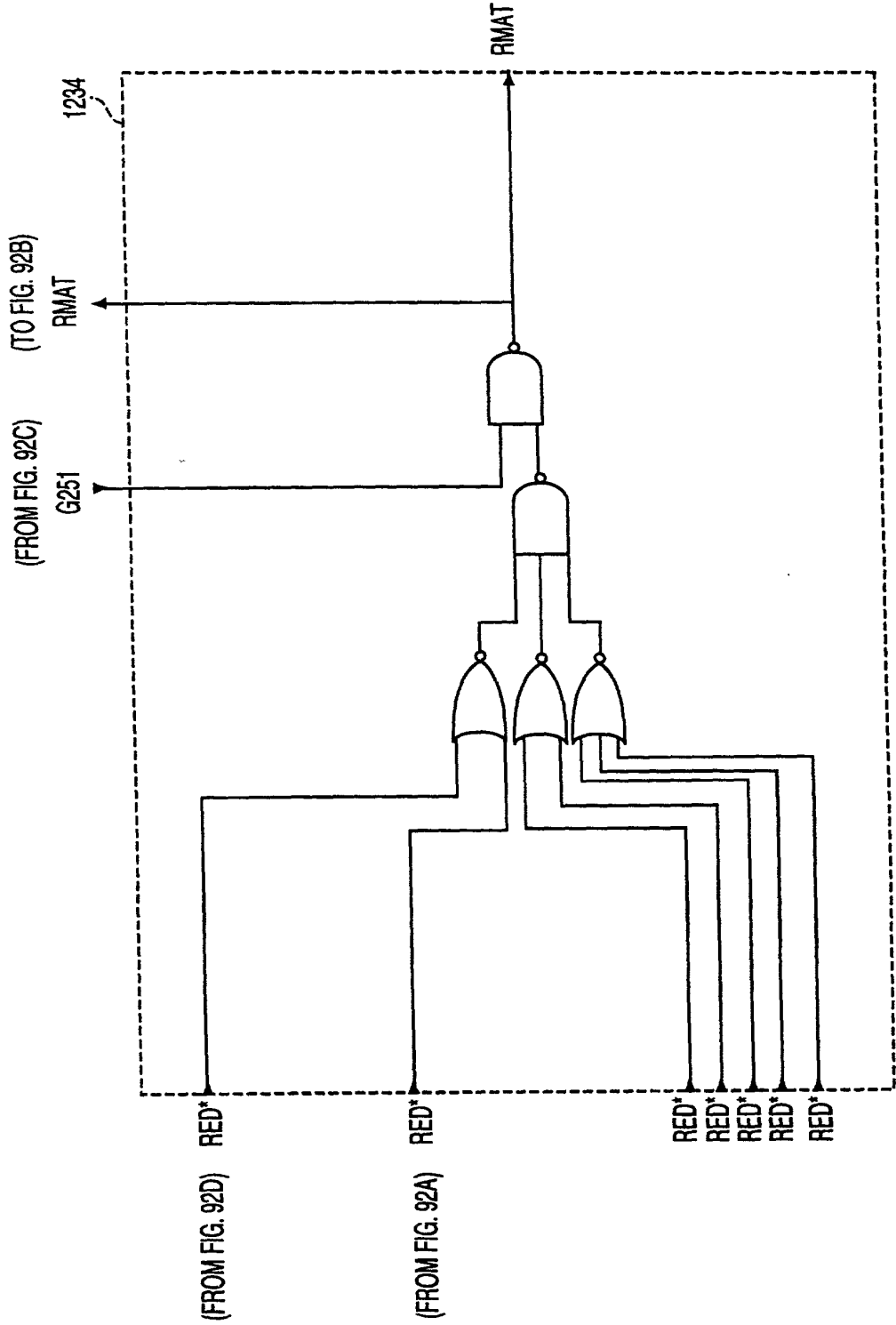
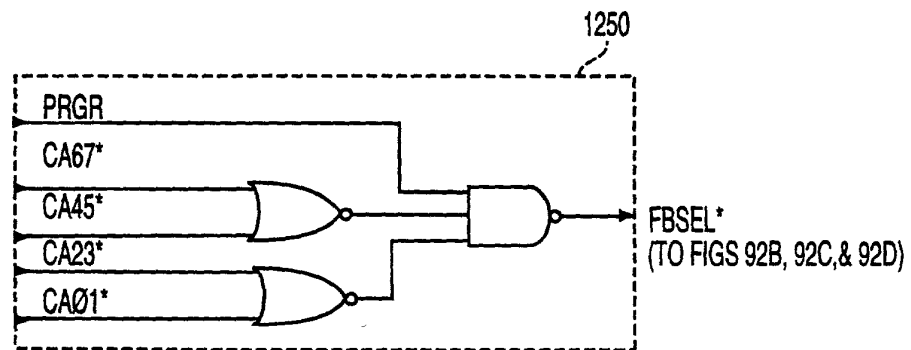


FIG. 92E

**FIG. 93A**

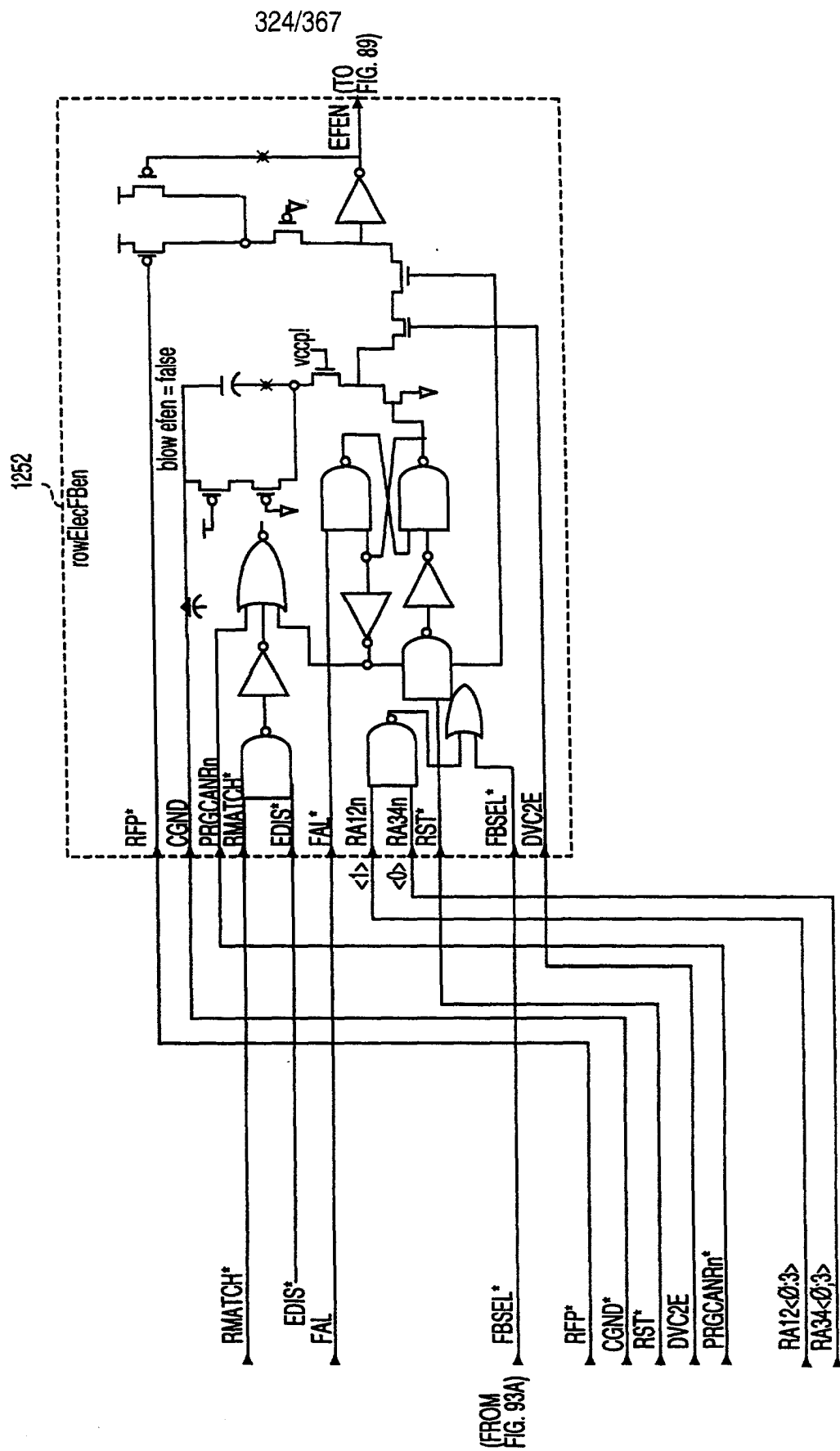


FIG. 93B

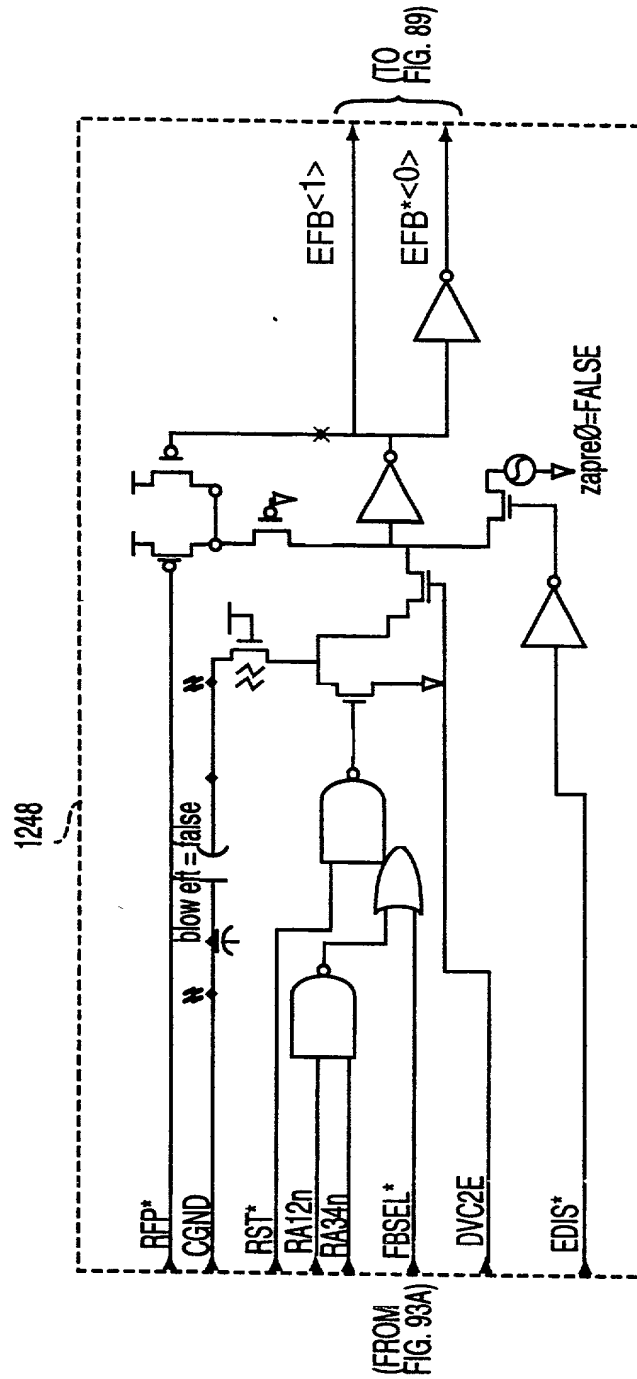


FIG. 93C

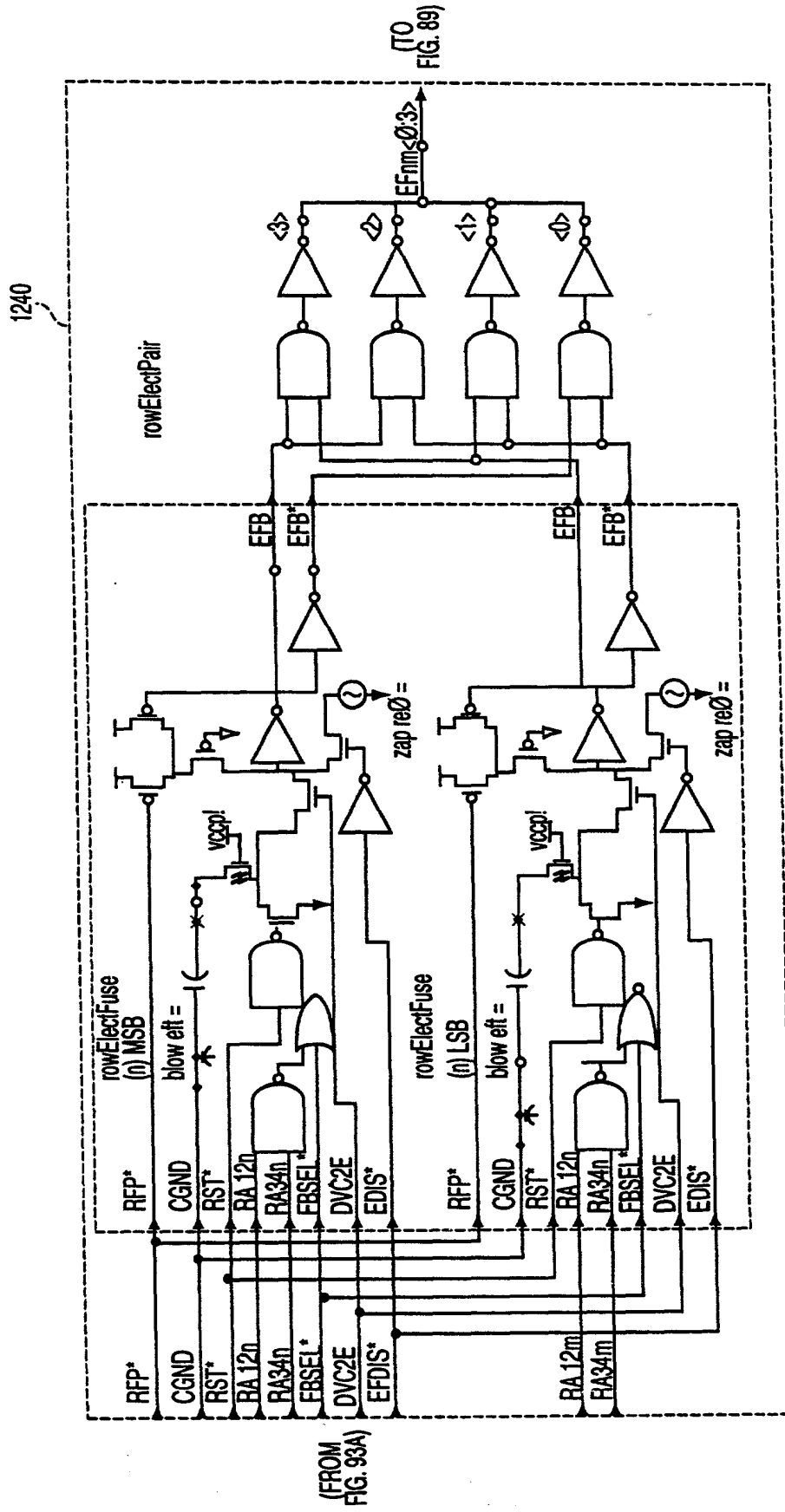
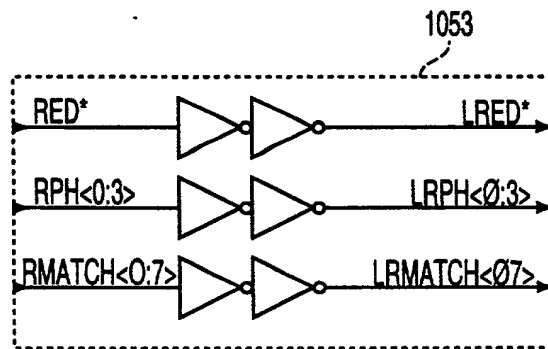


FIG. 93D

**FIG. 94**

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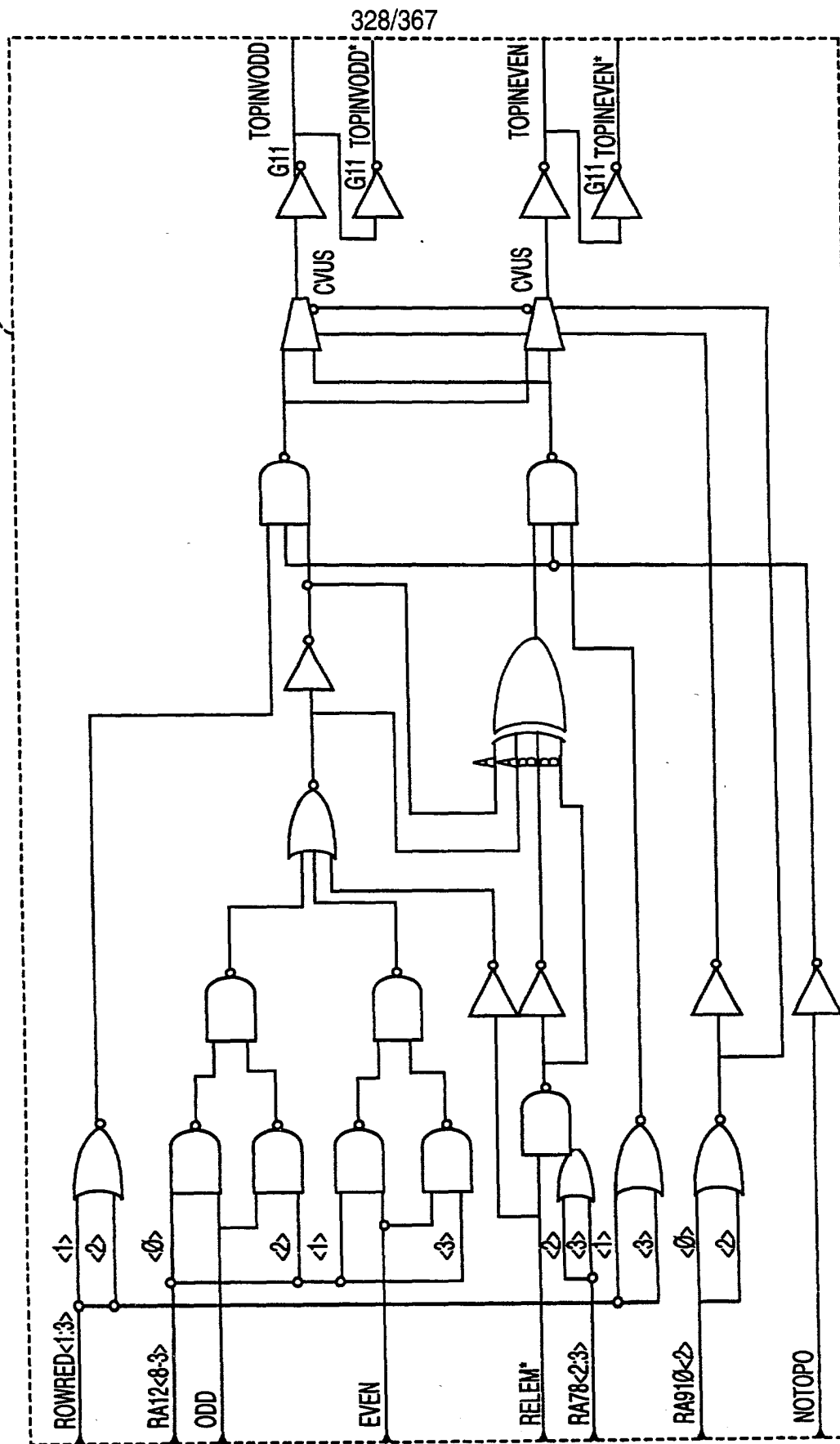


FIG. 95

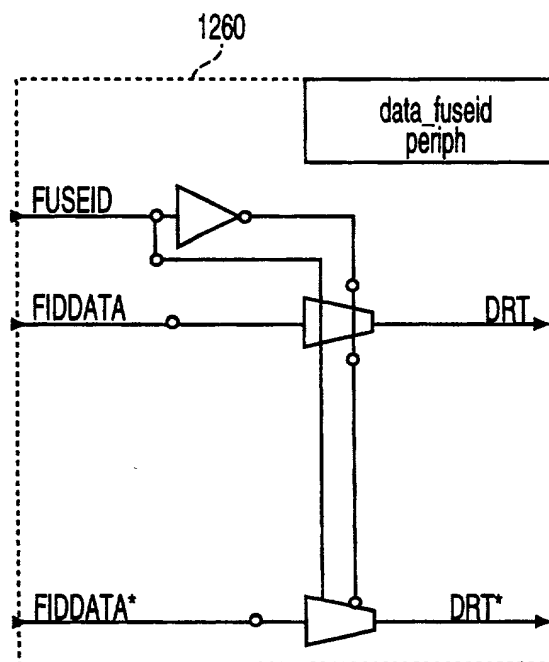
**FIG. 96**



FIG. 97-1 | FIG. 97-2

FIG. 97-1

FIG. 97-1

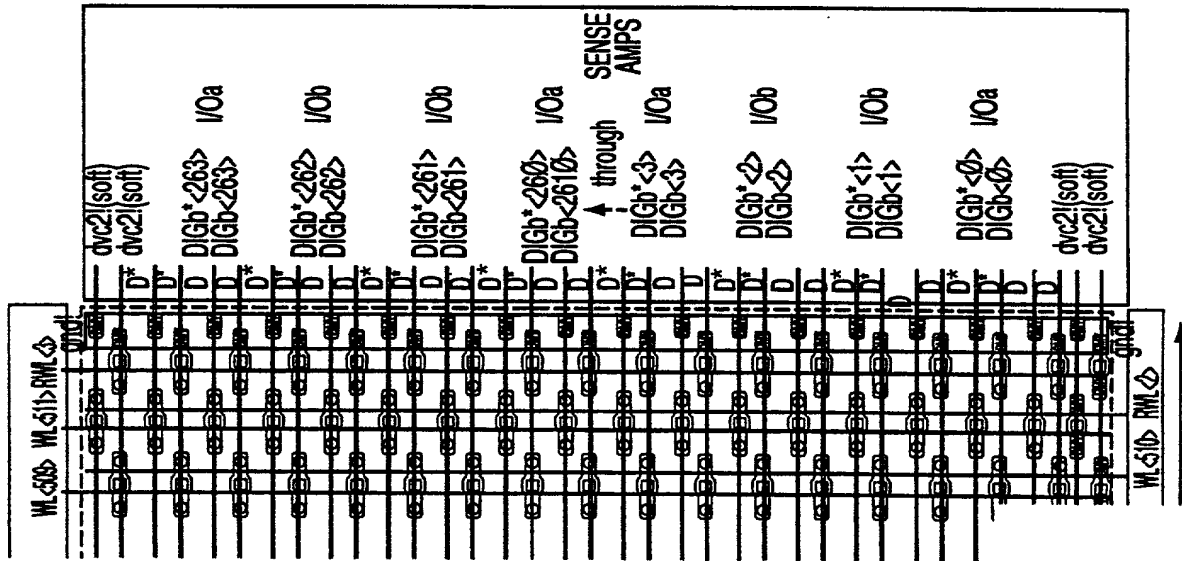
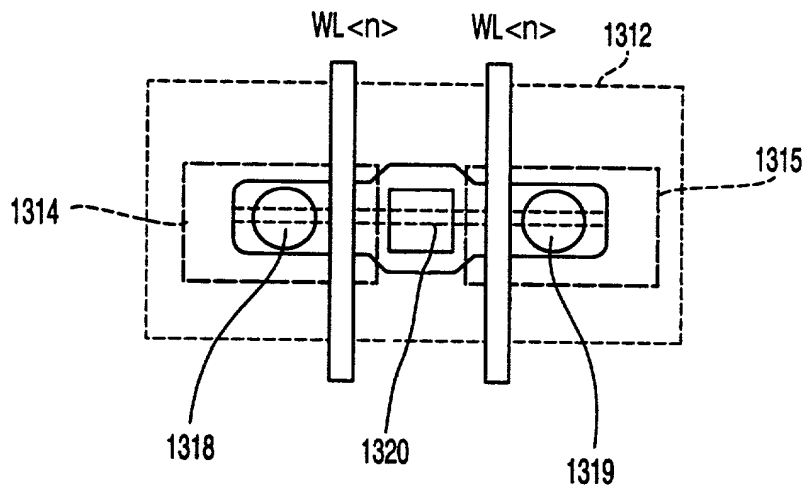


FIG. 97-1

FIG. 97-2

**FIG. 98**

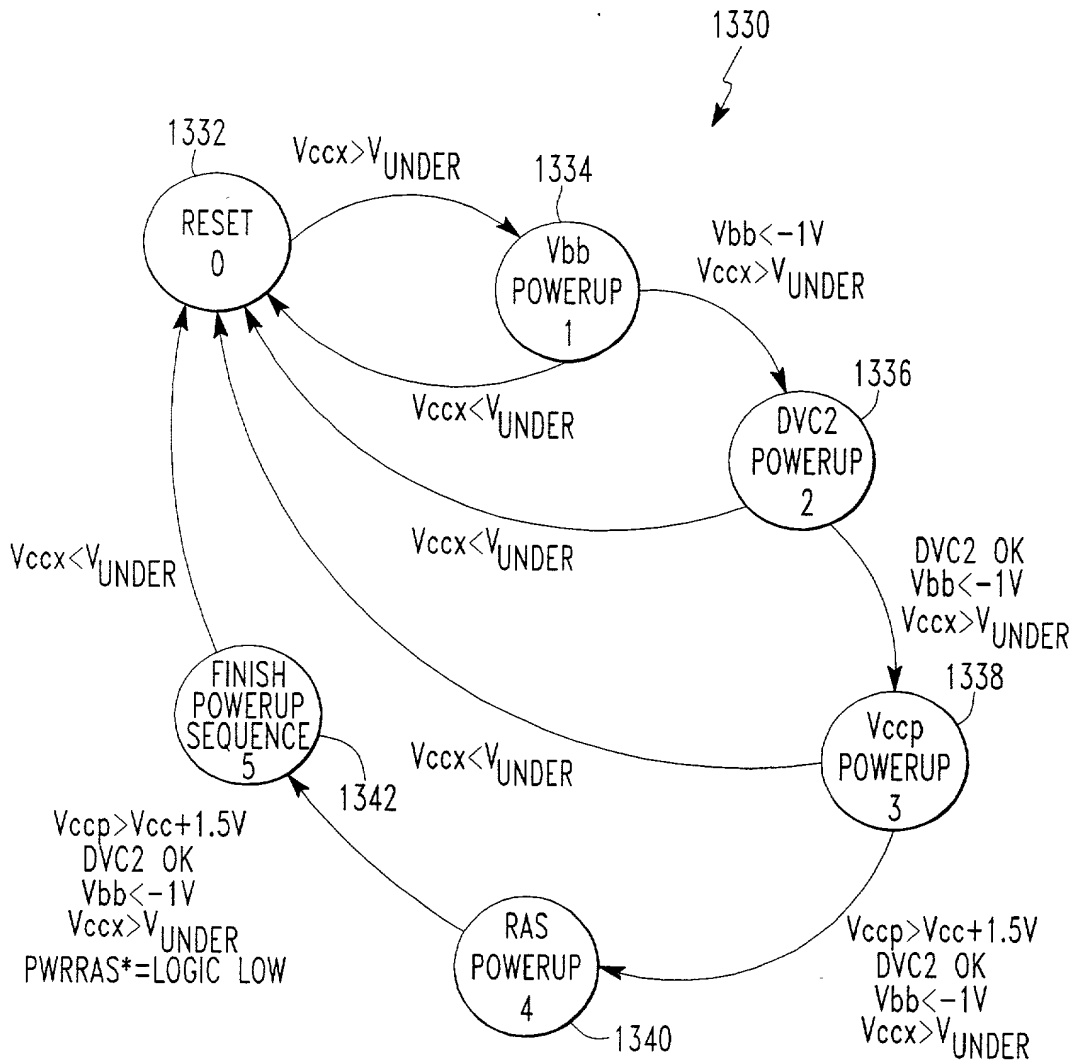


FIG. 99

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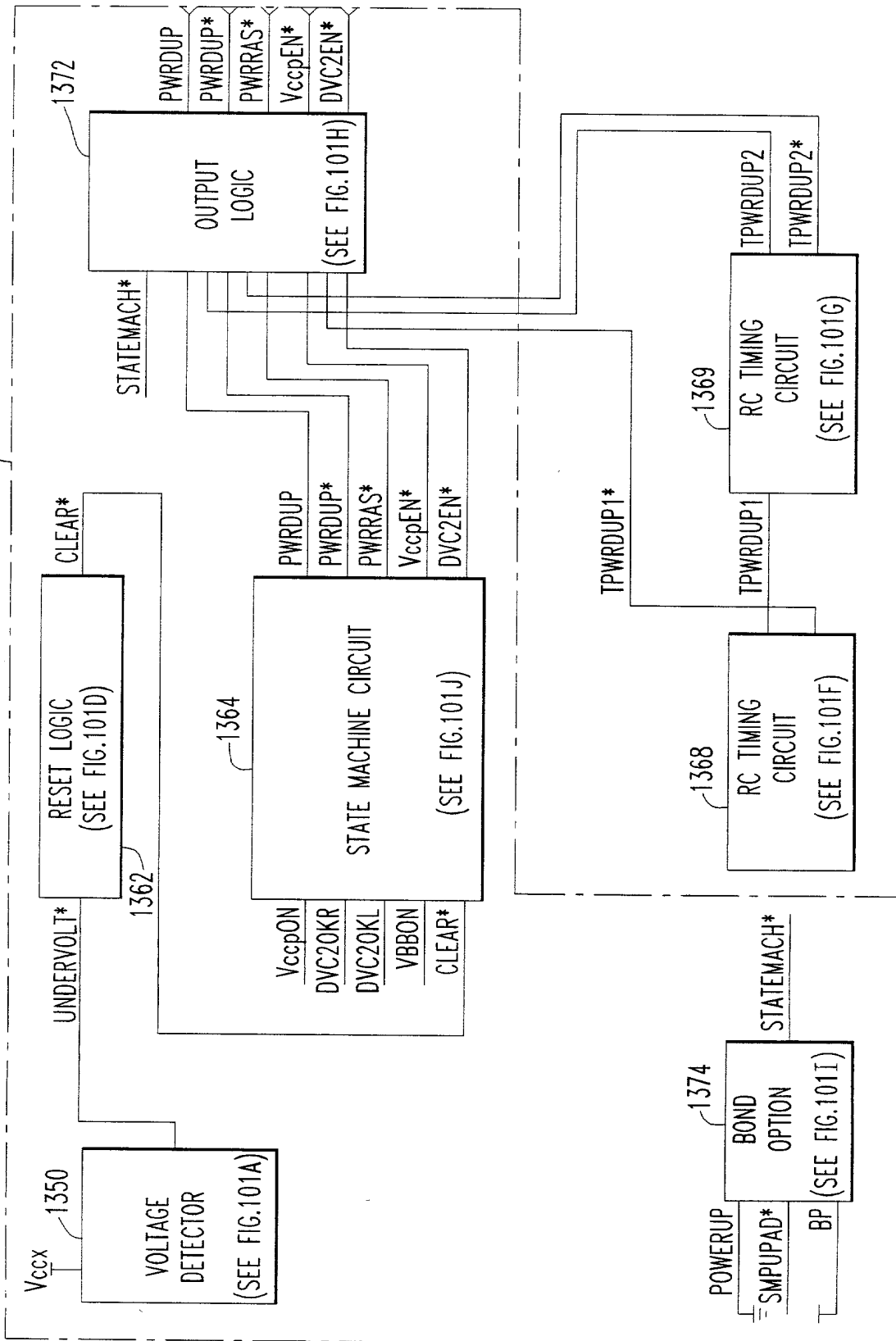


FIG. 100

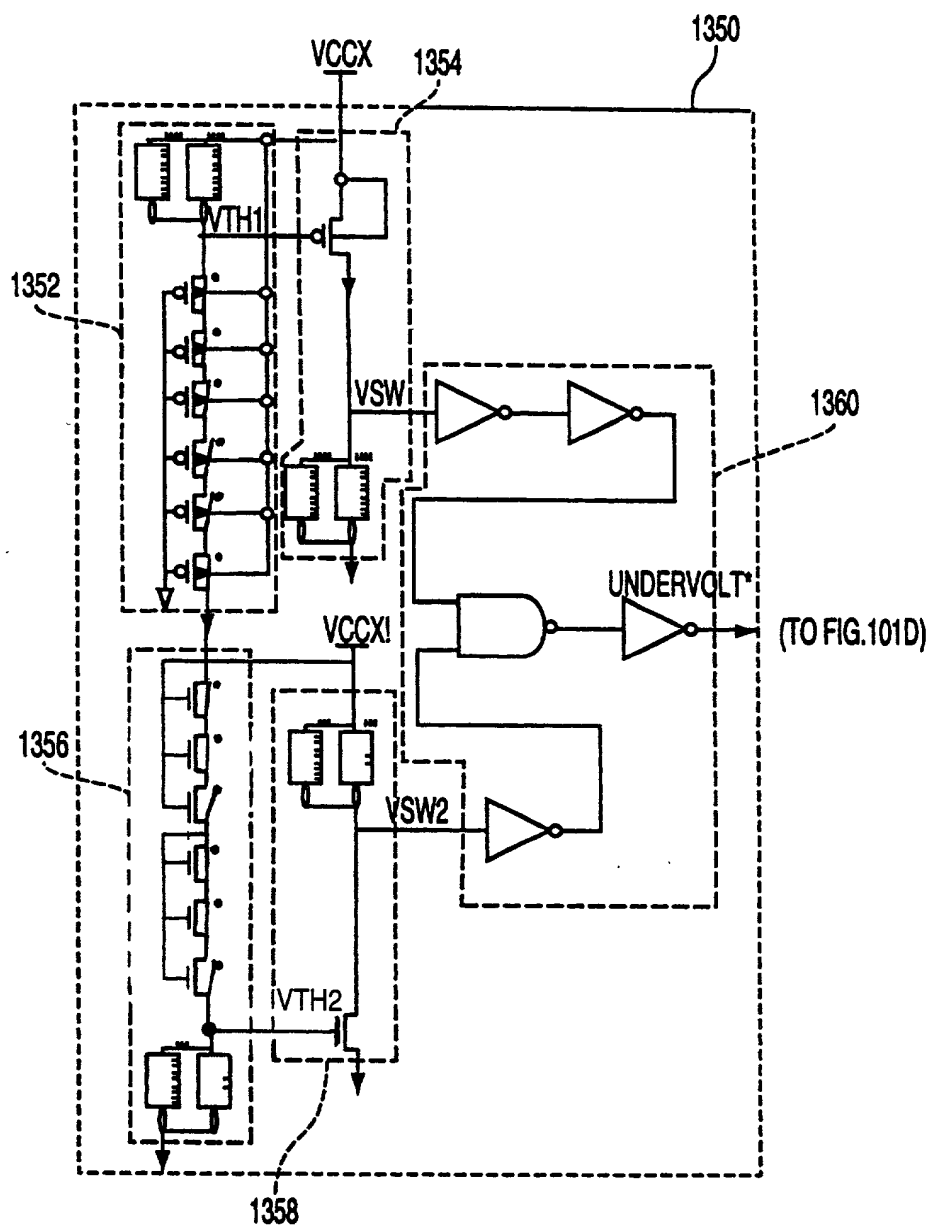
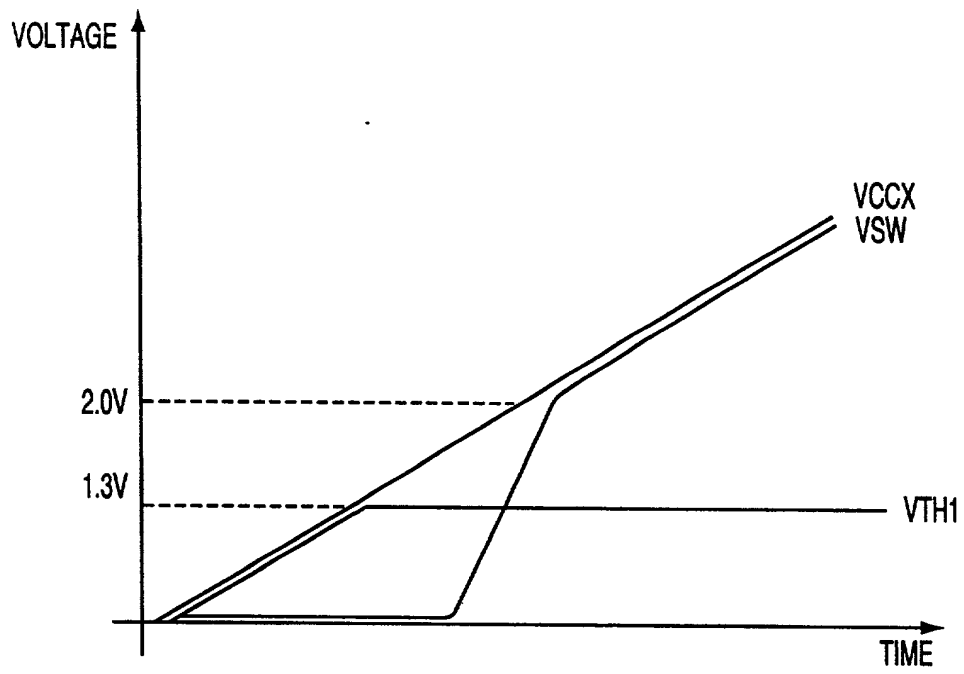
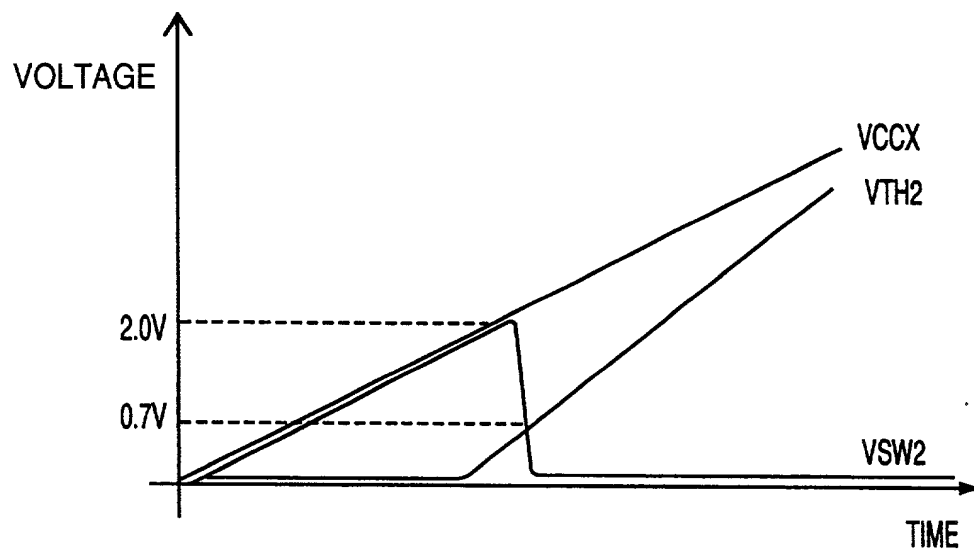


FIG. 101A

**FIG. 101B**

**FIG. 101C**

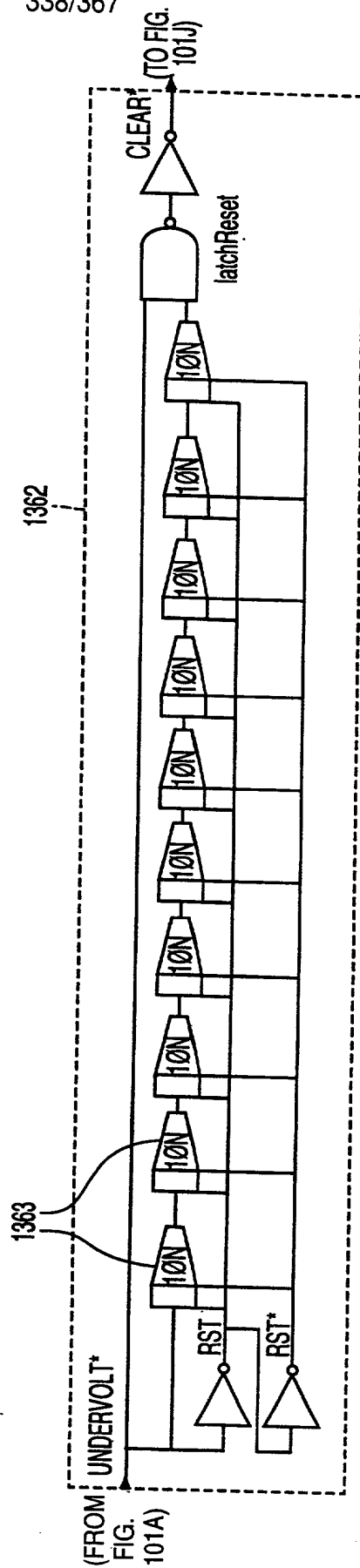


FIG. 101D

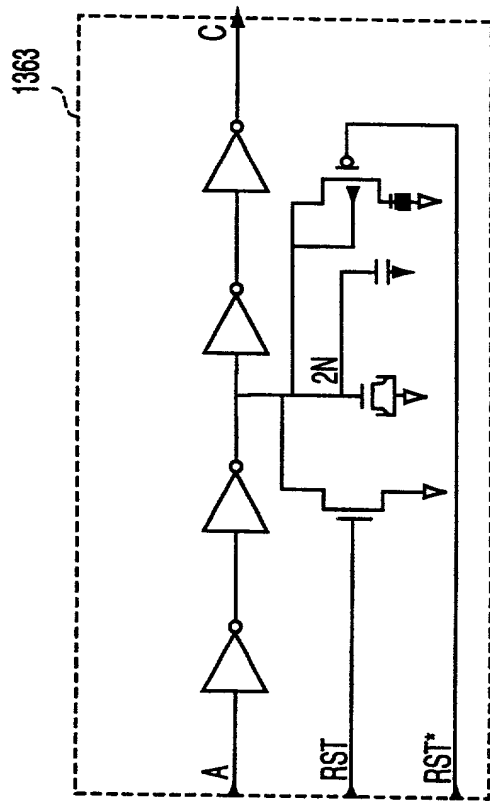


FIG. 101E

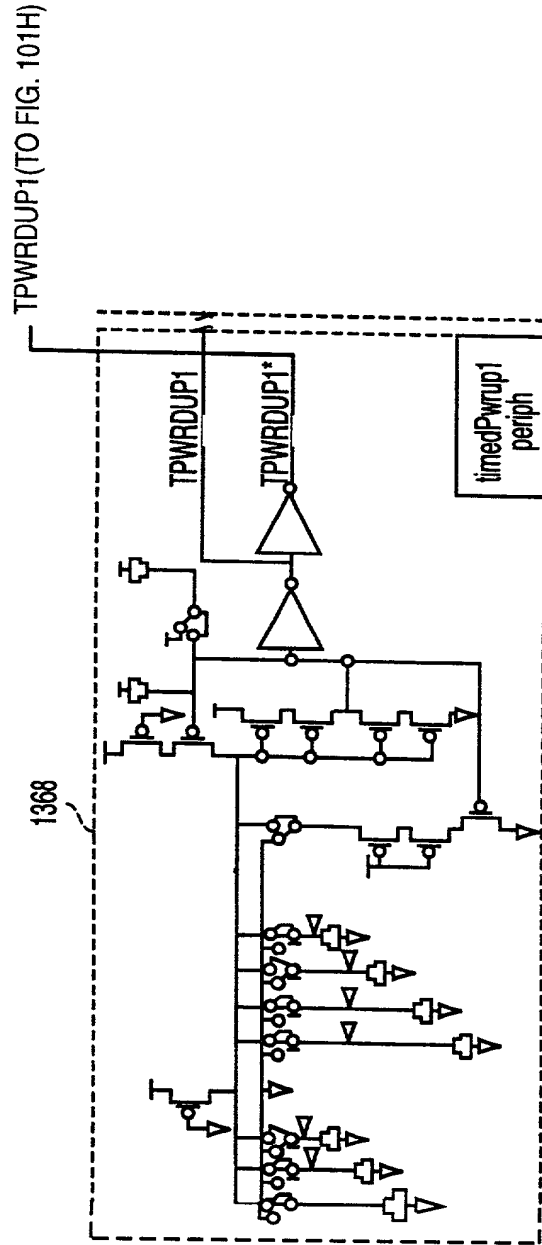


FIG. 101F

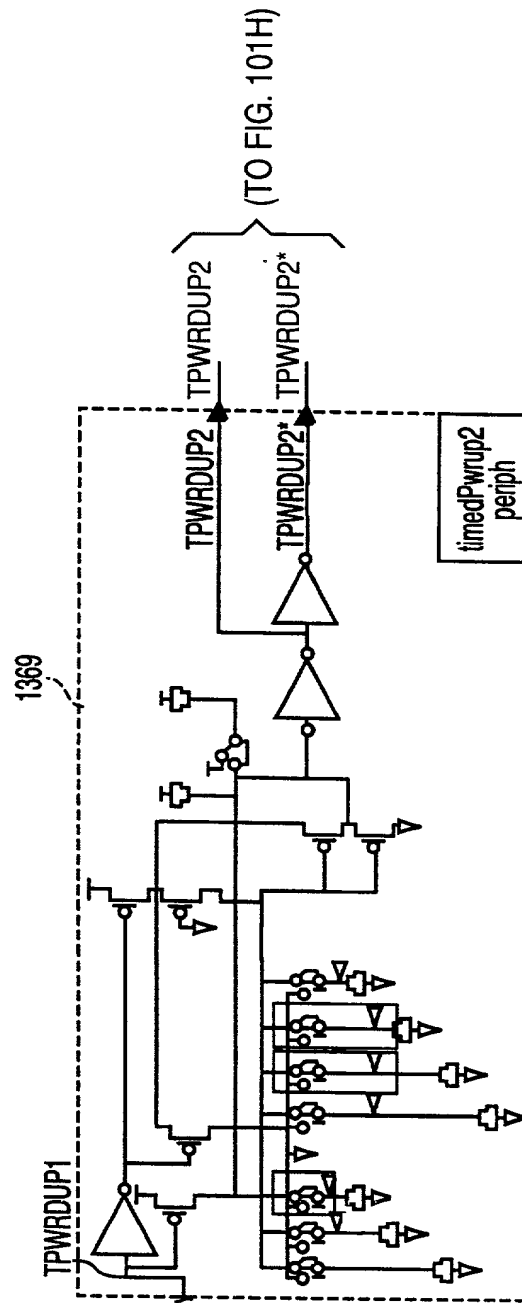


FIG. 101H

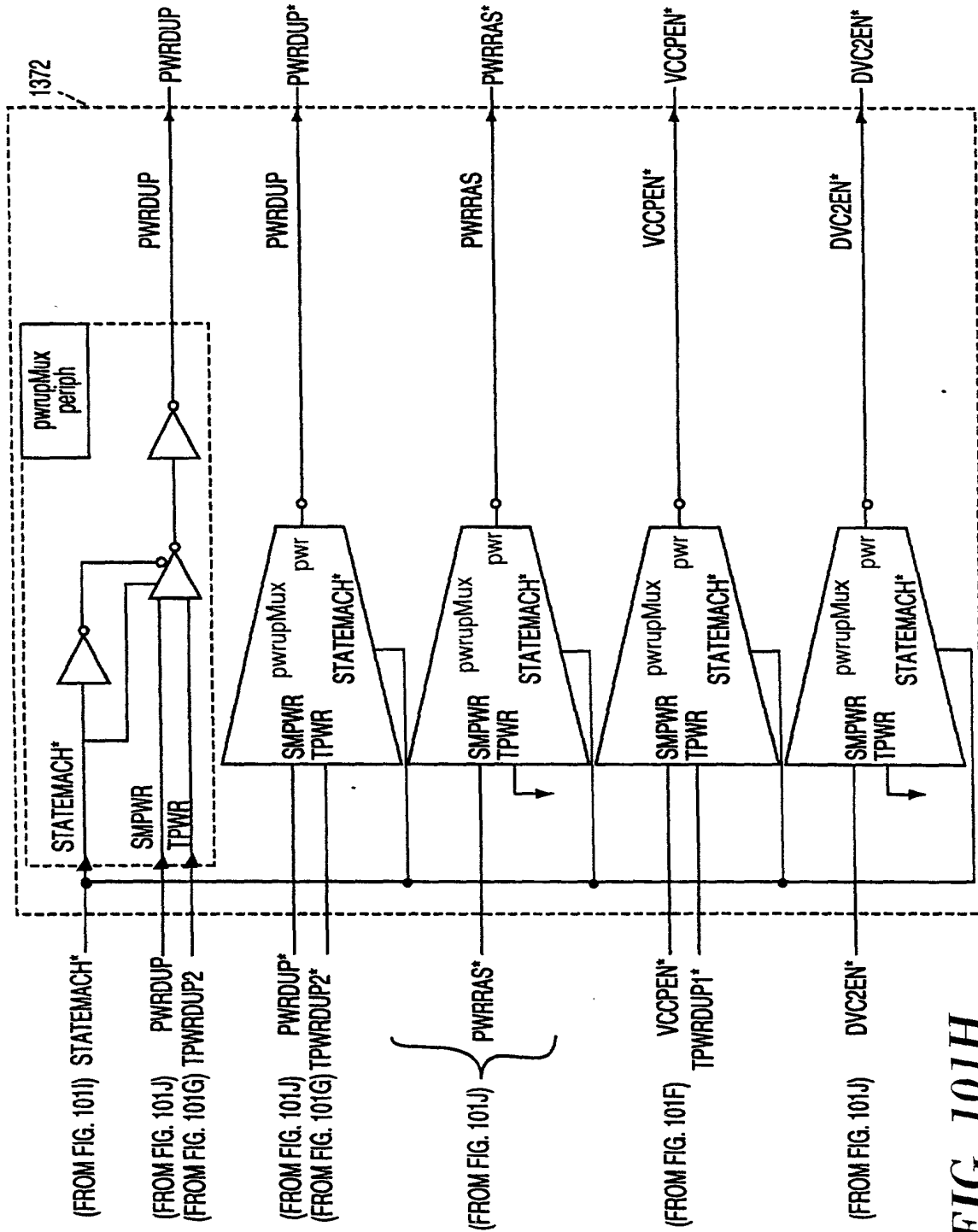
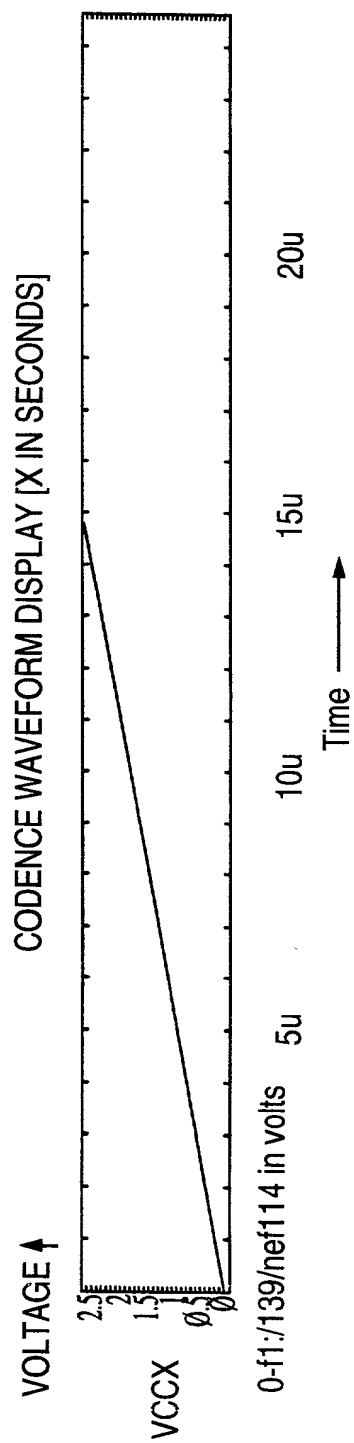
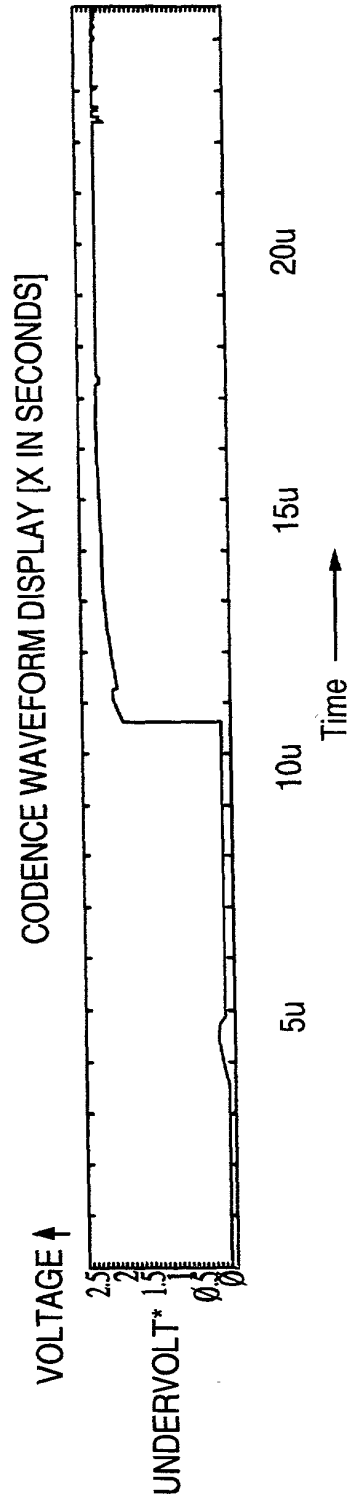


FIG. 101H



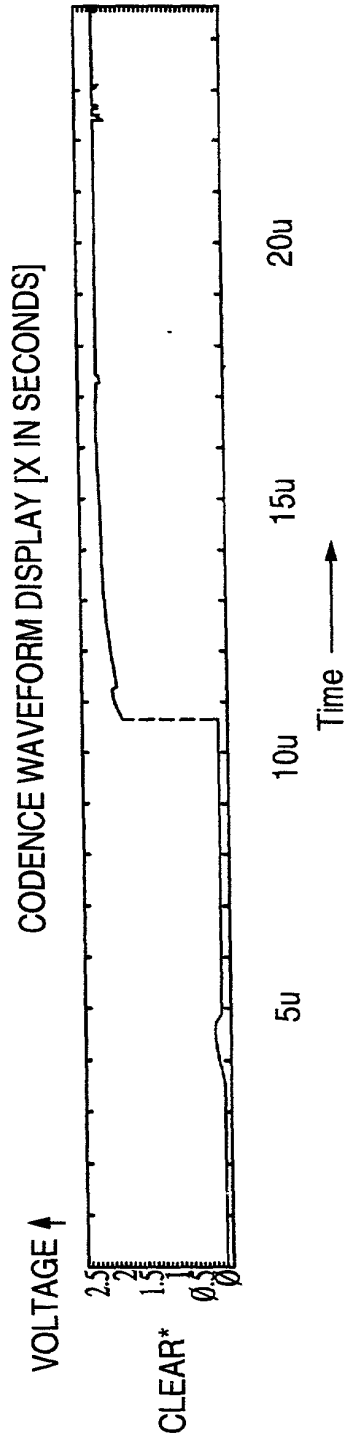
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102A



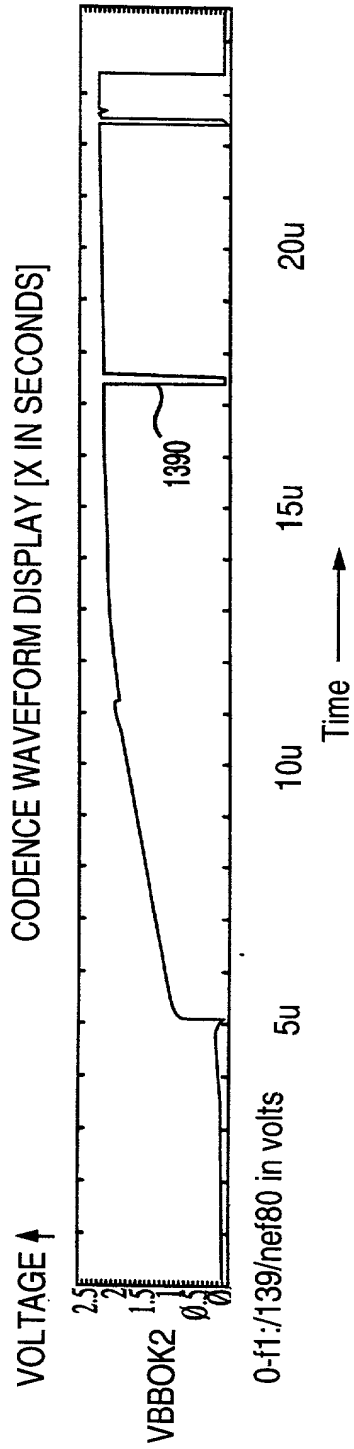
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102B



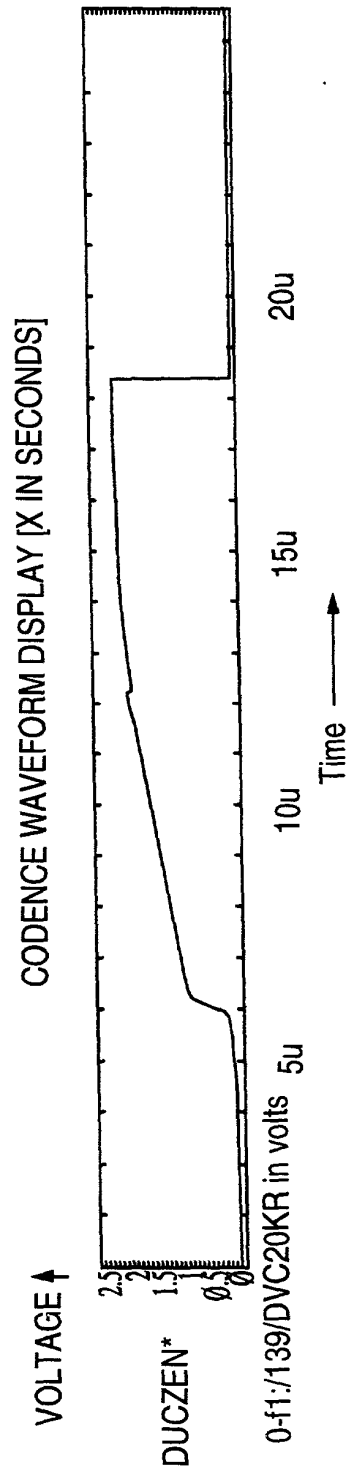
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102C



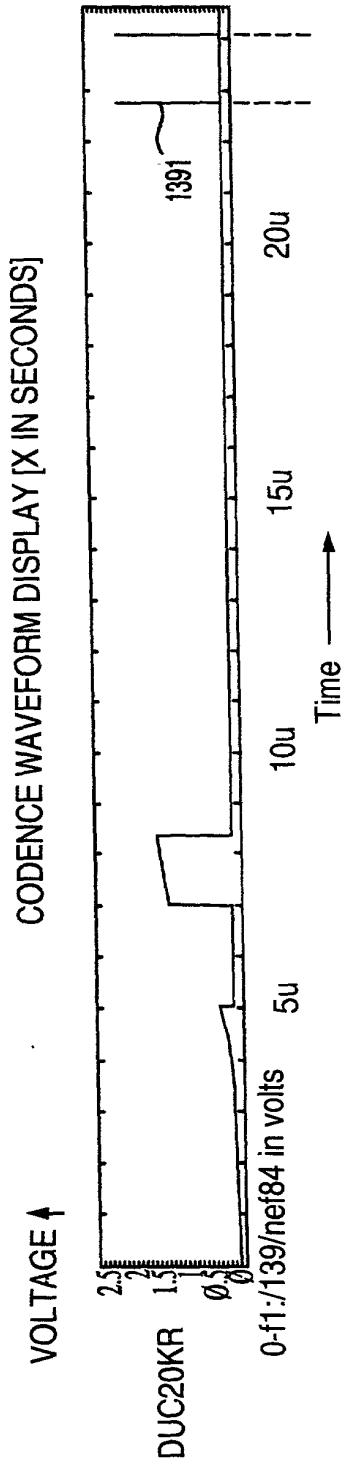
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102D



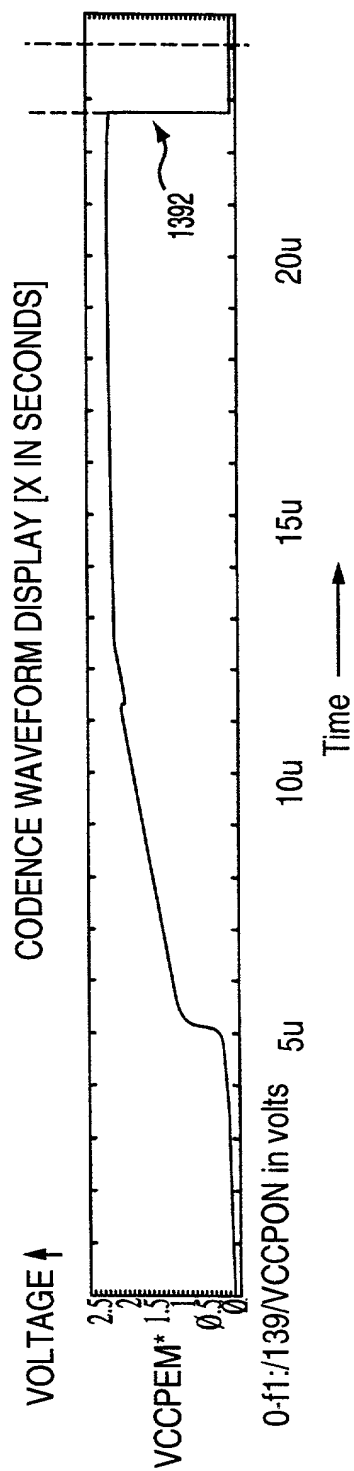
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102E



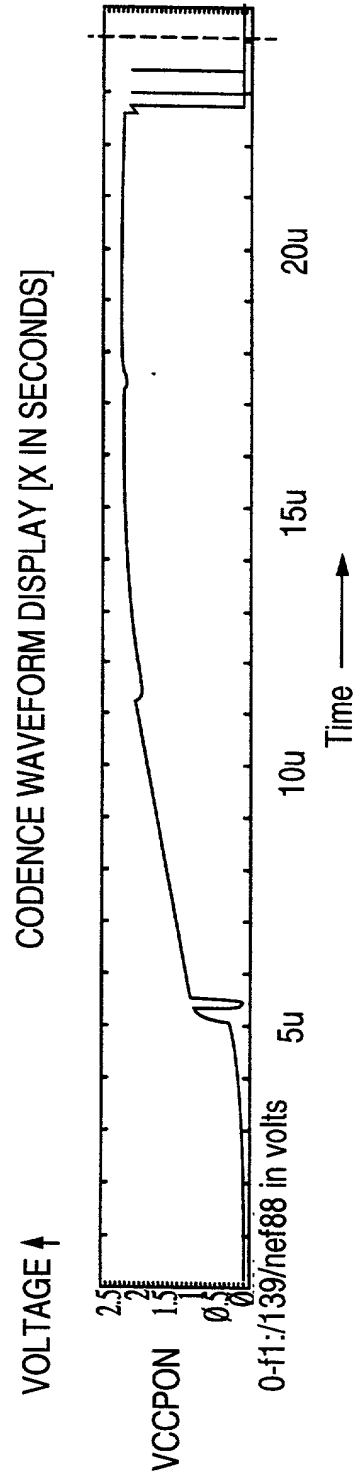
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102F



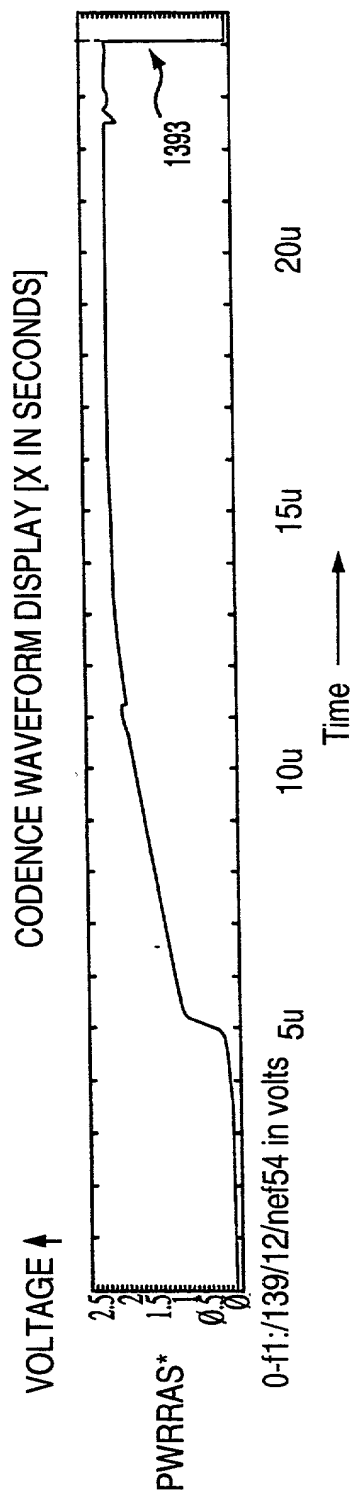
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102G



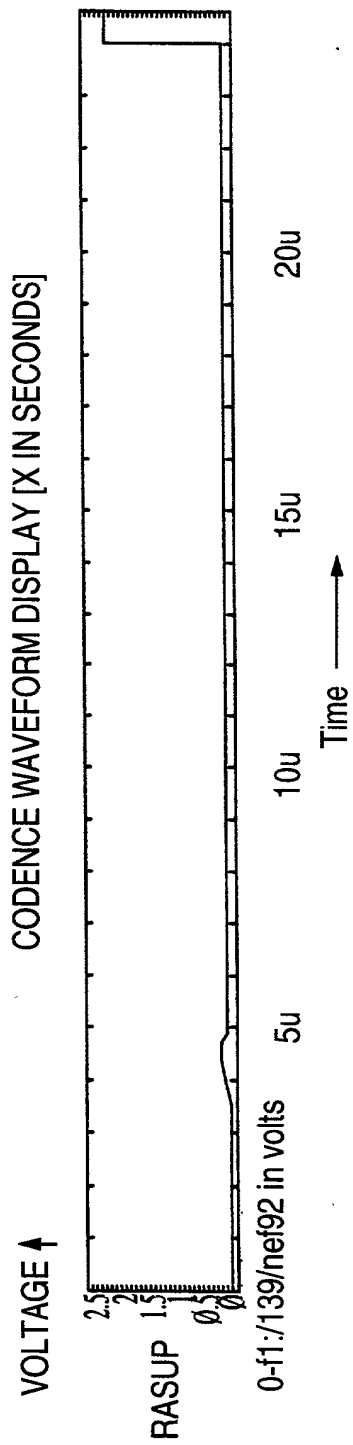
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102H



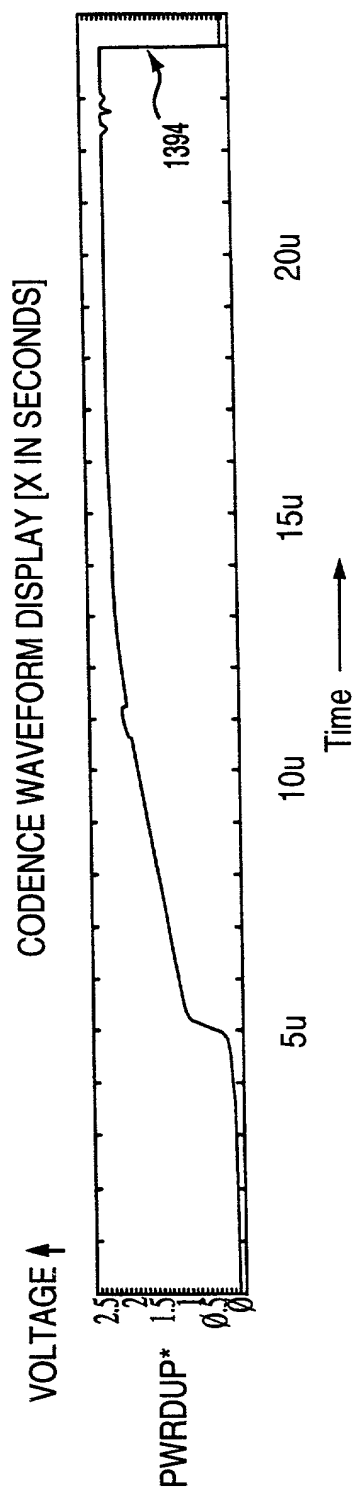
NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 1021



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102J



NOTE THAT PWRRAS* WAITED FOR DVC20KR

FIG. 102K

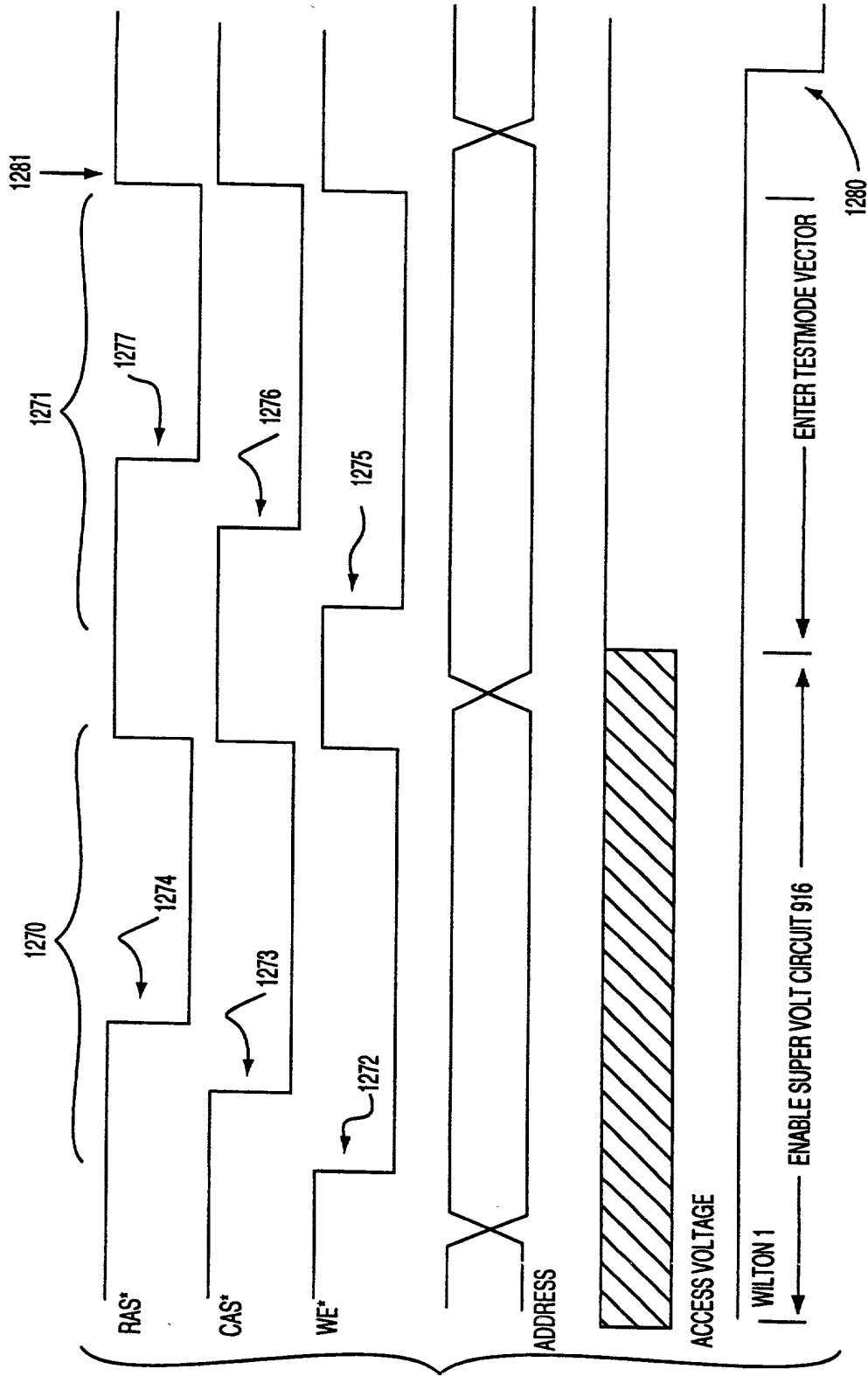


FIG.
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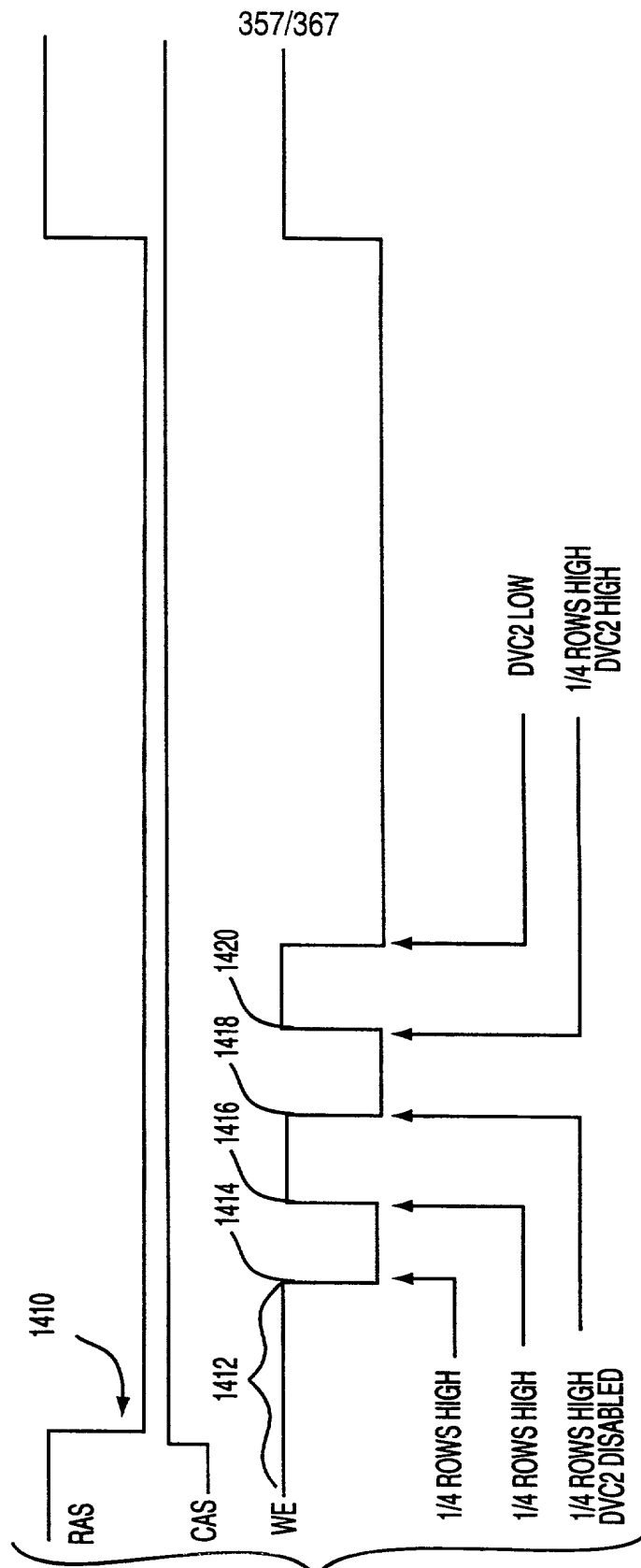


FIG.
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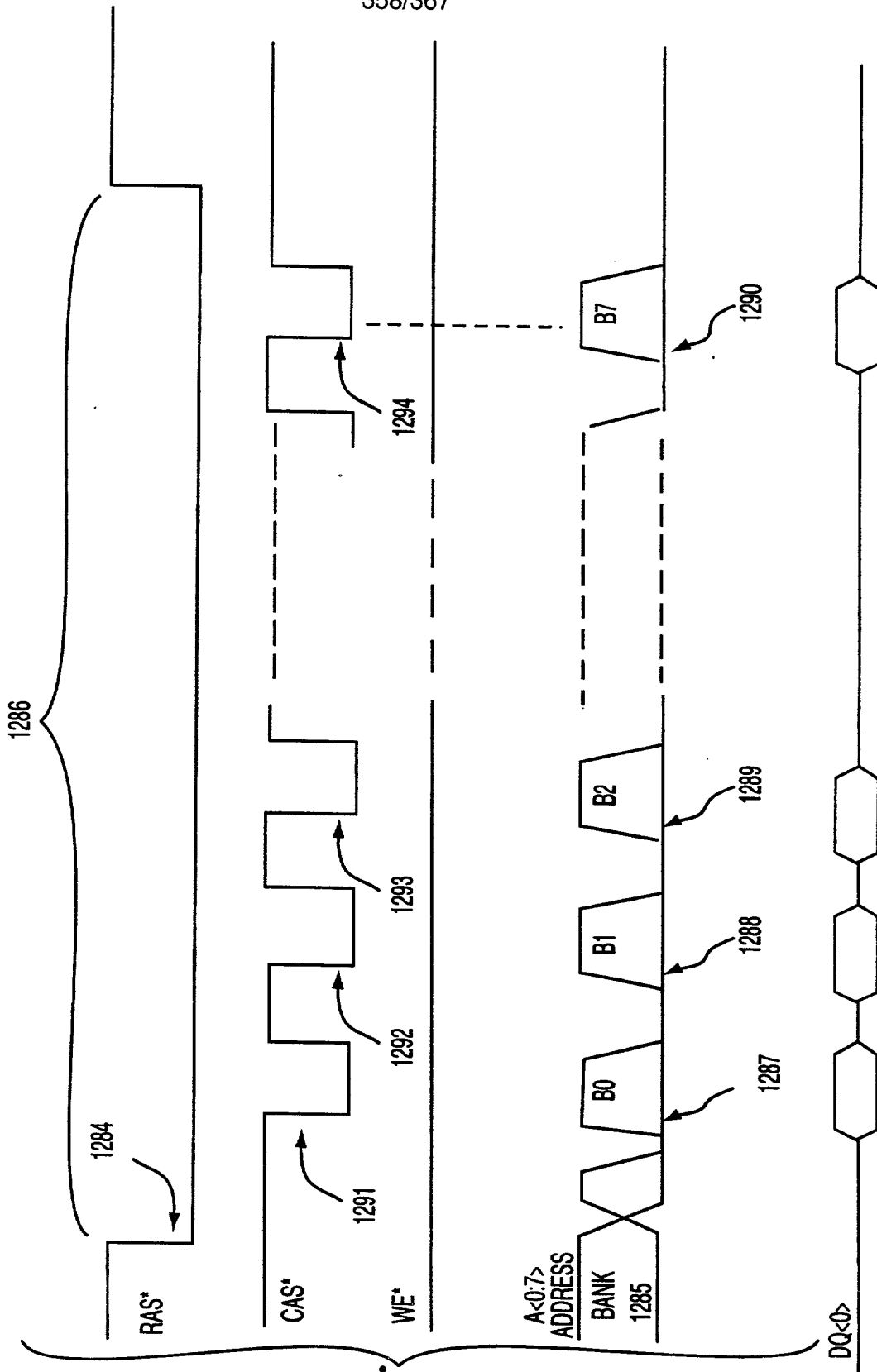


FIG. 105

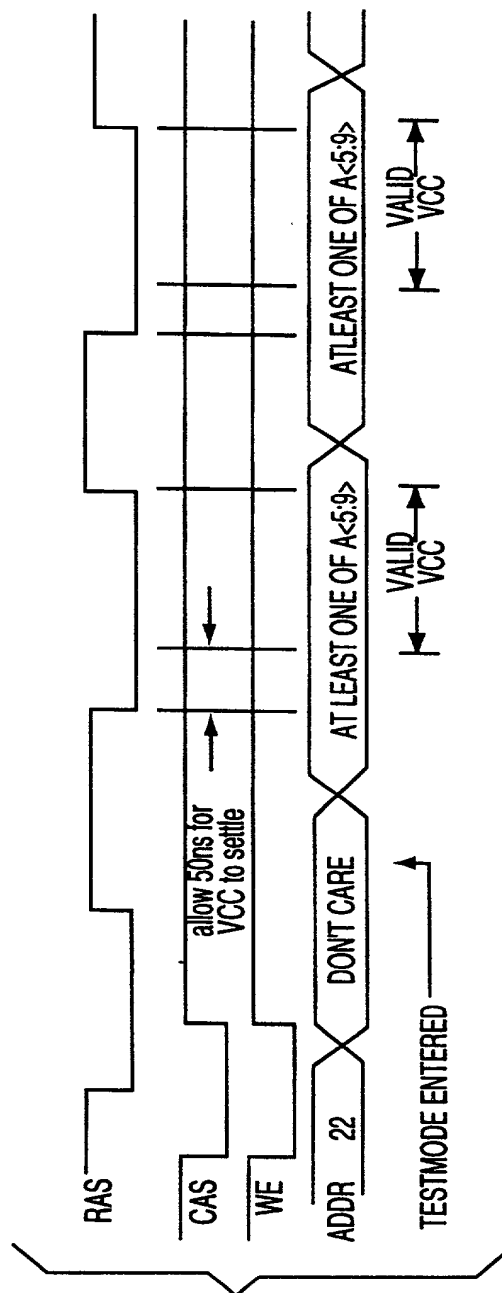


FIG. 106

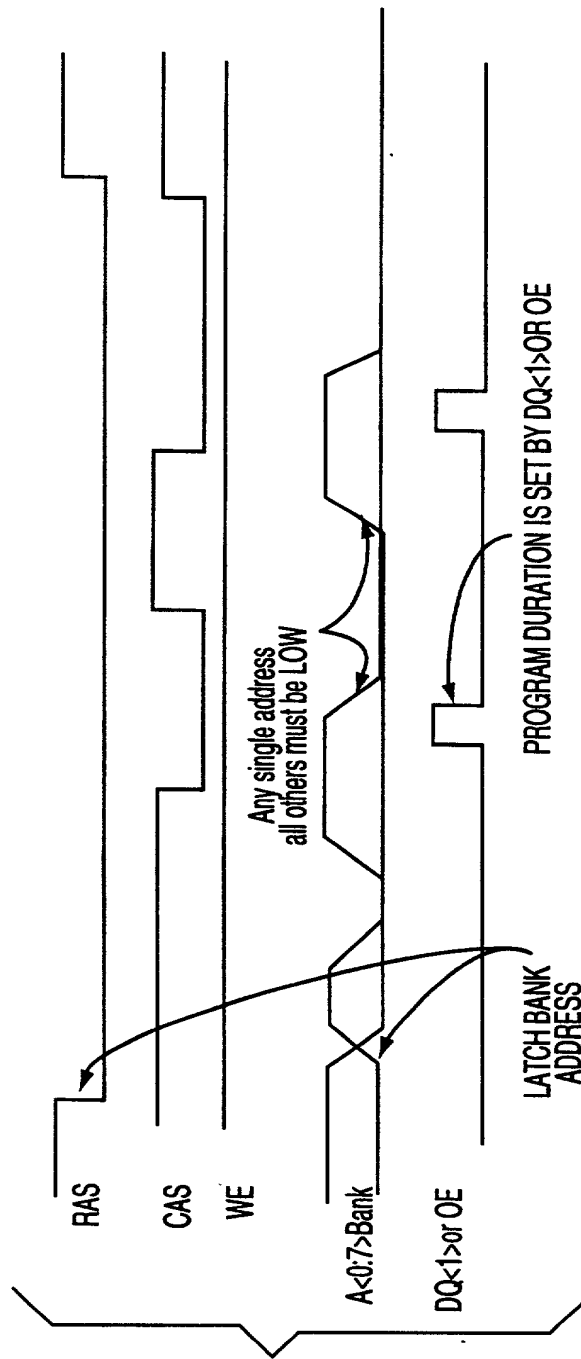


FIG. 107

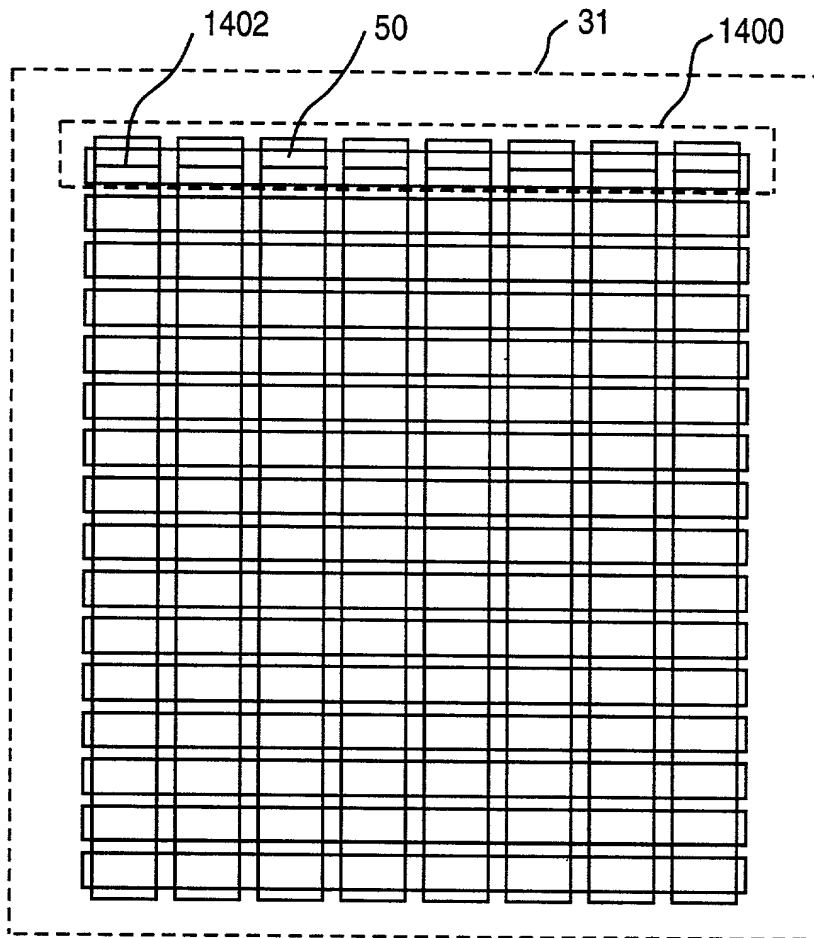
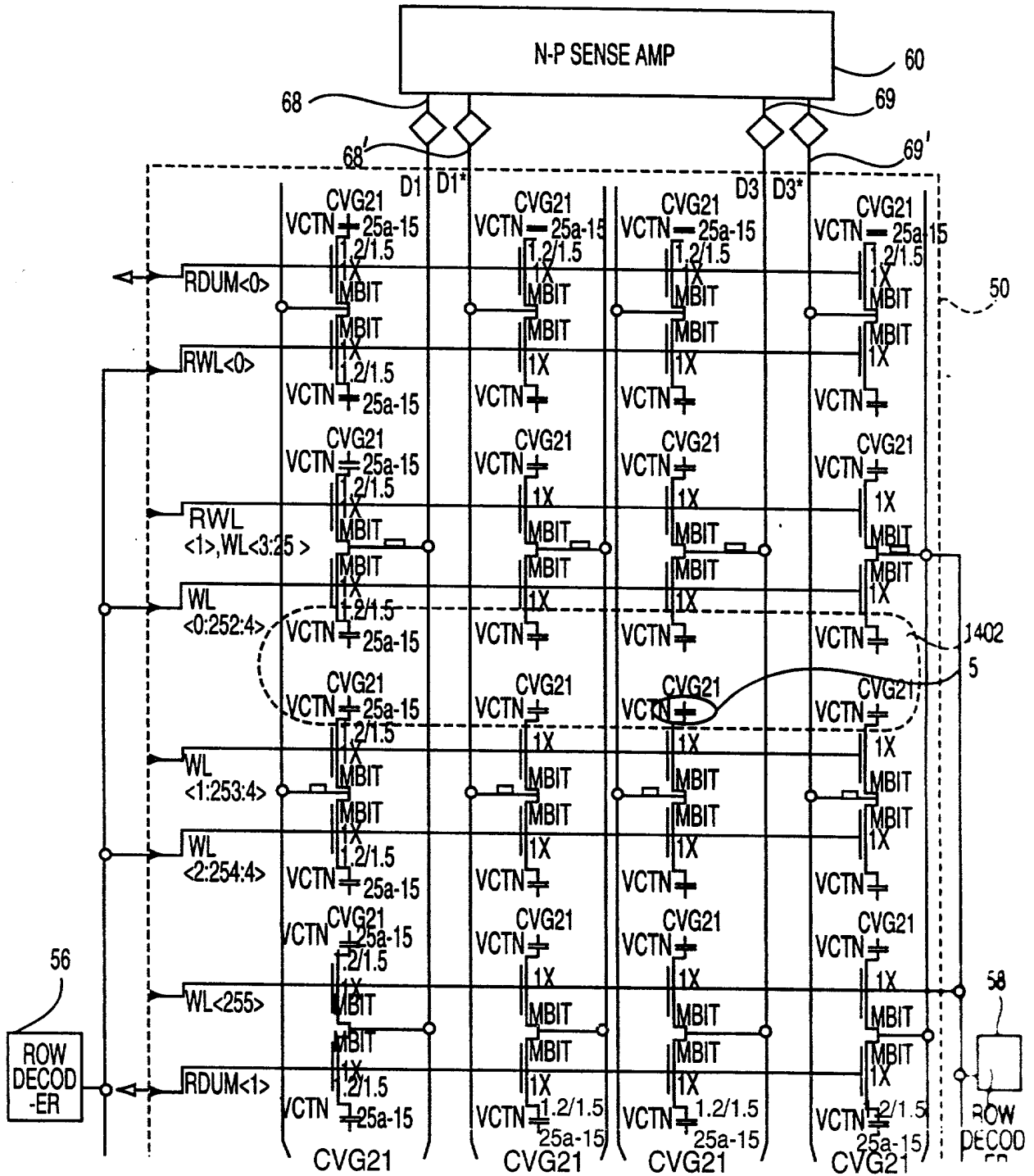


FIG. 108

FIG. 109-1

FIG. 109-1

FIG. 109-2



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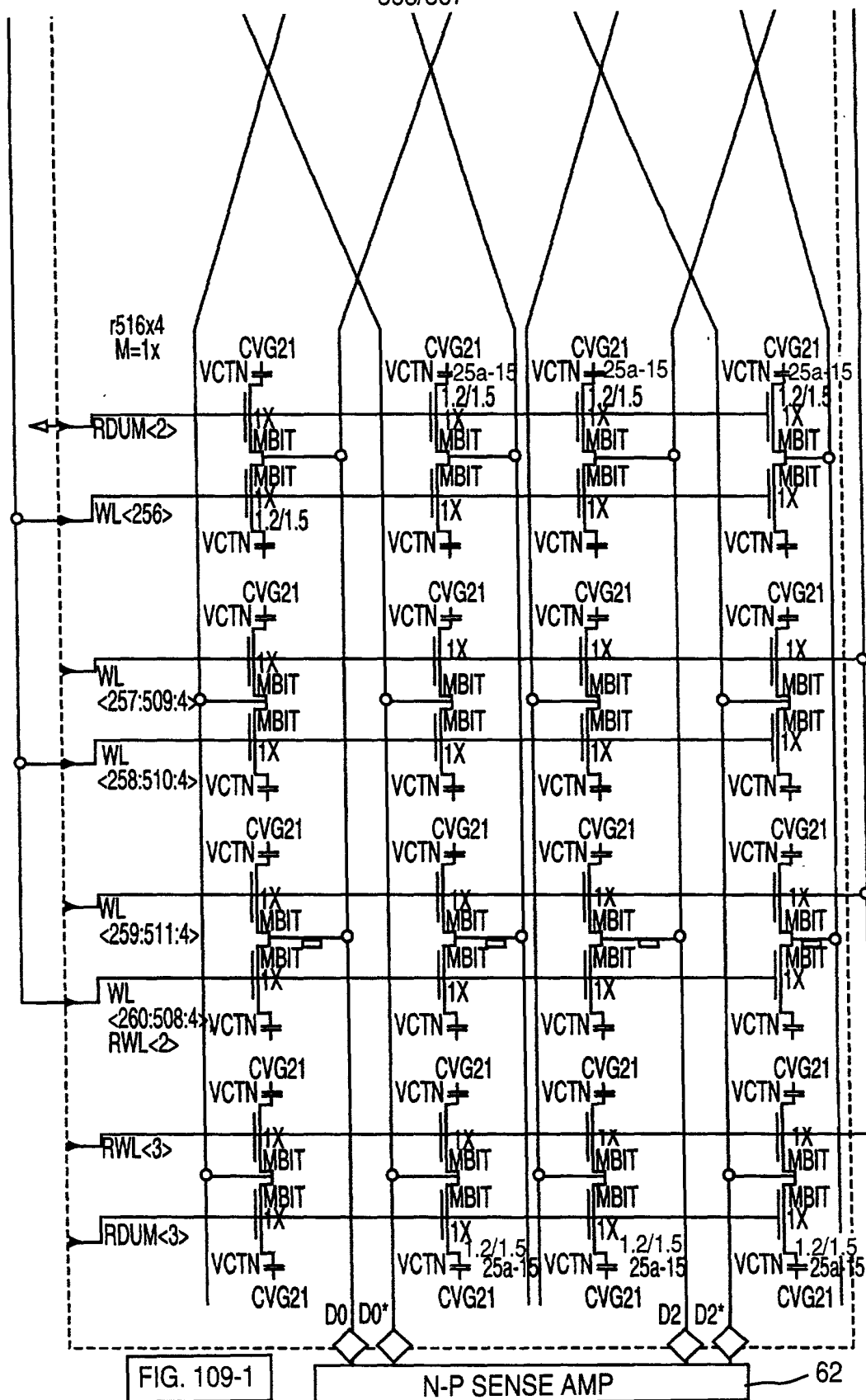


FIG. 109-1

FIG. 109-2

FIG. 109-2

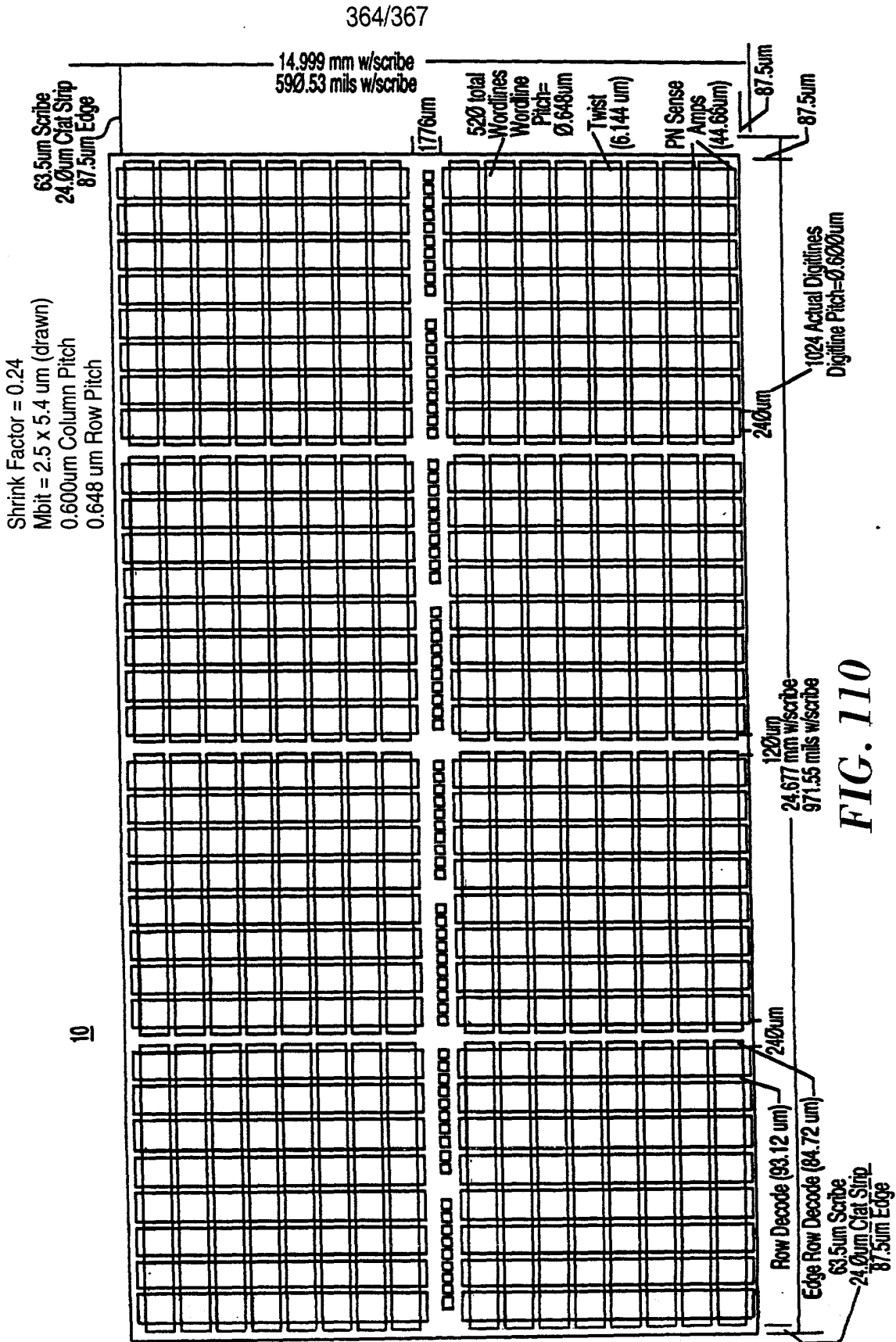


FIG. 110

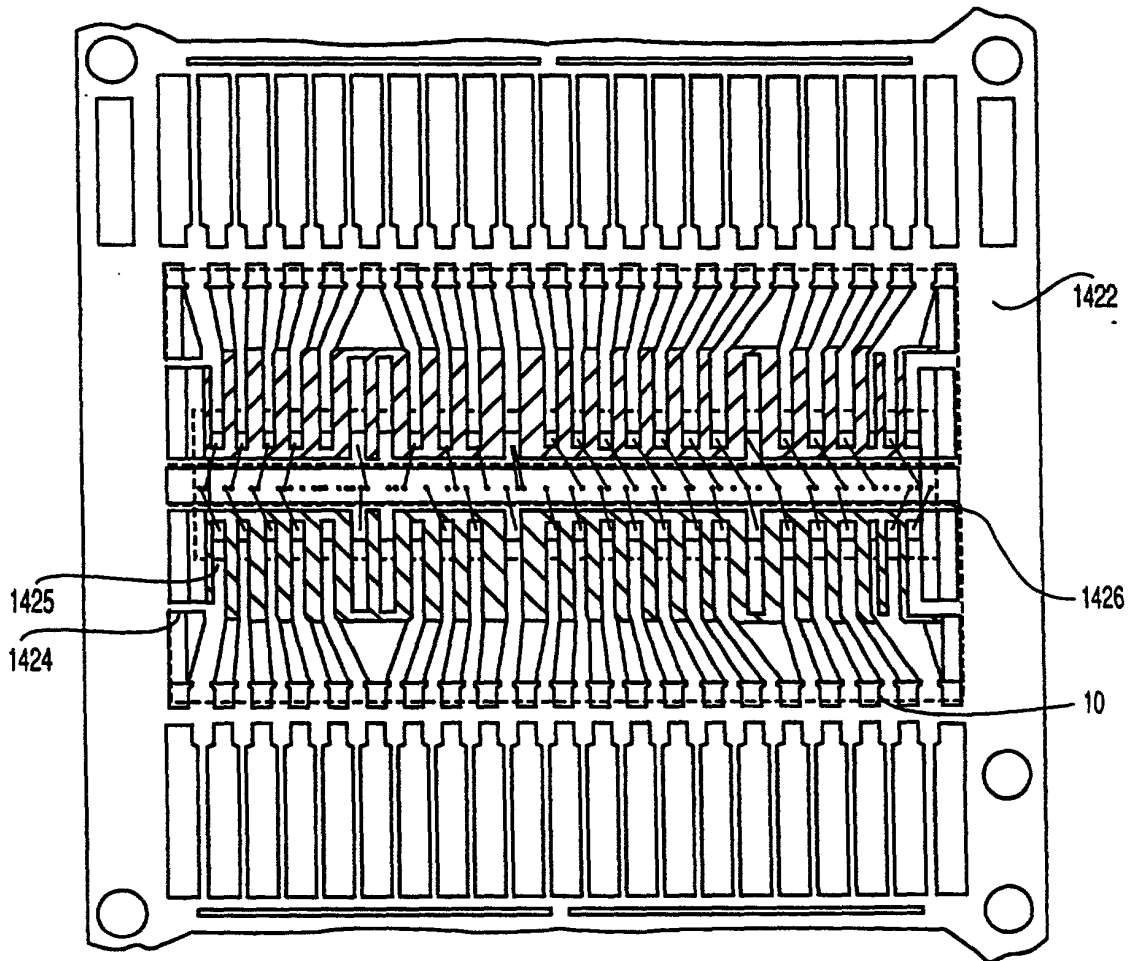


FIG. 111

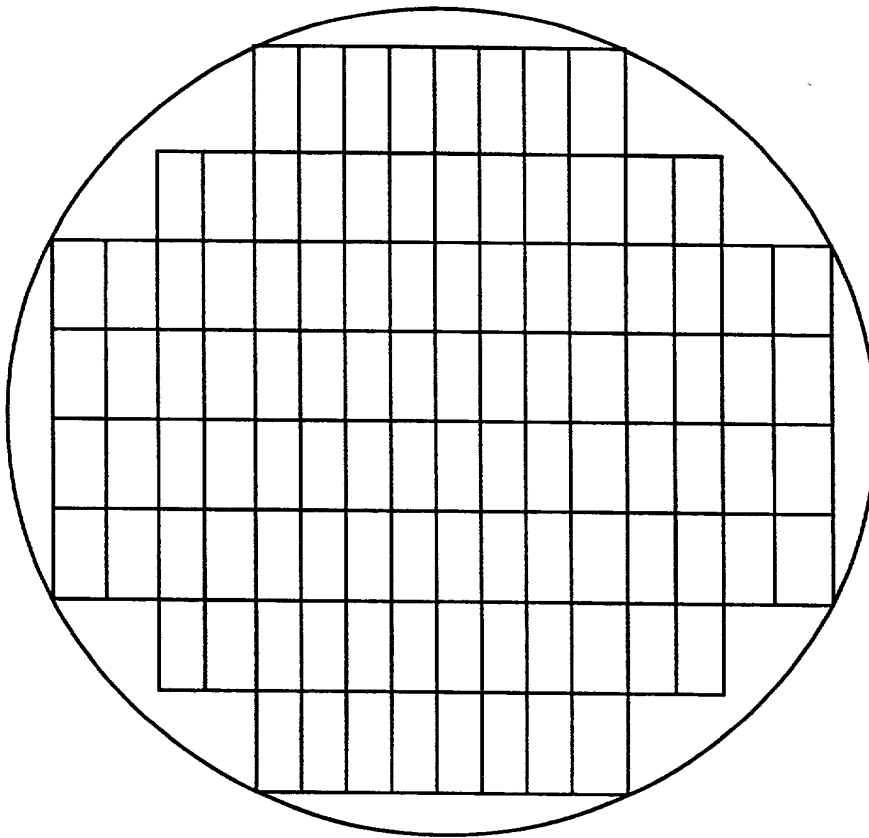
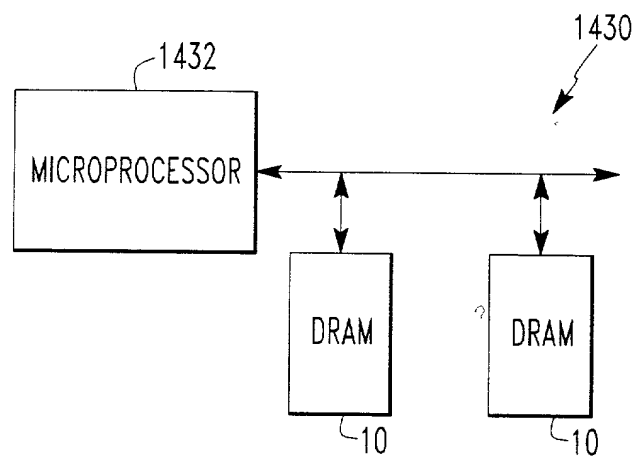


FIG. 112

*FIG. 113*